Multilayer Ceramic Chip Capacitor

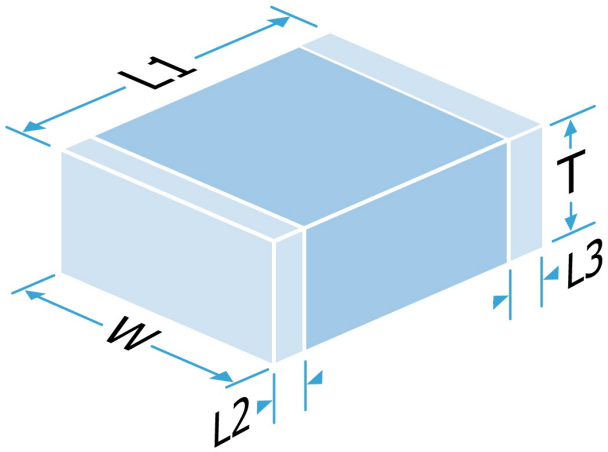
Part Number: 5550B184K202NT	**Description:** 5550 2000Vdc 180nF ±10% X7R (2R1) - Contains Lead

A range of X7R MLC capacitors to suit a variety of applications. In a wide selection of chip sizes, rated voltages and terminations, including FlexiCap™, the world's first commercially available flexible termination.

WS2, WR2, WS3 and WR3 parts use StackiCap™ patented construction technology.

DR1, WR2 and WR3 parts have a voltage de-rating above 105°C.

Suffix code PXX or PX mandates the use of precious metal electrode (PME) materials. This may incur additional costs.



Mechanical Specification

Size Code	5550
Length (L1) in mm (")	14.0 ± 0.711 (0.550 ± 0.028)
Width (W) in mm (")	12.7 ± 0.635 (0.500 ± 0.025)
Thickness (T) in mm (")	7.62 Max (0.3 Max)
Minimum Termination Band (L2,L3) in mm (")	0.50 (0.020)
Maximum Termination Band (L2,L3) in mm (")	1.50 (0.060)
Termination Material	Nickel Barrier, Sn Plated Solder (RoHS compliant)
Solderability	Per MIL-STD-202, Method 208
Packaging	Tape and Reel, 200 per reel
Conformal Coating	

General Electrical Specification

Rated Voltage	2000Vdc
Nominal Capacitance Value	180nF
Capacitance Tolerance	±10%
Tangent of Loss Angle (Tan δ)	≤0.025
Capacitance and Tan δ Test Conditions	1.0Vrms @ 1kHz
Voltage Proof (Voltage applied for 5 secs max. @ 50mA max. charge current. 50% Max, RH)	2400Vdc
Min Insulation Resistance (IR)	5.56GOhm @ 100Vdc
Dielectric Classification	X7R (2R1) - Contains Lead
Rated Temperature Range	-55°C / +125°C
Maximum Capacitance Change over Temperature Range	No DC Voltage ±15% Rated DC Voltage -
Climatic Category (IEC)	-
Ageing Characteristic	<2% per decade (nominal capacitance is 1000 hour value)

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This datasheet is for a standard item and is confirmed valid on the date generated, the latest published data for this part may differ and is available at http://www.knowlescapacitors.com or by contacting us.

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Data is correct to the best of our knowledge, errors and omissions excepted.

Date: Thursday, October 15, 2026

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Environmental

RoHS Compliant to 2011/65/EC as amended by 2015/863/EU	Compliant with exemption 7(c)-II
REACH Compliant	Contains 1 to 8% w/w Lead Titanium Oxide (PbTiO3, CAS 12060-00-3)
California Proposition 65	No exposure risk

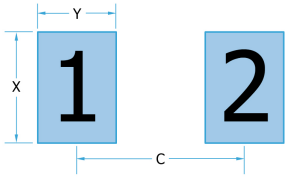
Board Layout

Knowles' conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should be considered.

Some high voltage parts may require modifications to the board layout and/or the addition of a conformal coating to prevent flashover, especially under high humidity conditions. Board cleanliness and environmental conditions can also impact this. Refer to application note AN0043 for further information.

IPC-7351 pad design

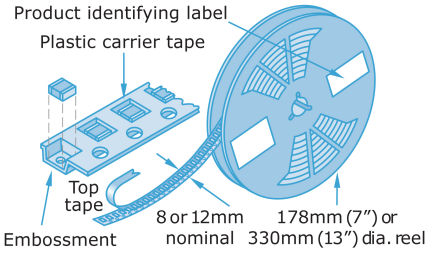
	5550	
C	13.20mm	0.520"
Y	2.20mm	0.087"
X	13.35mm	0.526"



Packaging

Tape packaging information for tape-and-reel parts:

Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.



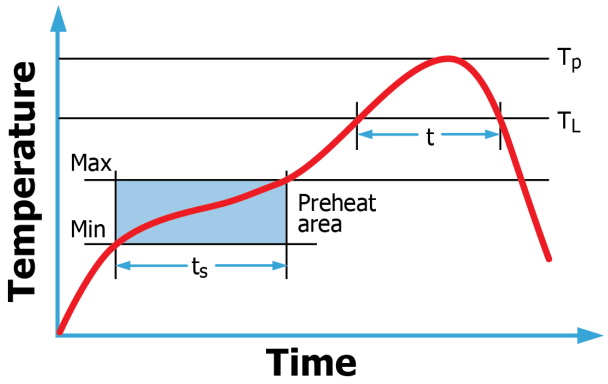
Soldering

Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness >1.0mm. Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.

PdAg terminations are primarily intended for conductive epoxy attachment - they may be suitable for soldering but trials are recommended.



Application notes with mounting and handling guidance are available on request.

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