USB 48V EPR Port Protector for CC & SBU

Features

- CC Switches: 1.25A, 300mΩ, 50pF, 180MHz
  - Automatic 5.1kΩ dead battery pull-down
- SBU Switches: 4.5Ω, 9pF, 900MHz
  - Thunderbolt™ Compatible
- USB PD3.0 SPR & PD3.1 48V EPR Compatible
  - $63V_{DC}$ Short-to-VBUS on CC1/2, SBU1/2
  - 1x/0.42x VBUS Level Shift for 48V → 20V
  - VBUS EPR Blocking via external NFET
- Overvoltage Protection
  - CC1/2 OVP = 5.9V
  - SBU1/2 OVP = 4.2V
  - Fast 60ns Response Time
- IEC61000-4-5 Surge Protection
  - +90V Surge Tolerance on CC1/2
  - +90V Surge Tolerance on SBU1/2
- IEC61000-4-2 ESD Protection
  - ±15kV air gap on CC1/2, SBU1/2
  - ±8kV contact on CC1/2, SBU1/2
  - ±2kV HBM on all pins (JEDEC JS-001-2017)
- 2.7V to 4.5V Operating Supply Voltage Range
- -40°C to 85°C Operating Temperature Range
- 20-pin WQFN 3mmx3mm (0.4mm pitch)
  - Pin-to-Pin Drop-In with TPD4S480

Brief Description

The KTU1133 provides safety management for USB PD3.1 48V EPR ports with comprehensive protection of the CC and SBU data lines. All four data lines include $63V_{DC}$ withstand for short-to-VBUS fault events in the connector and integrated transient voltage suppression (TVS) for IEC surge protection and IEC level-4 ESD protection. Fast over-voltage protection (OVP) isolates downstream system circuits during fault events.

The integrated VBUS level shift circuit and external blocking NFET gate driver allow SPR-rated PD controllers to safely operate in EPR systems.

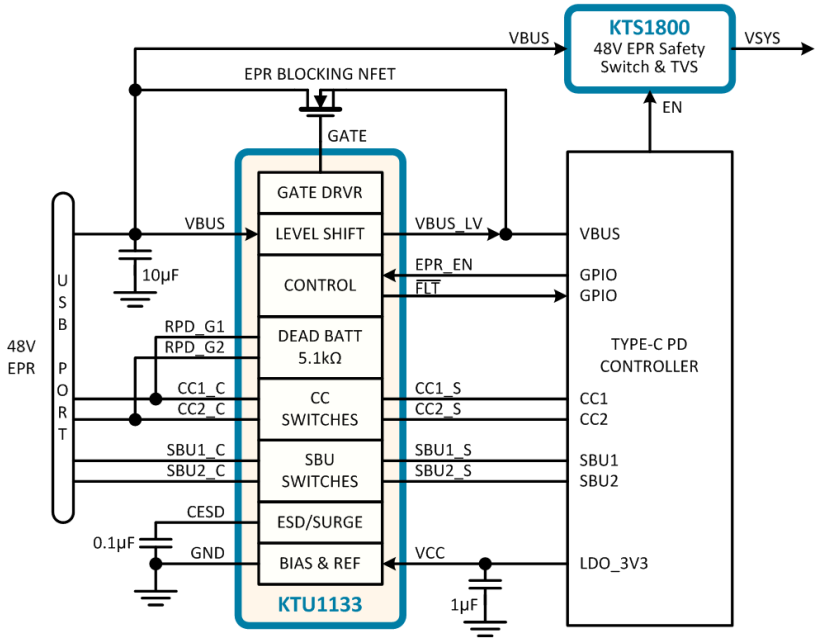
The CC1/2 switches have low on-resistance for passing V_{CONN} power up to 1.25A. During dead battery conditions, optional-use internal 5.1kΩ resistors automatically pull down on CC1/2 to ensure that the up-stream source provides 5V on VBUS.

The KTU1133 is packaged in RoHS and Green compliant 20-pin 3mm x 3mm WQFN package.

Applications

- Desktop PC, Workstation & Gaming Notebooks
- Monitors, Docking Stations, Conferencing Systems

Typical Application

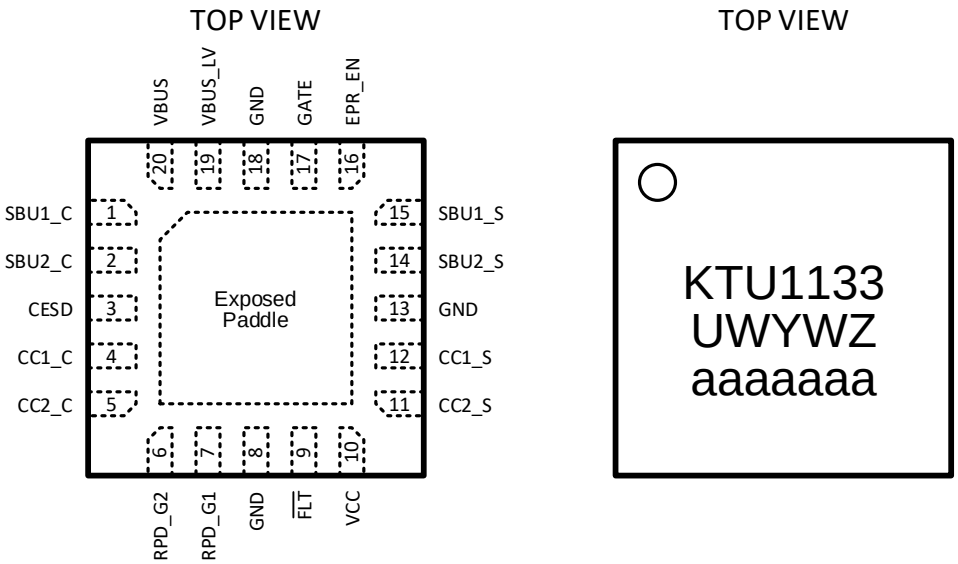


Ordering Information

Part Number	Marking[1]	Operating Temperature	Package
KTU1133EUAJ-TD	UWYWZ aaaaaaa	-40°C to +85°C	WQFN33-20

Pinout Diagram

WQFN33-20



20-pin 3mm x 3mm x 0.75mm WQFN Package, 0.4mm pitch

Top Mark

UW = Device ID, YW = Date Code, Z = Serial Number

aaaaaaa = Assembly Lot Tracking Number

1. UW = Device ID, YW = Date Code, Z = Serial Number, aaaaaaa = Assembly Lot Tracking Number.

Pin Descriptions

Pin #	Name	Function
12	CC1_S	System side of CC1 switch
11	CC2_S	System side of CC2 switch
4	CC1_C	Connector side of CC1 switch
5	CC2_C	Connector side of CC2 switch
1	SBU1_C	Connector side of SBU1 switch – alternatively, use to protect the USB2.0 D+/- path.
2	SBU2_C	Connector side of SBU2 switch – alternatively, use to protect the USB2.0 D+/- path.
15	SBU1_S	System side of SBU1 switch – alternatively, use to protect the USB2.0 D+/- path.
14	SBU2_S	System side of SBU2 switch – alternatively, use to protect the USB2.0 D+/- path.
7	RPD_G1	Dead battery pull-down resistor – connect to CC1_C if needed; connect to GND if not required.
6	RPD_G2	Dead battery pull-down resistor – connect to CC2_C if needed; connect to GND if not required.
9	$\overline{FLT}$	Active-low, open-drain fault flag output to alert system to an OVP fault condition – connect to GND if not required.
8, 13, 18	GND	Ground – connect to PCB ground plane.
3	CESD	Capacitor connection for ESD/surge protection – connect a 0.1µF capacitor from CESD to GND.
10	VCC	Device supply input – connect to a 2.5V to 4.5V power source.
20	VBUS	VBUS level shifter input – connect to VBUS on the connector.
19	VBUS_LV	VBUS level shifter output – 1x pass-through output is enabled in SPR mode; 0.42x divider output is enabled in EPR mode.
16	EPR_EN	EPR mode enable input – logic 0 = SPR mode; logic 1 = EPR mode.
17	GATE	Gate drive output to optional VBUS NFET – gate drive is enabled in SPR mode; gate drive is disabled in EPR mode to block high VBUS voltage from reaching the PD controller.
EP	EP	Exposed paddle – connect to GND pins and to PCB ground plane for thermal conduction.

Absolute Maximum Ratings[2]

Symbol	Description	Value	Units
V_{CC}	VCC to GND	-0.3 to 5	V
V_{LOGIC}	EPR_EN to GND	-0.3 to 3.6	V
	$\overline{FLT}$ to GND	-0.3 to 6	
V_{BUS}	VBUS to GND (continuous)	-0.3 to 63	V
	VBUS to GND (during IEC61000-4-5 surge event with external TVS)	-4 to 70	
V_{BUS_LV}	VBUS_LV to GND (continuous)	-0.3 to 24	V
V_{GATE}	GATE to GND	-0.3 to 30	V
$V_{RPD\_G1/2}$ $V_{CC1/2\_C}$ $V_{SBU1/2\_C}$	RPD_G1, RPD_G2 to GND CC1_C, CC2_C to GND SBU1_C, SBU2_C to GND	-0.3 to 63	V
V_{CESD}	CESD to GND	-0.3 to 63	V
$V_{CC1/2\_S}$ $V_{SBU1/2\_S}$	CC1_S, CC2_S to GND SBU1_S, SBU2_S to GND	-0.3 to 6	V
$I_{CC1/2}$	CC1_C to CC1_S, CC2_C to CC2_S Continuous Current	±1.25	A
$I_{SBU1/2}$	SBU1_C to SBU1_S, SBU2_C to SBU2_S Continuous Current	±100	mA
T_J	Die Junction Operating Temperature Range	-40 to 125	°C
T_S	Storage Temperature Range	-55 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

ESD and Surge Ratings[3]

Symbol	Description	Value	Units
V_{ESD_HBM}	JEDEC JS-001-2017 Human Body Model (all pins)	±2	kV
V_{ESD_CDM}	JEDEC JESD22-C101 Charged Device Model (all pins)	±500	V
V_{ESD_CD}	IEC61000-4-2 Contact Discharge (CC1_C, CC2_C, SBU1_C, SBU2_C)	±8	kV
V_{ESD_AGD}	IEC61000-4-2 Air Gap Discharge (CC1_C, CC2_C, SBU1_C, SBU2_C)	±15	kV
V_{SURGE}	IEC61000-4-5 Surge (CC1_C, CC2_C) IEC61000-4-5 Surge (SBU1_C, SBU2_C)	+90 +90	V V

Thermal Capabilities[4]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	60	°C/W
P_D	Maximum Power Dissipation at $T_A \leq 25°C$ ($T_J \leq 125°C$)	1.67	W
$\Delta P_D/\Delta T$	Derating Factor Above $T_A = 25°C$	-16.7	mW/°C

2. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
3. ESD and Surge Ratings conform to JEDEC and IEC industry standards. Some pins may actually have higher performance. Surge ratings apply with chip enabled, disabled, or unpowered, unless otherwise noted.
4. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to a PCB with thermal vias from the exposed paddle to the ground plane.

Recommended Operating Conditions[5]

Symbol	Description	Value	Units
V_{CC}	VCC Operating Voltage	2.7 to 4.5	V
V_{LOGIC}	EPR_EN Input Voltage	0 to V_{CC}	V
	$\overline{FLT}$ Output Pull-Up Voltage	2.7 to 5.5	
V_{BUS}	VBUS Input Voltage	0 to 55	V
V_{BUS_LV}	VBUS_LV Voltage	0 to 23	V
$V_{RPD\_G1/2}$	RPD_G1, RPD_G2 Input Voltage	0 to 5.9	V
$V_{CC1/2\_C}$	CC1_C, CC2_C Input/Output Voltage	0 to 5.9	V
$V_{SBU1/2\_C}$	SBU1_C, SBU2_C Input/Output Voltage	0 to 4.2	V
$V_{CC1/2\_S}$	CC1_S, CC2_S Input/Output Voltage	0 to 5.9	V
$V_{SBU1/2\_S}$	SBU1_S, SBU2_S Input/Output Voltage	0 to 4.2	V
$I_{CC1/2}$	CC1_C to CC1_S, CC2_C to CC2_S Current	±1.25	A
T_A	Ambient Operating Temperature Range	-40 to 85	°C
T_J	Die Junction Operating Temperature Range	-40 to 125	°C
C_{VCC}	VCC External Capacitor	1	µF
		6.3	V
$R_{\overline{FLT}}$	$\overline{FLT}$ External Pull-Up Resistor	1.7 to 300	kΩ
C_{VBUS}	VBUS External Capacitor	1 to 10	µF
		100	V
C_{VBUS_LV}	VBUS_LV External Capacitor	0.1	µF
		25	V
C_{ESD}	CESD External Capacitor	0.1	µF
		100	V

5. The recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Kinetic does not recommend exceeding them or designing to Absolute Maximum Rating.

Electrical Characteristics[6]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_A = -40°C to +85°C with V_{CC} = 2.7V to 4.5V. Typical values are specified at T_A = +25°C with V_{CC} = 3.3V.

Supply Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{CC}	VCC Supply Operating Voltage Range[7]		2.7		4.5	V
V_{UVLO}	VCC Under-Voltage Lockout	Rising threshold	2.1	2.3	2.65	V
		Hysteresis		100		mV
I_{CC}	VCC No-Load Supply Current	VCC = 3.3 V (typical), VCC = 4.5 V (maximum). –40°C ≤ T_J ≤ +85°C		110	140	µA

Logic Pin Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_I	Input Logic Threshold (EPR_EN)	Rising			0.73*V_{CC}	V
		Falling	0.27*V_{CC}			
R_{I_PD}	Input Logic Pull-Down (EPR_EN)			1		MΩ
V_{OL}	Output Logic Low ($\overline{FLT}$)	I_{O_SINK} = 1mA		0.01	0.2	V
		I_{O_SINK} = 3mA			0.4	
I_{O_LK}	Output Logic High-Z Leakage ($\overline{FLT}$)	V_O = 5V	-1		1	µA
$t_{\overline{FLT}}$	$\overline{FLT}$ Flag Response Time	Assertion		20		µs
		Deassertion debounce[8]		5		ms

Over-Temperature Protection (OTP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{OTP}	Over-Temperature Protection Threshold	T_J rising threshold T_J falling threshold Hysteresis	150 130	175 140 35		°C

TVS Surge Clamp Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{TVS_WRK}	Clamp Working Voltage		-0.3		60	V
V_{TVS_CLMP}	Clamp Breakdown Voltage	I_{IN} = 1mA		64		V

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6. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization, and correlation with statistical process controls.
7. To guarantee normal startup logical operation, the minimum ramp up time of VCC from 0V to >V_{UVLO} shall be longer than 0.5ms.
8. CC and SBU channels turn on before the $\overline{FLT}$ flag is deasserted and the dead battery resistors are turned off.

Electrical Characteristics (continued)[9]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_A = -40°C to +85°C with V_{CC} = 2.7V to 4.5V. Typical values are specified at T_A = +25°C with V_{CC} = 3.3V.

CC OVP Switch Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{ON_CC}	CC On-Resistance	V_{CCxC} = 0 to 5.5V, $T_J \leq$ +85°C		300	420	mΩ
I_{LK_CC}	CC Off-Leakage Current	V_{CC} = 0V, V_{CCx_C} = 5.5V, V_{CCx_S} = 0V, T_A = +25°C, measure current out of CCx_S		0.1	5	µA
I_{LK_CC-GND}	CC ON-Leakage Current to GND	V_{CC} = 3.3V, V_{CCx_C} = 3.6V, V_{CCx_S} = floating, T_A = +25°C, measure current into CCx_C		1	5	µA
C_{ON_CC}	CC On-Capacitance[10]	From CCx_C or CCx_S to GND when device is powered, V_{CCx_C} or V_{CCx_S} = 0V to 1.2V, f = 400kHz		50		pF
BW_{ON_CC}	CC On-Bandwidth[10]	-3dB bandwidth from CCx_C to CCx_S, single-ended, 50Ω system, V_{CM} = 0.1V to 1.2V		180		MHz
V_{STBUS_CC}	CCx_C Short-to-VBUS Tolerance[10]	Hot-plug CCx_C with 1m USB type-C cable, 30Ω load on CCx_S			55	V
V_{OVP_CC}	CCx_C OVP Threshold Voltage	Rising threshold	5.6	5.9	6.2	V
		Hysteresis		200		mV
t_{OVP_CC}	CCx_C OVP Response Time[10]	Rising		60		ns
		Falling debounce		0.9		ms
V_{MAX_CC}	CCx_S Rising Maximum Voltage[10]	During V_{STBUS_CC} or surge event		7		V
t_{ON_CC}	CC Turn-On Time	V_{CC} rising > V_{UVLO}		1.3	3.5	ms
t_{OFF_CC}	CC Turn-Off Time[10]	V_{CC} falling < V_{UVLO}		5		µs
R_{DB}	Dead Battery Pull-Down Resistance	V_{CC} < V_{UVLO}, V_{CCx_C} = 2.6V	4.1	5.1	6.1	kΩ
V_{DB}	RPD_Gx Dead Battery Threshold Voltage	V_{CC} < V_{UVLO}, I_{CCx_C} = 80 µA	0.5	0.9	1.2	V
t_{OFF_DB}	Dead Battery Resistor Turn-Off Delay[11]	V_{CC} rising > V_{UVLO} debounce		5.7	9.5	ms
		V_{CCx_C} falling < V_{OVP_CC} debounce		5		
I_{LK_CCOVP}	CC OVP Leakage Current	V_{CC} = 0 or 3.3V, V_{CCx_C} = 55V, V_{CCx_S} = 0V, T_A = +25°C, measure current into CCx_C			200	µA
		V_{CC} = 0 or 3.3V, V_{CCx_C} = 55V, V_{CCx_S} = 0V, T_A = +25°C, measure current out of CCx_S			1	

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9. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization, and correlation with statistical process controls.
10. Guaranteed by characterization and/or simulation.
11. CC and SBU channels turn on before the $\overline{FLT}$ flag is deasserted and the dead battery resistors are turned off.

Electrical Characteristics (continued)[12]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_A = -40°C to +85°C with V_{CC} = 2.7V to 4.5V. Typical values are specified at T_A = +25°C with V_{CC} = 3.3V.

SBU OVP Switch Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{ON_SBU}	SBU On-Resistance	V_{SBUxC} = 0 to 3.6V, $T_J \leq$ +85°C		4.5	6.5	Ω
I_{LK_SBU}	SBU Off-Leakage Current	V_{CC} = 0V, V_{SBUx_C} = 3.6V, V_{SBUx_S} = 0V, T_A = +25°C, measure current out of SBUx_S		0.1	3	µA
$I_{LK\_SBU-GND}$	SBU On-Leakage Current to GND	V_{CC} = 3.3V, V_{SBUx_C} = 3.6V, V_{SBUx_S} = floating, T_A = +25°C, measure current into SBUx_C		1	3	µA
C_{ON_SBU}	SBU On-Capacitance[13]	From SBUx_C or SBUx_S to GND when device is powered, V_{SBUx_C} or V_{SBUx_S} = 0.3V to 3.6V, f = 400kHz		9		pF
BW_{ON_SBU}	SBU On-Bandwidth[13]	-3dB bandwidth from SBUx_C to SBUx_S, single-ended, 50Ω system, V_{CM} = 0.1V to 3.6V		900		MHz
X_{TALK_SBU}	SBU Crosstalk[13]	From SBU1_S to SBU2C or SBU2_S to SBU1_C when device is powered, V_{CM1} = 3.6V, V_{CM2} = 0.3V to 3.6V, f = 1MHz, 50Ω open side termination		-70		dB
V_{STBUS_SBU}	SBUx_C Short-to-VBUS Tolerance[13]	Hot-plug SBUx_C with 1m USB type-C cable, 30Ω load on SBUx_S			55	V
V_{OVP_SBU}	SBUx_C OVP Threshold Voltage	Rising threshold	4.0	4.2	4.4	V
		Hysteresis		100		mV
t_{OVP_SBU}	SBUx_C OVP Response Time[13]	Rising		60		ns
		Falling debounce		0.6		ms
V_{MAX_SBU}	SBUx_S Rising Maximum Voltage[13]	During V_{STBUS_SBU} or surge event		6.5		V
t_{ON_SBU}	SBU Turn-On Time	V_{CC} rising > V_{UVLO}		1.3	3.5	ms
t_{OFF_SBU}	SBU Turn-Off Time[13]	V_{CC} falling < V_{UVLO}		4		µs
I_{LK_SBUOVP}	SBU OVP Leakage Current	V_{CC} = 0 or 3.3V, V_{SBUx_C} = 55V, V_{SBUx_S} = 0V, T_A = +25°C, measure current into SBUx_C			200	µA
		V_{CC} = 0 or 3.3V, V_{SBUx_C} = 55V, V_{SBUx_S} = 0V, T_A = +25°C, measure current out of SBUx_S			1	

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12. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization, and correlation with statistical process controls.
13. Guaranteed by characterization and/or simulation.

Electrical Characteristics (continued)[14]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_A = -40°C to +85°C with V_{CC} = 2.7V to 4.5V. Typical values are specified at T_A = +25°C with V_{CC} = 3.3V.

EPR Level Shifter Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{BUS_DIV}	VBUS_LV to VBUS Divider Ratio (V_{BUS_LV}/V_{BUS})	SPR Mode: EPR_EN = 0, V_{BUS} = 4.5V to 21V, $I_{VBUS\_LV} \leq$ 20mA		1		V/V
		EPR Mode: EPR_EN = 1, V_{BUS} = 26.6V to 50.4V, $I_{VBUS\_LV} \leq$ 20mA		0.42		
I_{VBUS_LV}	VBUS_LV Output Load Current				20	mA
V_{F_VBUSLV}	VBUS to VBUS_LV Forward Voltage Drop[15]	EPR_EN = 0, V_{BUS} = 4.5V, I_{BUS_LV} = 20mA			100	mV
		EPR_EN = 0, V_{BUS} = 22V, I_{BUS_LV} = 20mA			100	
V_{EPR_VBUS}	Automatic EPR Mode Threshold Voltage	V_{BUS} rising			24.5	V
		V_{BUS} falling	22			

EPR Blocking Gate Driver Specifications

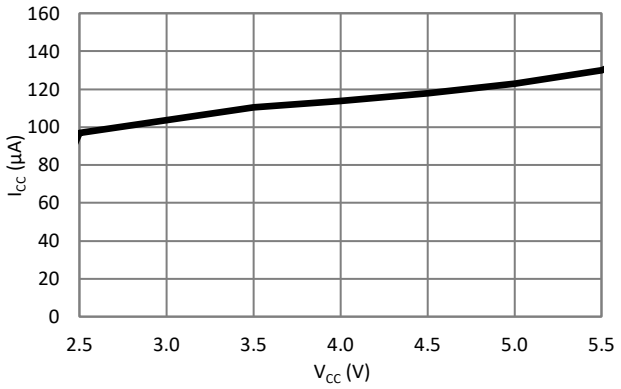
Symbol	Description	Conditions	Min	Typ	Max	Units
V_{EPR_GATE}	GATE Output Driver Voltage	$0 \leq V_{BUS} \leq$ 22V	5		12	V
I_{EPR_GATE}	GATE Output Driver Current	$0 \leq (V_{GATE} - V_{BUS}) \leq$ 5V, $0 \leq V_{BUS} \leq$ 22V		4		µA

14. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization, and correlation with statistical process controls.
15. $V_{F\_VBUSLV} = (V_{BUS\_DIV} \times V_{BUS}) - V_{BUS\_LV}$.

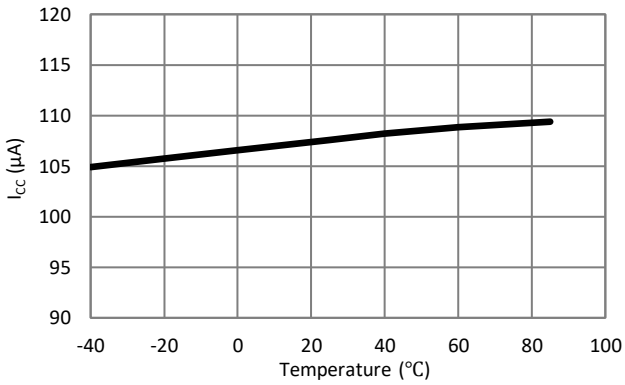
Typical Characteristics

V_{CC} = 3.3V and T_A = +25°C unless otherwise noted.

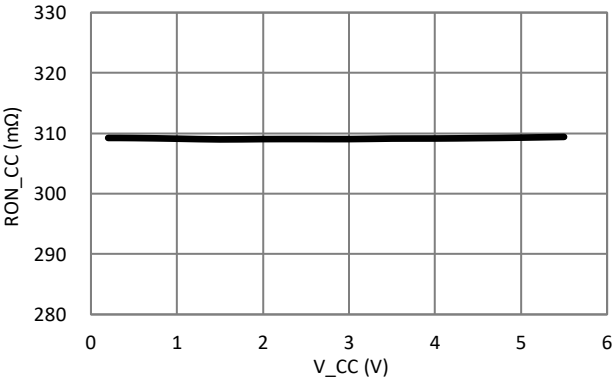
VCC Supply Current Vs. V_{CC} Voltage



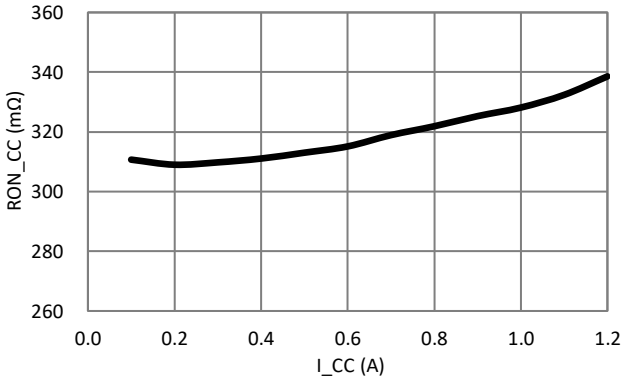
VCC Supply Current Vs. Temperature



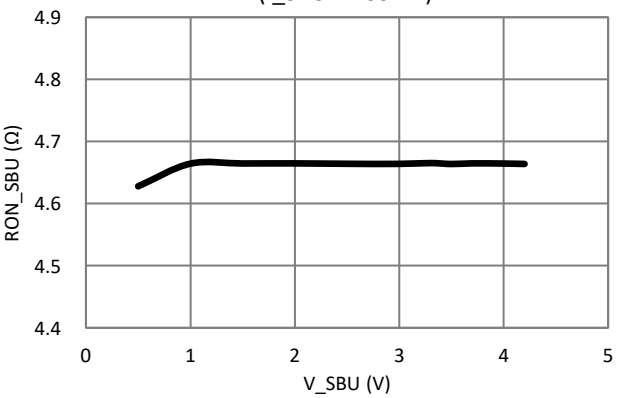
CC Switch R_{ON} VS. Switch Voltage
(I_CC = 200mA)



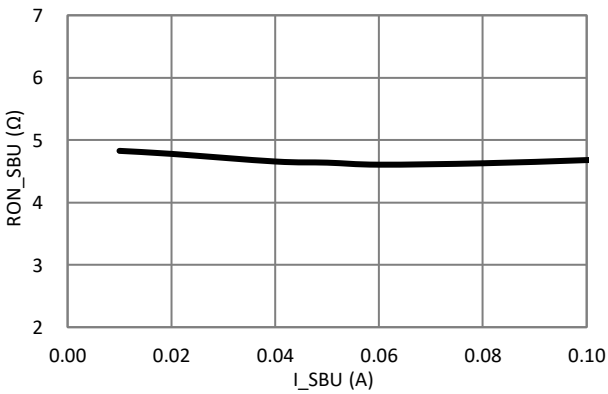
CC Switch R_{ON} VS. Switch Voltage



SBU Switch R_{ON} VS. Switch Voltage
(I_SBU = 100mA)



SBU Switch R_{ON} VS. Switch Voltage



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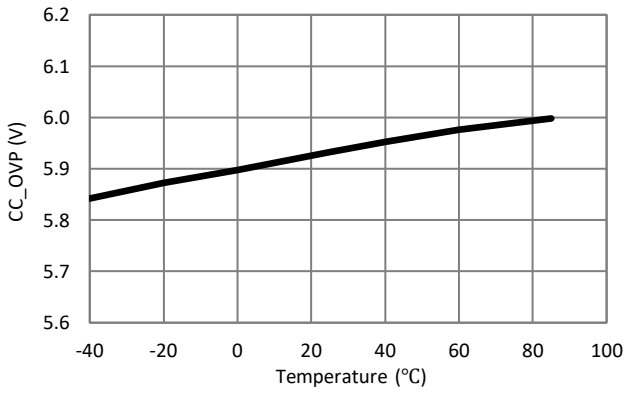
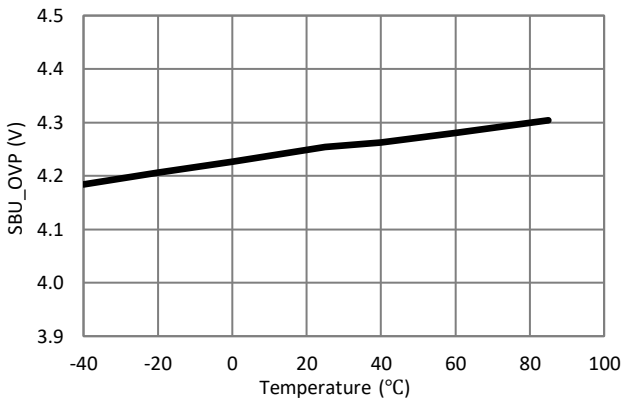
Typical Characteristics

V_{CC} = 3.3V and T_A = +25°C unless otherwise noted.

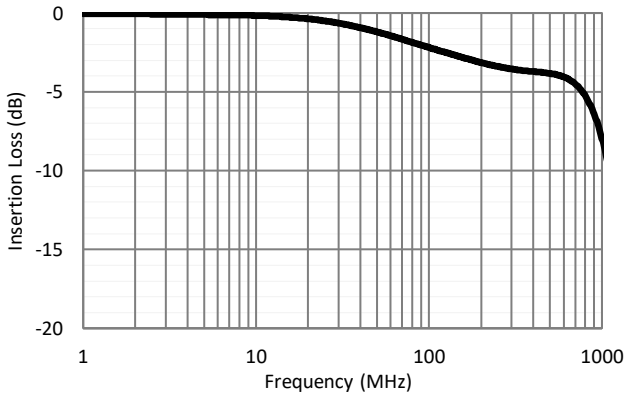
CC Switch OVP VS. Temperature



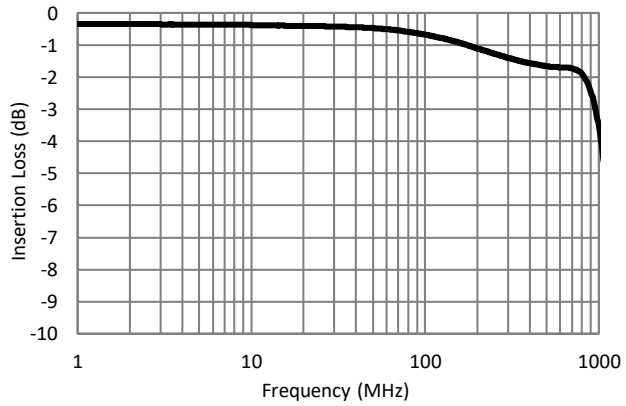
CC Switch OVP Level VS. Temperature



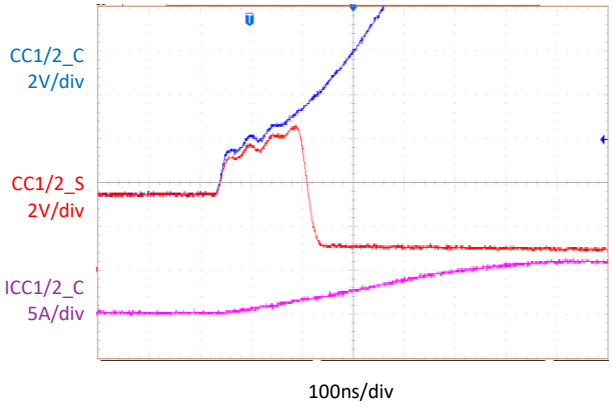
CC Switch OVP VS. Temperature



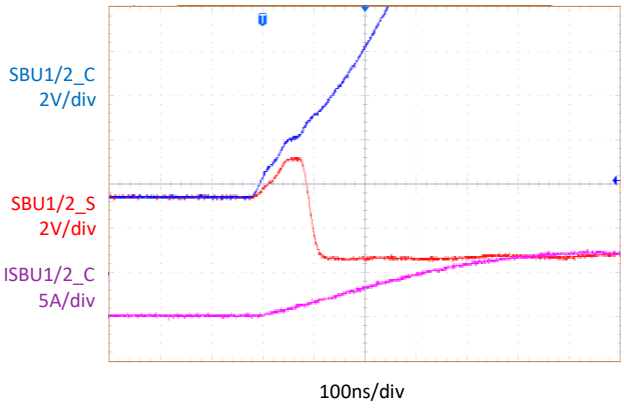
SBUx Switch Bandwidth



CCx_C Short-to-VBUS 48V



SBUx_C Short-to-VBUS 48V

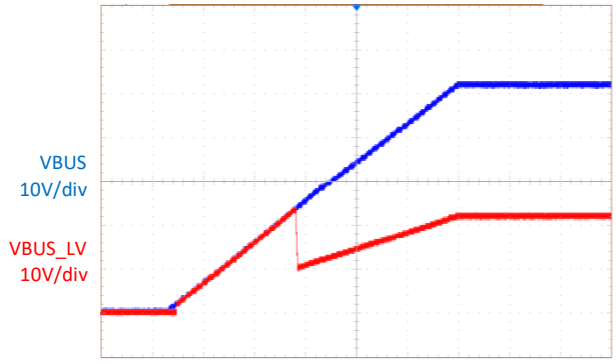


(continued next page)

Typical Characteristics

V_{CC} = 3.3V and T_A = +25°C unless otherwise noted.

EPR Level Shifter
(EPR_EN = Low)



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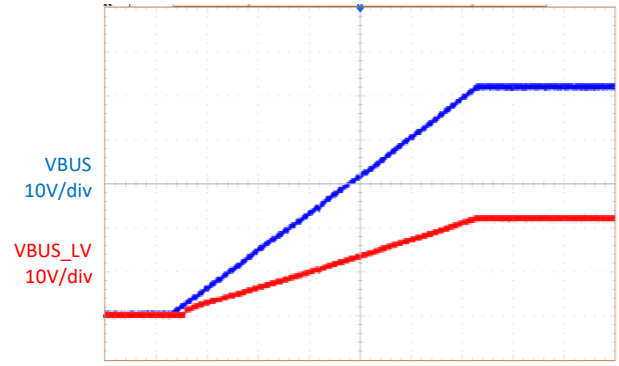
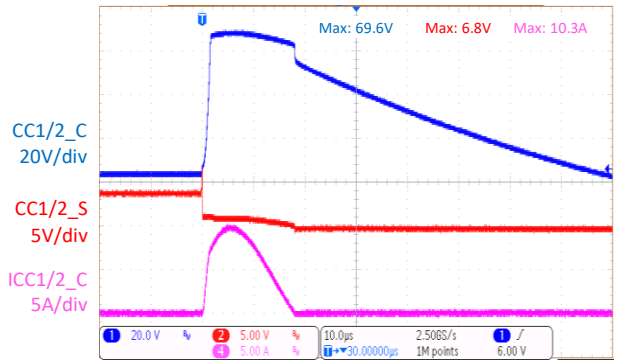
EPR Level Shifter
(EPR_EN = High)



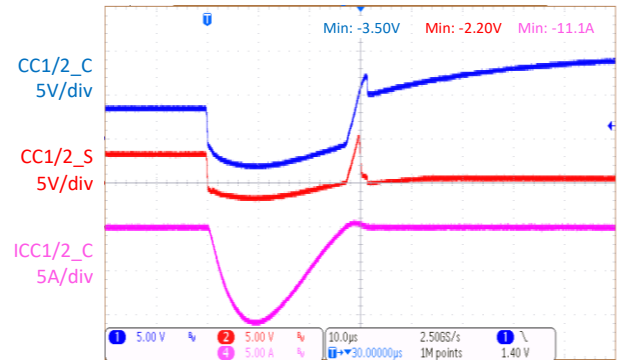
1.0s/div

CC OVP during + 90V Surge Event



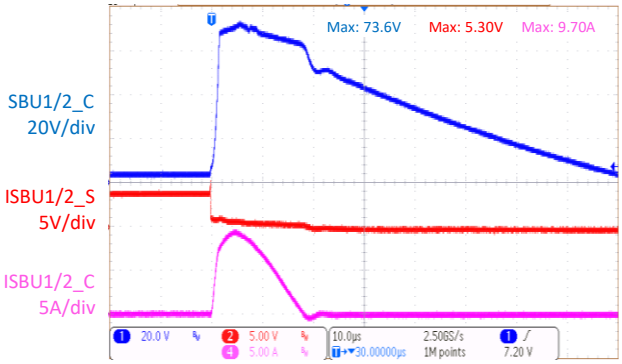
10µs/div

CC -30V Surge Event



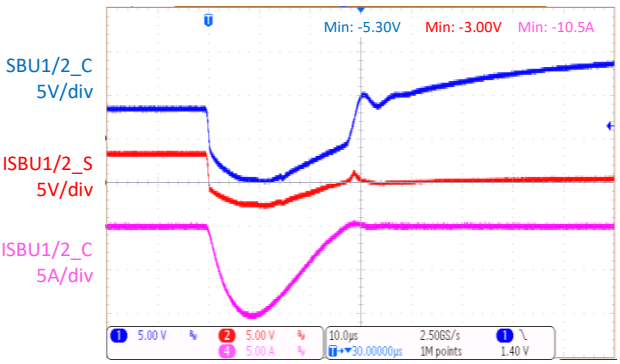
10µs/div

SBU OVP during + 90V Surge Event



10µs/div

SBU -30V Surge Event



10µs/div

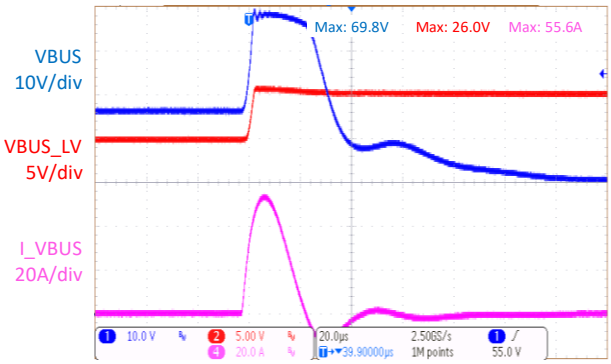
(continued next page)

Typical Characteristics

V_{CC} = 3.3V and T_A = +25°C unless otherwise noted.

Surge Transient Response

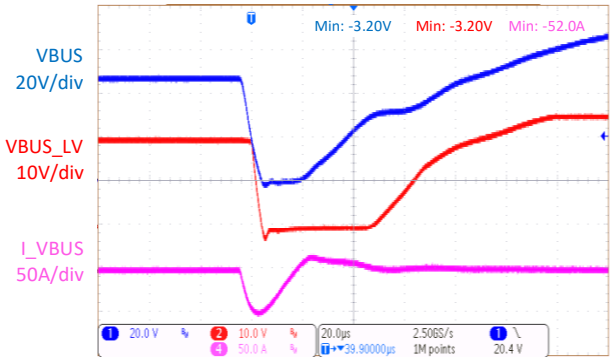
(VBUS = 48V + 130V Surge with KTS1800)



20µs/div

Surge Transient Response

(VBUS = 48V - 130V Surge with KTS1800)



20µs/div

Functional Block Diagram

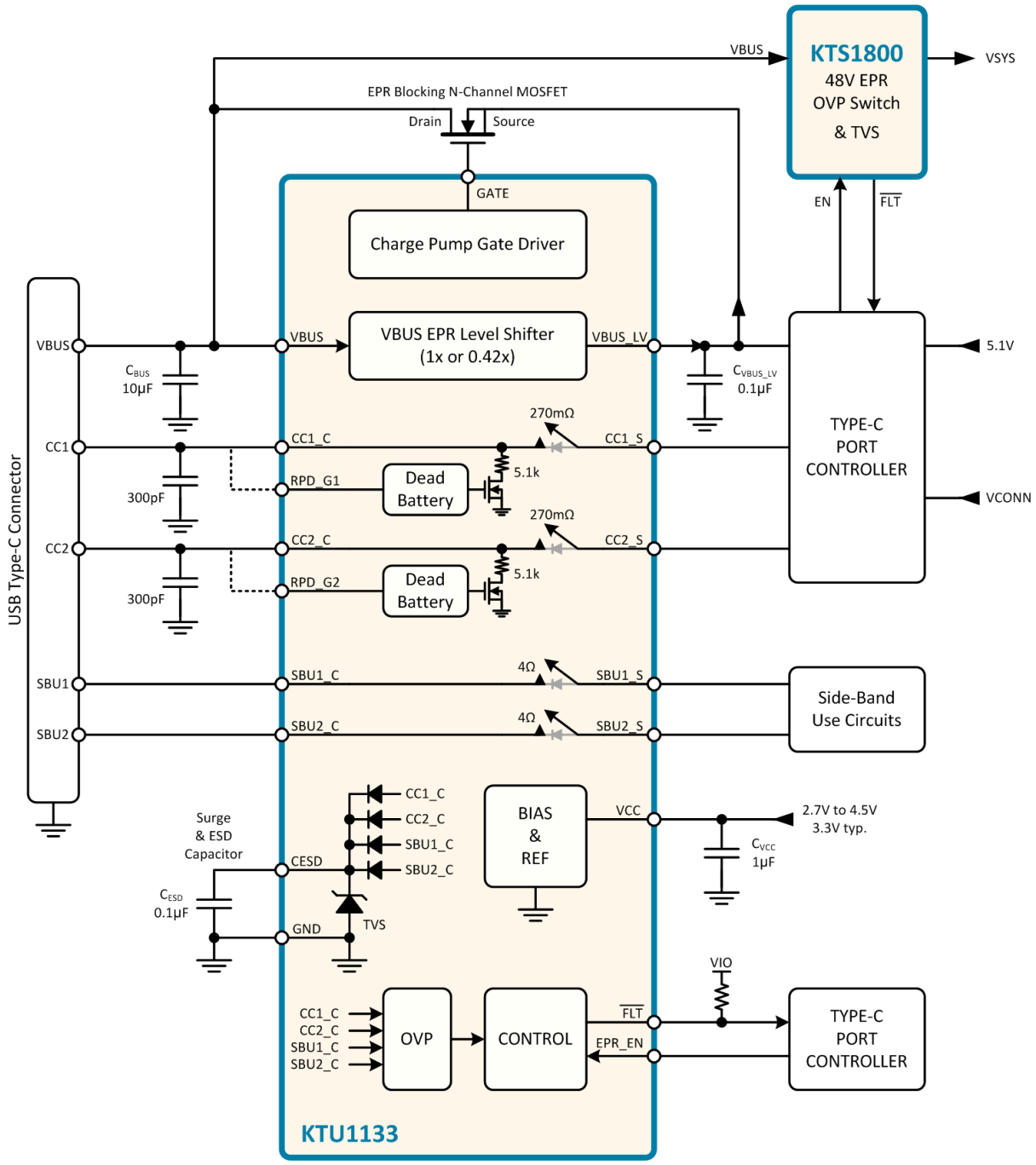


Figure 1. Functional Block Diagram

Functional Description

Overview

The KTU1133 provides comprehensive, single-chip protection for USB type-C PD3.1 extended power range (EPR) ports for the CC and SBU pins, as well as the VBUS path specifically to the PD controller. (See the KTS1800 for protecting the VBUS power path to the charger and/or system.) The KTU1133 enables the use of a 20V (nominal) PD controller in EPR systems that support up to 48V (nominal). It is a pin-to-pin alternate source for the TPD4S480.

Short-to-VBUS Protection

Although the CC and SBU data channels operate at low voltages, these pins are adjacent to VBUS in the type-C connector and vulnerable to short-to-VBUS fault events. Short-to-VBUS events may occur due to mechanical contact, debris, or moisture in the local-side connector or the connector at the other end of the USB cable. With relatively low capacitance on the CC and SBU lines and up to 10uF capacitance on VBUS that may be pre-charged to $48V_{DC}$, the voltage on CC1/2 or SBU1/2 rises very rapidly during short-to-$48V_{BUS}$ events. When coupled with cable and trace inductance, the voltage typically overshoots 48V by many volts. If not controlled and isolated, these high voltages go well beyond the absolute maximum ratings of PD controllers and other circuits within the system. With the KTU1133, the high voltages are contained and isolated from the system.

To protect the system from short-to-VBUS, the KTU1133 includes four channels (for CC1, CC2, SBU1, and SBU2 data-lines) of high-voltage transient-voltage-suppression (TVS) shunt clamping to contain overshoot and four in-line (series-connected) isolation switches to isolate the system. The TVS and switches are designed to work together and provide $63V_{DC}$ tolerance with dynamic short-to-VBUS protection up to 48V + 15% = 55V. During short-to-$55V_{BUS}$ events, the KTU1133 turns off the switches very quickly in just 70ns to isolate the system from high voltage. The CC1_S and CC2_S system-side is contained to $5.9V_{DC}$ and $7V_{PEAK}$ transient during short-to-$55V_{BUS}$. The SBU1_S and SBU2_S system-side is contained to $4.2V_{DC}$ and $6.5V_{PEAK}$ transient during short-to-$55V_{BUS}$.

ESD Protection

The KTU1133's four channels of TVS provide IEC61000-4-2 level 4 ESD protection for the CC1/2 and SBU1/2 data-lines. Level 4 is defined as ±8kV contact and ±15kV air-gap ESD tolerance without damage. ESD events are generally caused by static electricity jumping from an end-user to the exposed contacts within the USB port.

Surge Protection

The KTU1133's four channels of TVS also provide IEC61000-4-5 surge protection. Surge events are generally caused by lightning strikes or cloud-to-cloud lightning coupling into the power grid, passing through the USB wall adapter and USB cable, and entering the system through the USB port. Other surge events include failure of grid equipment (such as a transformer failure) or sudden loading and inductive surges by other appliances on the local AC lines. Usually, most surge power enters the USB port via VBUS. However, some surge energy may enter from the CC and SBU lines, as well. The KTU1133 provides 90V surge tolerance on CC1/2 and 90V surge tolerance on SBU1/2.

Over-Voltage Protection (OVP)

If an OVP event occurs on any CC or SBU channel, the KTU1133 turns off all channels at once and pulls $\overline{\text{FLAG}}$ low to indicate there is a fault. After the OVP is removed, the channels recover and $\overline{\text{FLAG}}$ automatically returns to high-Z.

Over-Temperature Protection (OTP)

If the KTU1133 die junction temperature rises above the thermal shutdown threshold, the KTU1133 turns off all channels at once and pulls $\overline{FLAG}$ low to indicate there is a fault. Once the die temperature cools sufficiently, the channels recover and $\overline{FLAG}$ automatically returns to high-Z.

$\overline{FLT}$ Output Flag

The $\overline{FLT}$ pin indicates the fault status. The $\overline{FLT}$ open-drain output requires an external pull-up resistor with recommended value in the 1.7kΩ to 300kΩ range. During OVP and OTP fault conditions, the $\overline{FLT}$ flag is active low. When there is no fault, the $\overline{FLT}$ flag is high-Z and pulled up via the external resistor.

DP/DM (D+/D-) Protection

For systems that do not utilize the SBU1/2 data-lines, the SBU1/2 channels in the KTU1133 may be used to protect the DP/DM data-lines. The KTU1133's SBU bandwidth and channel-to-channel isolation support USB data rates up to 900Mbps.

VCONN Power

Once the CC channel is identified by the system's PD controller as either CC1 or CC2, the unused CCn channel becomes available as VCONN power to support USB active cables, dongles, port-expanders, and other VCONN-powered devices. To support any VCONN device, the KTU1133's CC1/2 switches are rated to pass up to 1.25A continuous current.

Dead Battery 5.1kΩ Pull-Down Option

For systems that contain a battery, the KTU1133 includes optional-use circuitry to wake the system in the event of a dead battery. Unlike USB type-A and type-B ports where 5V VBUS power is always present, the type-C port has VBUS turned off before a connection is established. Without VBUS power, the dead battery cannot be charged to wake the system. For this reason, a connection must first be established via a 5.1kΩ pull-down on both CC1 and CC2 to accommodate cable-flip, as the CC line may connect at either terminal in the port. Once the upstream AC wall-adapter or other USB current source sees the CC line 5.1kΩ pull-down from the KTU1133, the connection is established and VBUS is turned on to 5V, enabling the system to wake.

The PD controller includes 5.1kΩ pull-down resistors; however, the KTU1133 protection is inserted between the port and PD controller and is turned off due to lack of system power. Therefore, to enable the dead battery 5.1kΩ pull-down option in the KTU1133, connect the RPD_G1 and RPD_G2 pins to the CC1_C and CC2_C pins, respectively. The KTU1133 presents the 5.1kΩ pull-down to the port when:

1) KTU1133 is unpowered ($V_{CC} < V_{UVLO}$), and…
2) KTU1133 RPD_G1/2 pins are optionally tied to the CC1/2_C pins, and…
3) CC line in the USB cable is pulled up via a pull-up resistor or current source within the upstream AC wall-adapter or other USB current source.

Once a connection is established, VBUS is turned on, and the system can awake and charge its battery. Then, system power is restored and the KTU1133 receives power at its VCC pin. With power, the CC and SBU switches turn on, but the 5.1kΩ pull-downs remain active for an additional 5.7ms to give sufficient time for the PD controller to take over with its internal 5.1kΩ pull-downs. Without this important delay, a USB detach event may trigger, causing the upstream AC wall-adapter or other USB current source to turn off VBUS, disrupting system power. After 5.7ms, the KTU1133 pull-downs are disabled.

For applications that do not require the dead battery 5.1kΩ pull-downs in the KTU1133, connect the RPD_G1 and RPD_G2 pins to ground.

Extended Power Range (EPR) Adapter

Compared to other CC/SBU protection ICs that target USB standard power range (SPR) up to 20V, the KTU1133 is designed to support EPR systems up to 48V/5A/240W nominal. For this reason, the CC1/2_C and SBU1/2_C voltage tolerances have been raised above 48V to survive short-to-VBUS fault events. Additionally, the KTU1133's TVS maximum working voltage, breakdown voltage, and clamping voltage are raised above 48V.

Furthermore, the KTU1133 includes two additional circuits to enable the use of a 20V SPR PD controller in a 48V EPR system. These two circuits are the *VBUS Level Shifter* and the *EPR Blocking FET Gate Driver*, as described below. The two circuits are enabled for EPR Mode via the EPR_EN active-high logic input **or** whenever the VBUS pin rises over $24V_{MAX}$. The KTU1133 returns to SPR Mode whenever the EPR_EN input is logic 0 **and** VBUS falls below $22V_{MIN}$.

VBUS Level Shifter

The VBUS level shifter provides a lower-voltage version of VBUS during EPR Mode so an SPR-rated PD controller can safely monitor the VBUS voltage. In EPR Mode, the VBUS_LV output is proportionally scaled to 0.42x VBUS. Therefore, 48V at the VBUS input is shifted to 20V at VBUS_LV output. In SPR Mode, the VBUS level shifter enters 1x VBUS "pass through" operation.

EPR Blocking FET Gate Driver

The EPR blocking FET gate driver controls an external n-channel MOSFET. In SPR Mode, the MOSFET is turned ON so that the PD controller can source VBUS to the USB port to power other devices within the SPR range from 5V*0.5A=2.5W up to 20V*5A=100W (as well as the full USB PPS range), depending upon the system capabilities. In EPR Mode, the MOSFET is turned OFF to block high EPR VBUS voltages that would otherwise damage the SPR-rated PD controller. Instead, the PD controller can safely monitor the voltage via the 0.42x VBUS level shifter output at VBUS_LV.

EPR-Rated UFP/DFP/DRP with KTU1133 + KTS1800 + 20V SPR PD Controller

The KTU1133 enables 20V SPR-rated PD controllers to be used in USB 36V/48V EPR upstream facing power ports (UFP), downstream facing power ports (DFP), and dual-role power ports (DRP). However, additional EPR-rated VBUS OVP load switches, such as the KTS1800, are required to safely route the EPR VBUS sink and/or source power within the system. The KTS1800 can operate as a current sink or current source switch. It integrates a plethora of fast protection features, including an integrated high-voltage transient voltage suppressor (TVS) for IEC surge and ESD protection. The active TVS in the KTS1800 also provides superior protection for the VBUS pin of the KTU1133, as they are designed to work together.

Functional Tables

Table 1. EPR/SPR Mode Control

	Inputs		Outputs	
Mode	**EPR_EN**	**VBUS**	**VBUS_LV**	**GATE**
SPR Mode	0	$V_{BUS} < V_{EPR\_VBUS}$	$V_{BUS\_LV} = 1x\ V_{BUS}$	Enabled (FET On)
EPR Mode	1	X	$V_{BUS\_LV} = 0.42x\ V_{BUS}$	Disabled (FET Off)
EPR Mode	X	$V_{BUS} > V_{EPR\_VBUS}$	$V_{BUS\_LV} = 0.42x\ V_{BUS}$	Disabled (FET Off)

Table 2. Device Operating State

	Inputs					Outputs					
Mode	**VCC**	**CCn_C**	**SBUn_C**	**RPD_Gn**	**T_J**	**$\overline{FLT}$**	**CCn_S**	**SBUn_S**	**VBUS_LV**	**GATE**	**5.1kΩ**
No Dead Battery Support	$<V_{UVLO}$	X	X	Connect to GND	X	high-Z	Off	Off	$1x\ V_{BUS}$	Disable	Off
Dead Battery Support	$<V_{UVLO}$	$>V_{DB}$	X	Connect to CCn_C	X	high-Z	Off	Off	$1x\ V_{BUS}$	Disable	On
SPR Mode	$>V_{UVLO}$	$<V_{OVP\_CC}$	$<V_{OVP\_SBU}$	X	$<T_{OTP}$	high-Z	On	On	$1x\ V_{BUS}$	Enable	Off
EPR Mode	$>V_{UVLO}$	$<V_{OVP\_CC}$	$<V_{OVP\_SBU}$	X	$<T_{OTP}$	high-Z	On	On	$0.42x\ V_{BUS}$	Disable	Off
OTP Fault	$>V_{UVLO}$	X	X	X	$>T_{OTP}$	0	Off	Off	Maintain State	Maintain State	Off
CC OVP Fault	$>V_{UVLO}$	$>V_{OVP\_CC}$	X	X	$<T_{OTP}$	0	Off	Off	Maintain State	Maintain State	Off
SBU OVP Fault	$>V_{UVLO}$	X	$>V_{OVP\_SBU}$	X	$<T_{OTP}$	0	Off	Off	Maintain State	Maintain State	Off

Applications Information

VCC Bypass Capacitor Selection

Place a 1.0µF/6.3V (or higher) ceramic capacitor between the VCC pin and ground. X5R or X7R dielectric ceramic capacitors are preferred for input supply bypass applications as they maintain better capacitance value and tolerance over operating voltage and temperature ranges when compared to lower cost Y5V dielectric type ceramic capacitors.

ESD Capacitor Selection

KTU1133 utilizes an ESD support capacitor to meet ESD protection requirements. The ESD support capacitor should be placed between the CESD pin and ground. The CC1/2_C and SBU1/2_C inputs can have as much as 65V applied during a short-to-VBUS event with overshoot and the KTU1133's TVS clamping. Therefore, a 0.1µF/100V X5R or X7R dielectric ceramic capacitor is recommended for this application.

VBUS Capacitor Selection

Although the KTU1133 does not require much capacitance on VBUS, most USB applications connect a 1µF to 10µF ceramic capacitor from VBUS to GND. Per USB specifications, a maximum of 10µF total is allowed on the VBUS port/connector node. 100V rated capacitors with X5R or better dielectric are recommended for EPR applications. If using the KTU1133 and KTS1800 together, they can share the same VBUS capacitor. For optimal surge and ESD performance with the KTS1800, 10µF is preferred.

Recommended PCB Layout

Place the bypass capacitors as close as possible to the VCC pin, and ESD protection capacitor as close as possible to the CESD pin. Capacitors must be attached to a solid ground. This minimizes voltage disturbances during transient events such as short-to-VBUS and ESD strikes.

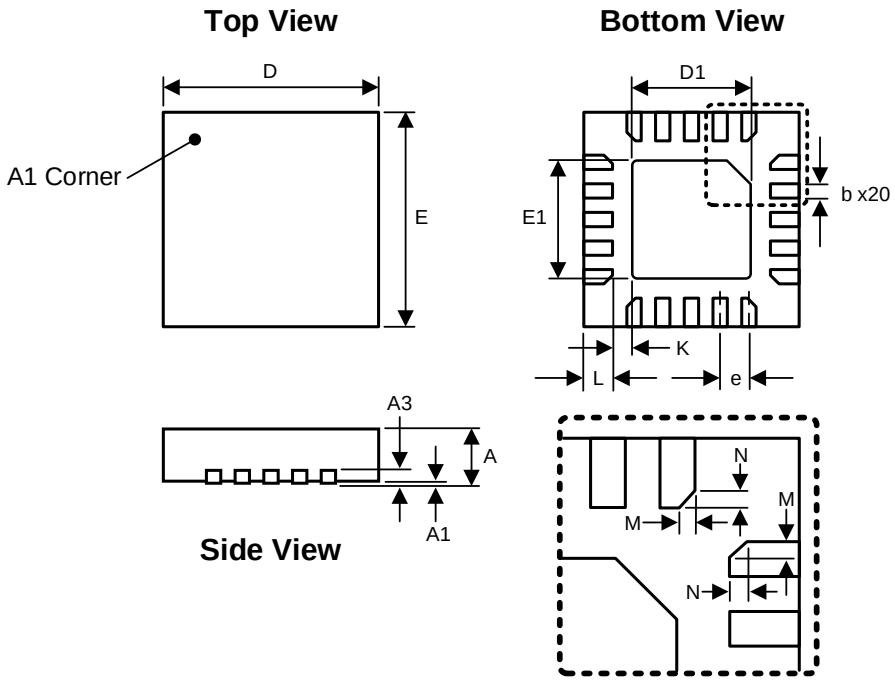
The SBU lines must be routed as straight as possible, and any sharp bends must be minimized. Eliminate any sharp corners on the SBU1_C, SBU2_C, SBU1_S, and SBU2_S traces by using rounded corners with the largest radii possible.

Standard ESD recommendations apply to the CC1_C, CC2_C, SBU1_C, and SBU2_C. Route these protected traces as straight as possible. The optimum placement for the device is as close to the connector as possible. EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures. The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the KTU1133 and the connector.

For the VBUS connection of the KTU1133, the trace should first route from the VBUS terminal of the connector directly to a VBUS capacitor and an appropriate TVS (such as the one integrated within the KTS1800), and then to the KTU1133.

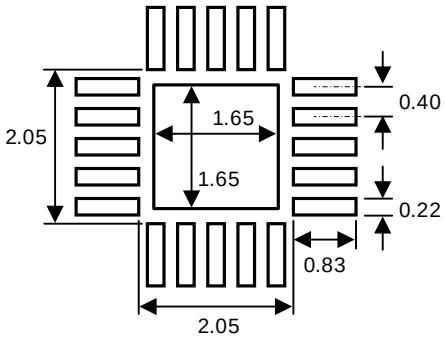
Packaging Information

WQFN33-20 (3.00mm x 3.00mm x 0.75mm)



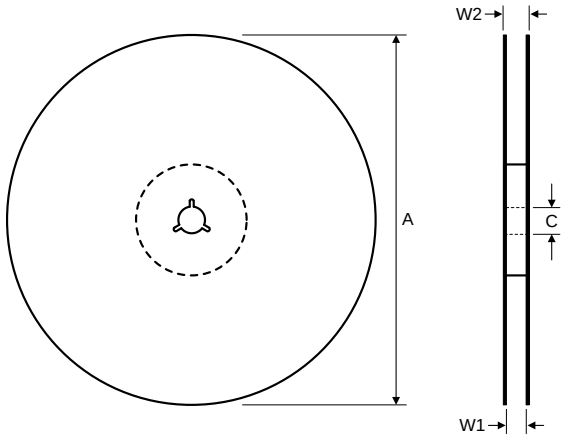
Dimension	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.15	0.20	0.25
D	2.90	3.00	3.10
D1	1.60	1.65	1.70
E	2.90	3.00	3.10
E1	1.60	1.65	1.70
e	0.40 BSC		
K	0.20	–	–
L	0.30	0.40	0.50
M	–	0.10	–
N	–	0.10	–

Recommended Footprint



Packing Material Information

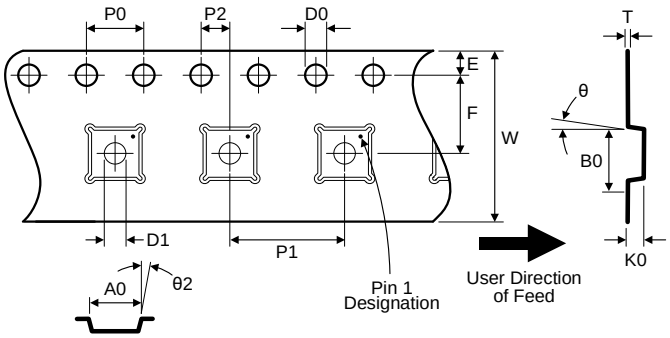
Reel Dimensions



Dimension	mm		
	Min.	Typ.	Max.
A	328	330	332
C	12.8	13.0	13.5
W1	12.4	12.8	14.4
W2	—	—	18.4

43-00003-021

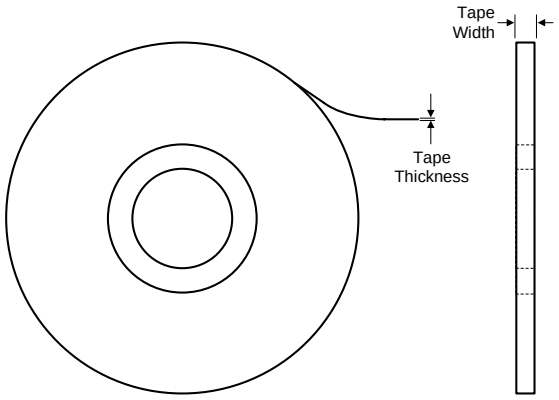
Carrier Tape Dimensions



Dimension	mm		
	Min.	Typ.	Max.
A0	—	3.30	—
B0	—	3.30	—
K0	—	1.10	—
P0	3.98	4.00	4.02
P1	—	8.00	—
P2	1.95	2.00	2.05
D0	1.50	1.50	1.60
D1	1.50	—	—
E	1.65	1.75	1.85
F	5.45	5.50	5.55
10P0	39.8	40.0	40.2
W	11.70	12.00	12.30
T	0.25	0.30	0.35
Θ	0°		5°
Θ2	0°		5°
Quantity	5000 each		

43-010X2-306

Cover Tape Dimensions



Dimensions	Dimension	mm		
		Min.	Typ.	Max.
	Tape Thickness	0.047	0.052	0.057
12mm	Tape Width	9.2	9.3	9.4

43-00002-061