6.5A VBUS Bi-Directional Safety Switch for USB SPR

Features

- Bi-Directional Switch for USB I_{SINK}, I_{SOURCE}, or DRP
- 3V to 23V Operating Voltage Range
  - $29V_{DC}$ Abs. Max. Rating at VBUS & VSYS
- $6.5A_{RMS}$ Current Rating in I_{SINK} Mode
- $5.0A_{RMS}$ Current Rating in I_{SOURCE} Mode
- 20mΩ typ. On-Resistance
- Transient Voltage Suppression (TVS) at VBUS
  - ±100V Surge Protection (IEC61000-4-5)
  - ±30kV ESD Contact & Air-Gap (IEC61000-4-2)
- Soft-Start (SS) Limits In-Rush Current
  - Fast SS for USB Fast Role Swap (FRS)
- Over-Voltage Protection (OVP)
- "Ideal Diode" Reverse Current Protection (RCP)
- Short-Circuit Protection (SCP) at VBUS & VSYS
- Over-Current Protection (OCP) in I_{SINK} Mode
- Current-Limit Protection (CLP) in I_{SOURCE} Mode
- Over-Temperature Protection (OTP)
- POK Safe LDO provides 3.3V/100mA
- $\overline{FLT}$ Open-Drain Output Flag
- Auto-Retry Hiccup Operation after Faults
- Active Discharge for VBUS
- Safety approvals for I_{SOURCE} Mode
  - UL 2367, File No. E515099
  - IEC 62368-1, File No. E515099
- -40°C to 85°C Operating Temperature Range
- 20-bump WLCSP 2.71 x 2.16mm (0.5mm pitch)

Brief Description

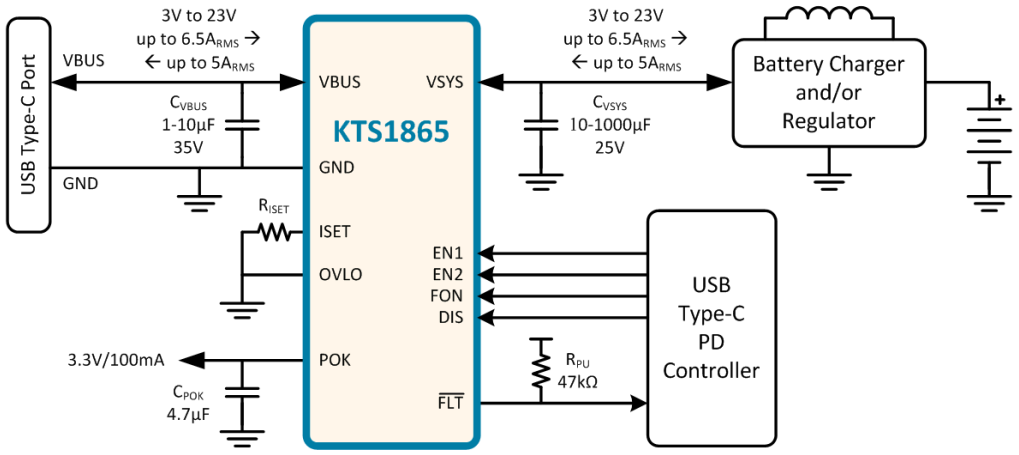
The KTS1865 is a low-resistance, high-current load switch optimized to protect USB Standard Power Range (SPR) Type-C ports that sink up to 130W at 20V and/or source up to 100W at 20V. The protection features include soft-start, over-voltage protection, "ideal diode" reverse-current protection with fast recovery, short-circuit protection, over-current protection, programmable current limit protection, over-temperature protection, and integrated TVS for IEC surge and ESD protection. Other features include a POK Safe LDO, $\overline{FLT}$ open-drain output flag, fast soft-start mode for USB fast role swap, and active discharge for VBUS. The EN1 and EN2 logic inputs enable/disable the switch and set the I_{SINK} vs. I_{SOURCE} operating mode.

The KTS1865 is packaged in advanced, fully "green" compliant, 2.71 x 2.16mm, 20-bump Wafer-Level Chip-Scale Package (WLCSP).

Applications

- Desktop PC, Notebooks, Netbooks, Tablets
- Docking Stations, Monitors, POS Terminals
- Battery/Solar Generators, Conferencing Systems
- Charger-per-Port Systems, Power Banks

Typical Application



Ordering Information

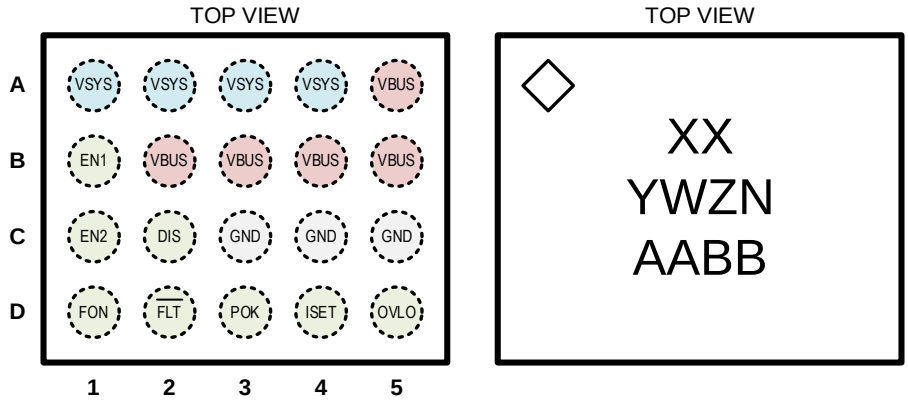
Part Number	Marking[1]	EN1/EN2 Options (see Table 1)	Operating Temperature	Package
KTS1865AEIAA-TA	QQYWZNAABB	Default Setting	-40°C to +85°C	WLCSP-20
KTS1865BEIAA-TA[2]	UCYWZNAABB	Alternative 1	-40°C to +85°C	WLCSP-20
KTS1865CEIAA-TA	UDYWZNAABB	Alternative 2	-40°C to +85°C	WLCSP-20

EN1	EN2	KTS1865A	KTS1865B	KTS1865C
0	0	Switch Off + POK LDO On	Switch Off + POK LDO On	I_{SINK} Mode + POK LDO On
0	1	I_{SINK} Mode + POK LDO On	Shutdown	I_{SOURCE} Mode + POK LDO On
1	0	I_{SOURCE} Mode + POK LDO On	I_{SINK} Mode + POK LDO On	Switch Off + POK LDO On
1	1	Shutdown	I_{SOURCE} Mode + POK LDO On	Shutdown

Table 1. EN1/EN2 Mode-Control Options[3]

Pinout Diagram

WLCSP54-20



20-bump 2.71mm x 2.16mm x 0.555mm
WLCSP Package, 0.5mm pitch

Top Mark

XX = Device ID, YW = Date Code, ZN = Assembly Code, AABB = Serial Number

1. QQ = Device ID for the KTS1865A, UC = Device ID for the KTS1865B, UD = Device ID for the KTS1865C, YW = Date Code, ZN = Assembly Code and AABB = Serial Number.
2. Contact a Kinetic Technologies authorized representative for availability.
3. Besides EN1 and EN2, the UVLO and Fault conditions affect the On/Off status of the Switch and POK LDO. Note that the POK LDO is powered from VBUS, so it is Off when $V_{BUS} < V_{UVLO}$. See the *Typical Characteristics* section for multiple oscilloscope images showing the behavior.

Pin Descriptions

Pin #	Name	Function
A1, A2, A3, A4	VSYS	Power Switch System-Side Connection – connect to system internal power rail.
A5, B2, B3, B4, B5	VBUS	Power Switch Port-Side Connection – connect to VBUS on USB power port.
C3, C4, C5	GND	Ground
B1	EN1	Enable 1 Logic Input – with EN2, controls operating modes; see Table 1.
C1	EN2	Enable 2 Logic Input – with EN1, controls operating modes; see Table 1.
C2	DIS	V_{BUS} Active Discharge Input – active-high analog input to gate of V_{BUS} active discharge FET with internal 600kΩ pull down.
D1	FON	Fast Turn-On Logic Input – active-high with internal 1MΩ pull down; enables fast turn-on for USB Fast Role Swap (FRS).
D2	$\overline{FLT}$	Fault Logic Output – active-low, open-drain flag indicates any fault condition(s). $\overline{FLT}$ is held active-low during soft-start and auto-retry.
D3	POK	Power-OK “Safe LDO” Regulator Output – regulated output voltage when $V_{BUS} > V_{UVLO}$ and LDO is enabled via EN1 and EN2; see Table 1.
D4	ISET	Current Limit Setting – adjusts the I_{SOURCE} mode current limit with a resistor from ISET to GND.
D5	OVLO	Over-Voltage Lockout Adjustment – connect to GND to use the internally-fixed OVP threshold. Connect an external resistive voltage divider from VBUS (or VSYS) to OVLO to GND to set an adjustable OVLO threshold.

Absolute Maximum Ratings[4]

Symbol	Description	Value	Units
V_{BUS}	VBUS to GND (continuous) VBUS to GND (during IEC61000-4-5 surge event)	-0.3 to 29 -5 to 36	V
V_{SYS}	VSYS to GND	-0.3 to 29	V
$V_{BUS-SYS}$	VBUS to VSYS	-29 to 29	V
V_{OVLO}	OVLO to GND	-0.3 to V_{BUS}	V
V_{EN1}, V_{EN2}, V_{ISET}, V_{DIS}, V_{POK}, V_{FON}, $V_{\overline{FLT}}$	EN1, EN2, ISET, DIS, POK, FON, $\overline{FLT}$ to GND	-0.3 to 6	V
I_{SW}	Maximum Switch Current (continuous) Peak Switch Current (2ms, OCP and OTP Pd limited)	8 17	A
T_J	Die Junction Operating Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-55 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

ESD and Surge Ratings[5]

Symbol	Description	Value	Units
V_{ESD}	JEDEC JS-001-2017 Human Body Model (all pins) IEC61000-4-2 Contact Discharge (VBUS) IEC61000-4-2 Air Gap Discharge (VBUS)	±2 ±30 ±30	kV
V_{SURGE}	IEC61000-4-5 Surge (VBUS, C_{VBUS} = 10µF, V_{BUS} = 0V to 23V pre-bias)	±100	V

Thermal Capabilities[6]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	60	°C/W
P_D	Maximum Power Dissipation at $T_A \leq 25°C$ ($T_J \leq 150°C$)	2.08	W
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	-16.7	mW/°C

4. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

5. ESD and Surge Ratings conform to JEDEC and IEC industry standards. Some pins may have higher performance. Surge ratings apply with chip enabled, disabled, or unpowered, unless otherwise noted.

6. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.

Recommended Operating Conditions[7]

Symbol	Description	Value	Units
V_{BUS}, V_{SYS}	VBUS, VSYS Operating Voltage	3 to 23	V
V_{IO}	EN1, EN2, FON, DIS, $\overline{FLT}$ Voltage	0 to 5.5	V
I_{SINK}	VBUS to VSYS Current	0 to 6.5	A
I_{SOURCE}	VSYS to VBUS Current	0 to 5.0	A
C_{VBUS}	VBUS External Local Capacitance (nominal)	1 to 10 35 or 50	µF V
C_{VSYS}	VSYS External Capacitance (nominal)	10 to 1000 25	µF V
T_A	Ambient Operating Temperature	-40 to 85	°C

Electrical Characteristics[8]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_A = -40°C to +85°C with V_{BUS} = 3V to 23V or V_{SYS} = 3V to 23V. Typical values are specified at T_A = +25°C with V_{BUS} = 5V or V_{SYS} = 5V.

Supply Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{TVS}[9]	TVS Working Voltage at VBUS		-0.3		29	V
	TVS Clamping Voltage at VBUS	I_{BUS} = 10mA I_{BUS} = -10mA	30 -2	32.5 -0.6	35 -0.3	
V_{BUS}	VBUS Supply Operating Voltage Range	I_{SINK} mode	3		23	V
V_{SYS}	VSYS Supply Operating Voltage Range	I_{SOURCE} mode	3		23	V
V_{UVLO}	Under-Voltage Lockout	V_{BUS} rising threshold, I_{SINK} mode V_{SYS} rising threshold, I_{SOURCE} mode Hysteresis, I_{SINK} or I_{SOURCE} mode		2.7 2.7 200	2.9 2.9	V V mV
I_Q	No-Load Supply Current	V_{BUS} = 5V, I_{SINK} mode V_{BUS} = 20V, I_{SINK} mode V_{SYS} = 5V, I_{SOURCE} mode V_{SYS} = 20V, I_{SOURCE} mode		350 450 350 450		µA
I_{Q_POK}	No-Load POK LDO Supply Current	V_{BUS} = 5V, Switch Off, POK On V_{BUS} = 20V, Switch Off, POK On		110 170		µA
I_{SHDN}	Shutdown Supply Current	V_{BUS} = 5V, shutdown mode V_{BUS} = 20V, shutdown mode V_{SYS} = 5V, shutdown mode V_{SYS} = 20V, shutdown mode		1.9 4.0 1.9 4.0		µA
I_{Q_RCP}	Output Supply Current in RCP	V_{BUS} = 0V, V_{SYS} = 5V, I_{SINK} mode V_{SYS} = 0V, V_{BUS} = 5V, I_{SOURCE} mode		420 450		µA

(continued next page)

7. The recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Kinetic does not recommend exceeding them or designing to Absolute Maximum Rating.

8. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

9. V_{TVS} is guaranteed by design and characterization; not production tested.

Electrical Characteristics (continued)[10]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_A = -40°C to +85°C with V_{BUS} = 3V to 23V or V_{SYS} = 3V to 23V. Typical values are specified at T_A = +25°C with V_{BUS} = 5V or V_{SYS} = 5V.

Logic Pin (EN1, EN2, FON, $\overline{FLT}$) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input Logic High (EN1, EN2, FON)		1.2			V
V_{IL}	Input Logic Low (EN1, EN2, FON)				0.4	V
R_{I_PD}	Input Logic Pull-Down (FON)			1		MΩ
I_{I_LK}	Input Logic Leakage (EN1, EN2)	V_I = 5V	-1		1	µA
V_{OL}	Output Logic Low ($\overline{FLT}$) [11]	I_{O_SINK} = 1mA		0.01	0.2	V
I_{O_LK}	Output Logic High-Z Leakage ($\overline{FLT}$) [12]	V_O = 5V	-1		1	µA

V_{BUS} Active Discharge (DIS) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{AD}	Active Discharge Resistance (from V_{BUS}=5V to GND)	V_{DIS} = 3V V_{DIS} = 2V V_{DIS} = 1.5V V_{DIS} = 1.4V V_{DIS} = 1.2V, T_A = 0°C to +85°C		0.22 0.57 1.4 1.8 3.4	 5.0	kΩ
V_{IH_DIS}	DIS Input High Voltage	R_{AD} < 5kΩ, T_A = 0°C to +85°C	1.2			V
V_{IL_DIS}	DIS Input Low Voltage[13]	R_{AD} is high-Z			0.5	V
R_{DIS_PD}	DIS Internal Pull-Down Resistor	V_{DIS} = V_{SYS} = 5V, I_{SOURCE} mode		600		kΩ
t_{VBUS_DIS}	V_{BUS} Active Discharge Time[14]	V_{BUS} = 5V, V_{DIS} = 3V, C_{VBUS} = 1µF		600		µs

POK Safe LDO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{POK}	POK LDO Output Voltage	V_{BUS} = 5V to 20V, I_{POK} = 0 to 100mA, T_A = +25°C	3.0	3.3	3.6	V
V_{UVLO_POK}	POK LDO Under-Voltage Lockout[15]	V_{BUS} rising threshold, POK On Hysteresis		2.7 150	2.9	V mV
I_{Q_POK}	No-Load POK LDO Supply Current	V_{BUS} = 5V, Switch Off, POK On V_{BUS} = 20V, Switch Off, POK On		110 170		µA
I_{LK_POK}	POK-to-GND Leakage Current	V_{POK} = 5V, V_{BUS} = 0V, T_A = +25°C		0.01	1	µA
I_{POK_VBUS}	POK-to-VBUS Leakage Current at VBUS	V_{POK} = 5V, V_{BUS} = 0V, dark		-0.001		µA

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10. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.
11. V_{OL} is guaranteed by design and characterization; not production tested.
12. I_{O_LK} is guaranteed by design and characterization; not production tested.
13. V_{IL_DIS} is guaranteed by design and characterization; not production tested.
14. t_{VBUS_DIS} is the time for V_{BUS} to fall from 5V (vSafe5V) to below 0.8V (vSafe0V). The USB specification for tSafe0V is 0ms to 650ms, so in theory, this can discharge up to 1000µF in case of excessive source bulk capacitance.
15. POK Safe LDO is enabled when V_{BUS} is above V_{UVLO_POK}, depending upon EN1 and EN2 status, regardless of OVP, OVLO, and OCP.

Electrical Characteristics (continued)[16]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_A = -40°C to +85°C with V_{BUS} = 3V to 23V or V_{SYS} = 3V to 23V. Typical values are specified at T_A = +25°C with V_{BUS} = 5V or V_{SYS} = 5V.

Power Switch Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{ON}	Switch On-Resistance in I_{SINK} mode	V_{BUS} = 5V, I_{SYS} = 1.0A[17] V_{BUS} = 5V, I_{SYS} = 1.5A V_{BUS} = 20V, I_{SYS} = 1.5A, T_A = +25°C		22 20 20	 30	mΩ
	Switch On-Resistance in I_{SOURCE} mode	V_{SYS} = 5V, I_{BUS} = 1.0A[17] V_{SYS} = 5V, I_{BUS} = 1.5A V_{SYS} = 20V, I_{BUS} = 1.5A, T_A = +25°C		22 20 20	 30	
I_{BUS_OFF}	Switch Off-Leakage at VBUS (tested in shutdown mode)	V_{BUS} = 5V, V_{SYS} = 0V V_{BUS} = 20V, V_{SYS} = 0V V_{BUS} = 29V, V_{SYS} = 0V V_{BUS} = 0V, V_{SYS} = 3V to 23V, dark		1.9 4.0 5.0 -0.001	 10 	µA
I_{SYS_OFF}	Switch Off-Leakage at VSYS[18] (tested in shutdown mode)	V_{SYS} = 5V, V_{BUS} = 0V V_{SYS} = 20V, V_{BUS} = 0V V_{SYS} = 29V, V_{BUS} = 0V V_{SYS} = 0V, V_{BUS} = 3V to 23V, dark		1.9 4.0 5.0 -0.001	 10 	µA

Soft-Start (SS) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{DEB}	Soft-Start Debounce Time[19]	I_{SINK} or I_{SOURCE}, FON = 0 I_{SINK} or I_{SOURCE}, FON = 1	10	16 0	25	ms
t_R	Soft-Start Rising Slew-Rate Ramp Time[20]	I_{SINK} or I_{SOURCE}, FON = 0 I_{SINK} or I_{SOURCE}, FON = 1	1	3 0.05	5 0.1	ms
I_{LIM_SS}	Soft-Start Current Limit	I_{SINK}, V_{BUS} = 5V, FON = 0 I_{SINK}, V_{BUS} = 20V, FON = 0 I_{SOURCE}, V_{SYS} = 5V, FON = 0 I_{SINK} or I_{SOURCE}, FON = 1		2 1 I_{CLP_FB} n/a		A
t_{LIM_SS}	Soft-Start Current Limit Done Time	I_{SINK} or I_{SOURCE}, FON = 0 I_{SINK} or I_{SOURCE}, FON = 1		7 0.115		ms
t_{DOFF}	Turn-Off Delay Time[21]		0	10	30	µs

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16. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.
17. When tested less than 1A, the R_{ON} is limited by the V_{RCP} specification.
18. I_{SYS_OFF}, V_{IL_DIS} are guaranteed by design and characterization; not production tested.
19. t_{DEB} is time from enabled logic and valid supply voltage until the output voltage begins to rise.
20. t_R is time from the output voltage reaches 10% until the output voltage reaches 90% of the input voltage. t_R is guaranteed by design and characterization; not production tested.
21. t_{DOFF} is time from enable logic until the output voltage begins to fall.

Electrical Characteristics (continued)[22]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_A = -40°C to +85°C with V_{BUS} = 3V to 23V or V_{SYS} = 3V to 23V. Typical values are specified at T_A = +25°C with V_{BUS} = 5V or V_{SYS} = 5V.

Fault Flag ($\overline{FLT}$) Recovery and Hiccup Timer Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{HICCUP}	Fault Condition Hiccup Retry Time[23]	after failed fault recoveries		64		ms
$t_{\overline{FLT}}$	Fault Flag Release Delay after t_{LIM_SS}	after t_{LIM_SS}, FON = 0 after t_{LIM_SS}, FON = 1		3 0		ms

Over-Voltage Protection (OVP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OVP}	Internally Fixed Over-Voltage Protection	V_{BUS} rising threshold, I_{SINK} mode V_{SYS} rising threshold, I_{SOURCE} mode Hysteresis	22 22	23 23 300	25 25	V V mV
t_{OVP}	OVP Response Time[24]	V_{BUS} > V_{OVP}, C_{VSYS} = 0µF, R_L = 100Ω V_{SYS} > V_{OVP}, C_{VBUS} = 0µF, R_L = 100Ω		90 90		ns
V_{OVLO}	Externally Adjustable Over-Voltage Lockout	V_{OVLO} enable threshold V_{OVLO} rising OVP threshold Hysteresis	0.2 1.10	0.25 1.227 25	0.3 1.34	V V mV
t_{OVLO}	OVLO Response Time[25]	R_L = 100Ω, C_{VSYS} = 0µF		300		ns

Over-Temperature Protection (OTP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{OTP}	IC Junction Over-Temperature Protection	T_J rising threshold Hysteresis		150 20		°C

Over-Current Protection (OCP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{OCP}	OCP Current Threshold after t_{LIM_SS}[26]	I_{SINK} mode I_{SOURCE} mode	10 10	17 17		A
t_{OCP}	OCP Response Time[27]			200		ns

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22. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

23. Faults include OVP, OTP, OCP, and SCP. After the fault condition has ended, auto-retry follows the soft-start sequence. If auto-retry fails the first time, then the hiccup timer increases the delay before each subsequent soft-start retry. The $\overline{FLT}$ flag is released only after a successful retry. Other protections that are not classified as faults include RCP and CLP. These non-faults do not trigger the $\overline{FLT}$ flag and hiccup timer. RCP and CLP have fast recovery without initiating a soft-start. UVLO does trigger the $\overline{FLT}$ flag and soft-start, but without the hiccup timer.

24. t_{OVP} is time from when the input voltage > V_{OVP} until the output voltage stops rising.

25. t_{OVLO} is time from when V_{OVLO} rises above its OVP threshold until output voltage stops rising.

26. I_{OCP} is guaranteed by design and characterization; not production tested.

27. t_{OCP} is time from when the switch current > I_{OCP} until switch turns off.

Electrical Characteristics (continued)[28]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_A = -40°C to +85°C with V_{BUS} = 3V to 23V or V_{SYS} = 3V to 23V. Typical values are specified at T_A = +25°C with V_{BUS} = 5V or V_{SYS} = 5V.

Reverse-Current Protection (RCP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{RCP}	RCP Droop Regulation Voltage	I_{SINK}, $V_{RCP}=V_{BUS}–V_{SYS}$, I_{SYS}=100mA I_{SOURCE}, $V_{RCP}=V_{SYS}–V_{BUS}$, I_{BUS}=100mA	5 5	15 15	30 30	mV
t_{RCP_REC}	RCP Fast Recovery Time[29]			15		µs

Current Limit Protection (CLP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{CLP_LIM}	Current Limit Regulation (after t_{LIM_SS})[30]	I_{SINK} mode		n/a		A
		I_{SOURCE} mode, R_{ISET} = 83k	0.5	0.6	0.7	
		I_{SOURCE} mode, R_{ISET} = 51k	0.90	1.00	1.10	
		I_{SOURCE} mode, R_{ISET} = 30k	1.5	1.7	1.9	
		I_{SOURCE} mode, R_{ISET} = 15k	3.1	3.4	3.7	
		I_{SOURCE} mode, R_{ISET} = 11.1k	4.2	4.6	5.0	
		I_{SOURCE} mode, R_{ISET} = 9.1k	5.1	5.6	6.1	
I_{CLP_TRANS}	Current Limit Threshold for CLP-to-Foldback Transition	I_{SOURCE} mode		1.1*I_{CLP_LIM}		A
I_{CLP_FB}	Current Limit Regulation in Foldback (after t_{LIM_SS})	I_{SOURCE} mode		0.8*I_{CLP_LIM}		A

Short Circuit Protection (SCP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{HSCP_SS}	Hard Short-Circuit Protection SS Voltage (at 2.7ms into soft-start ramp)	I_{SINK} mode, V_{SYS} not rising		0.1*V_{BUS}		V
		I_{SOURCE} mode, V_{BUS} not rising		0.1*V_{SYS}		
V_{SSCP}	Soft Short-Circuit Protection Voltage (after soft-start t_{LIM_SS})	I_{SINK} mode, V_{SYS} falling		0.6*V_{BUS}		V
		I_{SOURCE} mode, V_{BUS} falling		0.6*V_{SYS}		
t_{SSCP_DEB}	Soft Short-Circuit Protection Debounce Timer			64		µs

28. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

29. t_{RCP_REC} is time from when the output voltage falls 50mV below the input voltage until switch turns back on. Before measuring, first raise the output voltage significantly above the input voltage.

30. I_{CLP_LIM} is guaranteed by design and characterization; not production tested.

Timing Diagrams

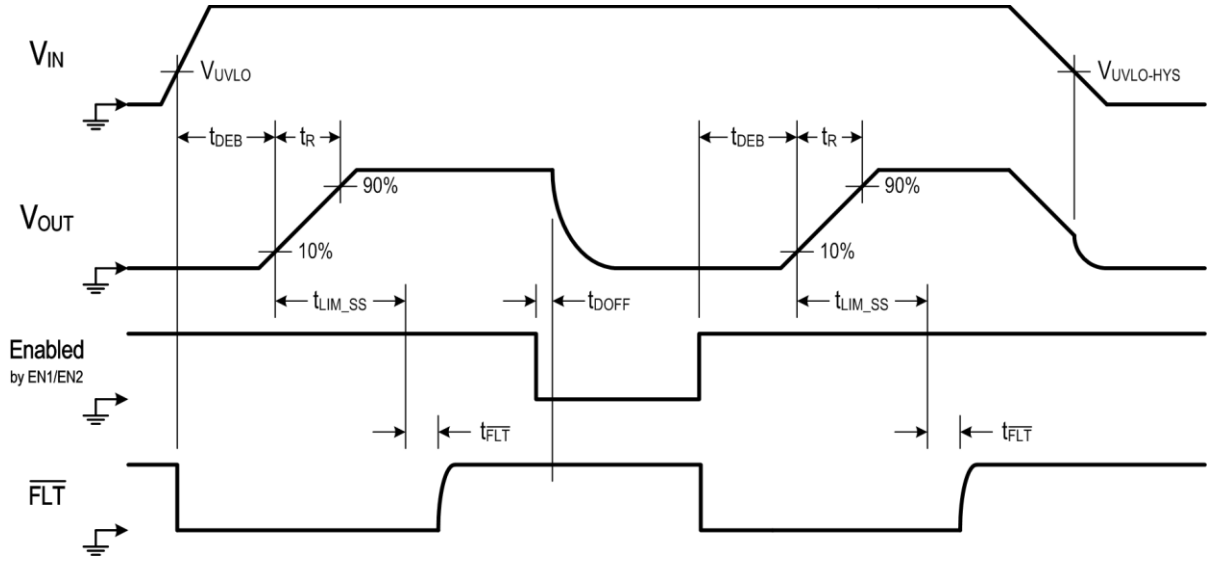


Figure 1. UVLO, Soft-Start and Turn-Off Timing Diagram

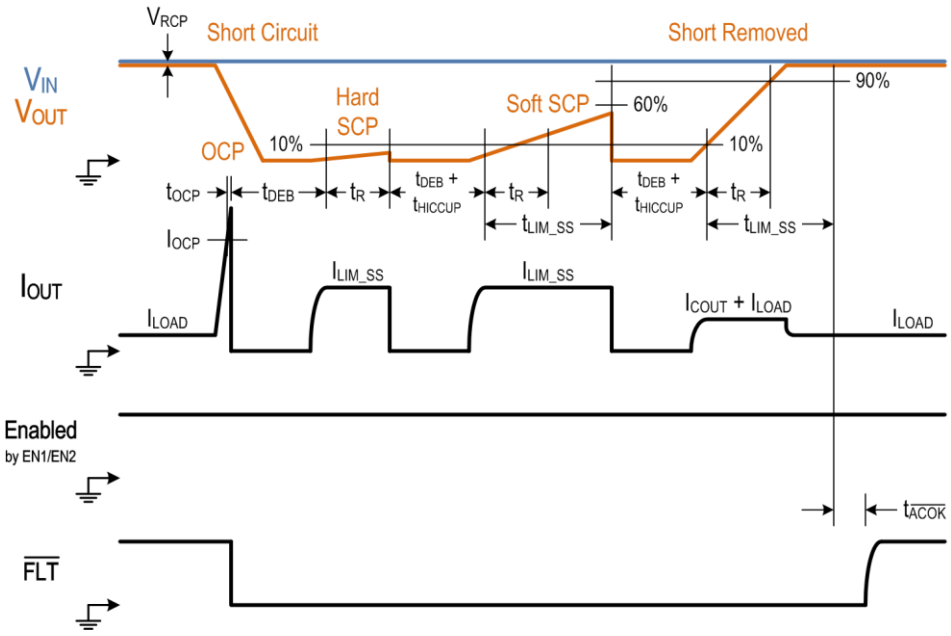


Figure 2. OCP, Hard SCP, Soft SCP, Auto-Retry and Hiccup Timing Diagram

Timing Diagrams (continued)

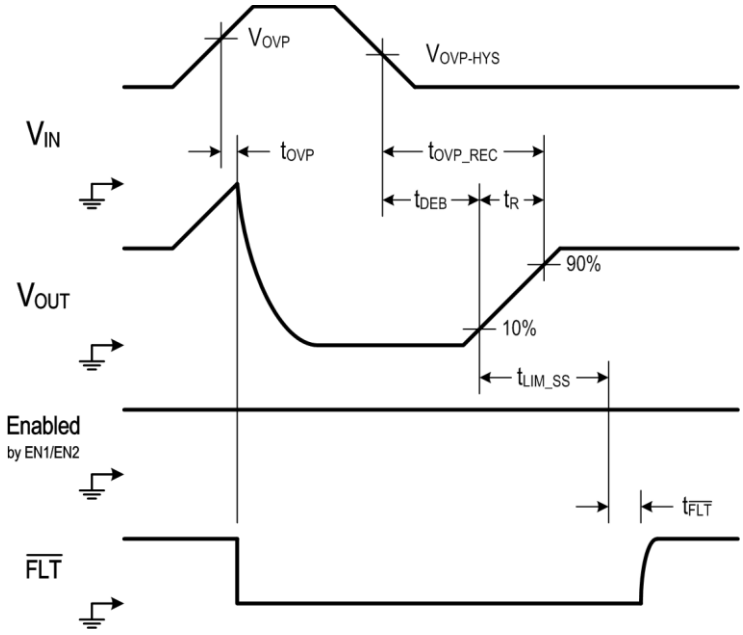


Figure 3. OVP Timing Diagram

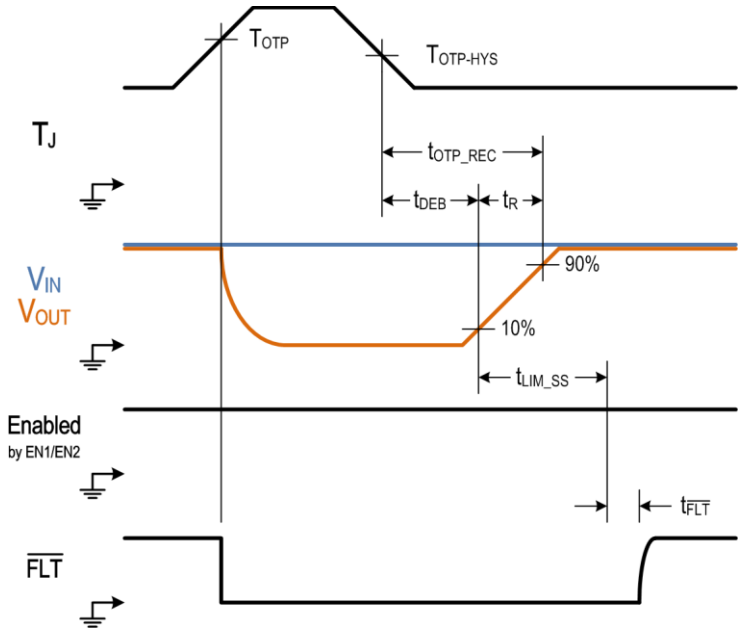
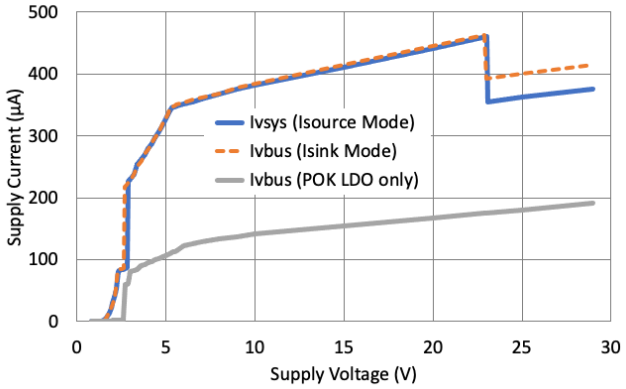


Figure 4. OTP Timing Diagram

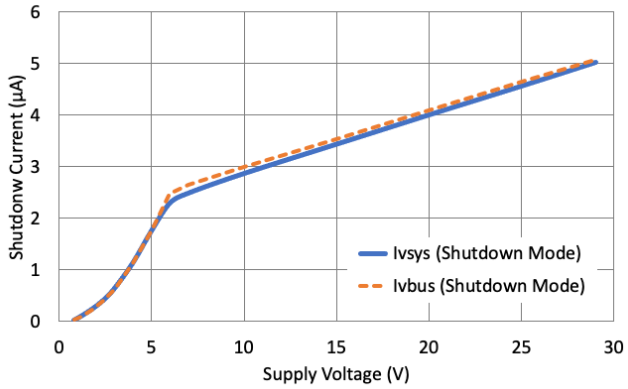
Typical Characteristics

C_{VSYS} = 2x 22µF, C_{VBUS} = 10µF, C_{POK} = 4.7µF, FON = 0, R_{ISET} = 14.7kΩ, T_A = 25°C, unless otherwise specified.

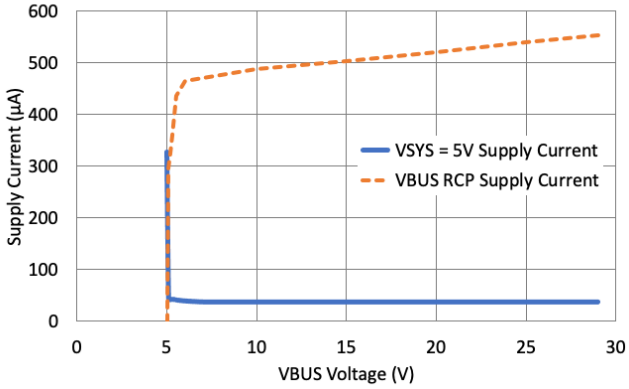
Supply Current vs. Supply Voltage
(enabled, no load)



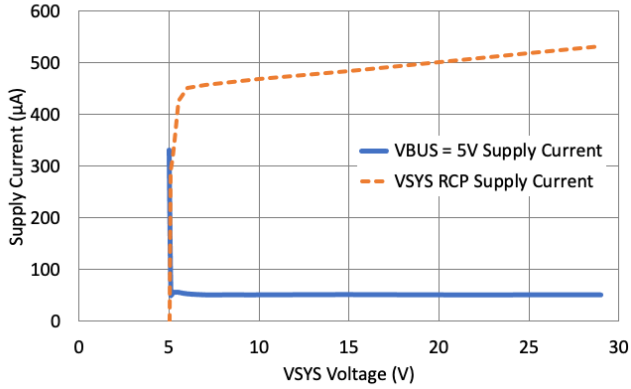
Shutdown Supply Current vs. Supply Voltage
(Shutdown Mode)



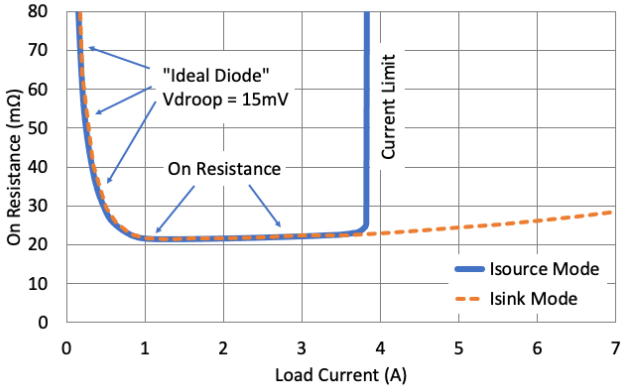
RCP Supply Current in Isource Mode
(V_{SYS} = 5V, enabled, V_{BUS} lifted)



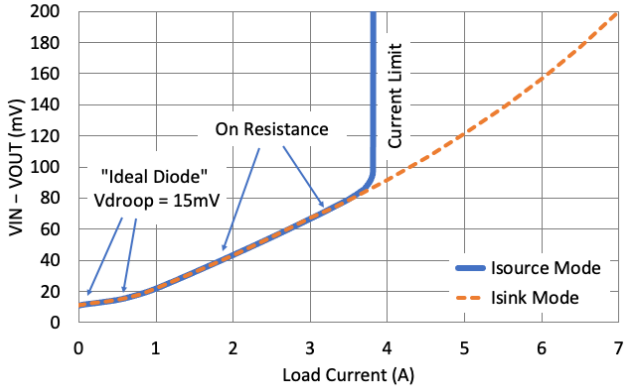
RCP Supply Current in Isink Mode
(V_{BUS} = 5V, enabled, V_{SYS} lifted)



On Resistance vs. Load Current
(V_{IN} ≥ 5V, enabled, R_{ISET} = 14.7kΩ)



"Ideal Diode" Vdroop vs. Load Current
(V_{IN} ≥ 5V, enabled, R_{ISET} = 14.7kΩ)



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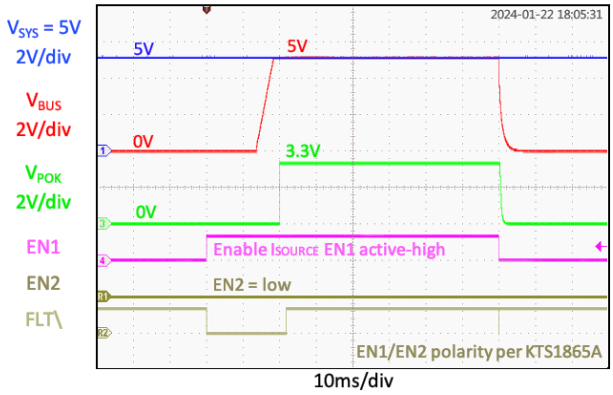
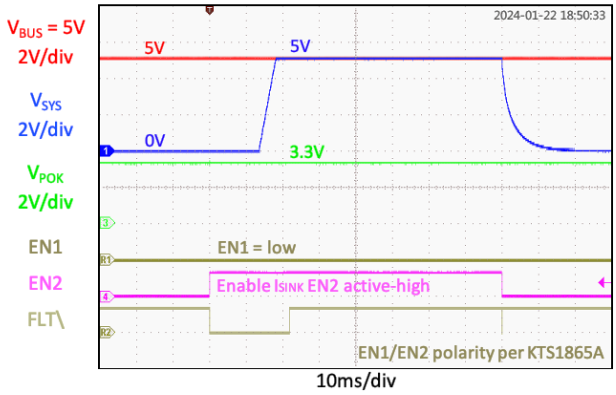
Typical Characteristics (continued)

C_{VSYS} = 2x 22µF, C_{VBUS} = 10µF, C_{POK} = 4.7µF, FON = 0, R_{ISET} = 14.7kΩ, T_A = 25°C, unless otherwise specified.

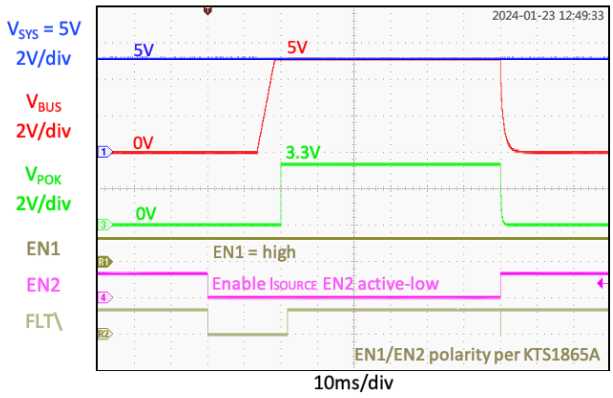
Active-High Enable/Soft-Start in ISOURCE Mode
(VSYS = 5V, RLOAD_VBUS = 100Ω, RLOAD_POK = 300Ω)



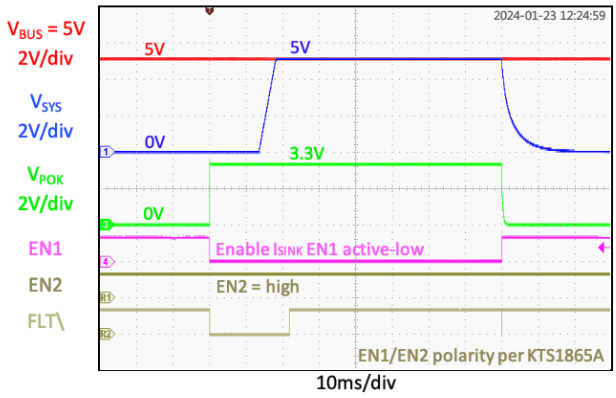
Active-High Enable/Soft-Start in ISINK Mode
(VBUS = 5V, RLOAD_VSYS = 100Ω, RLOAD_POK = 300Ω)



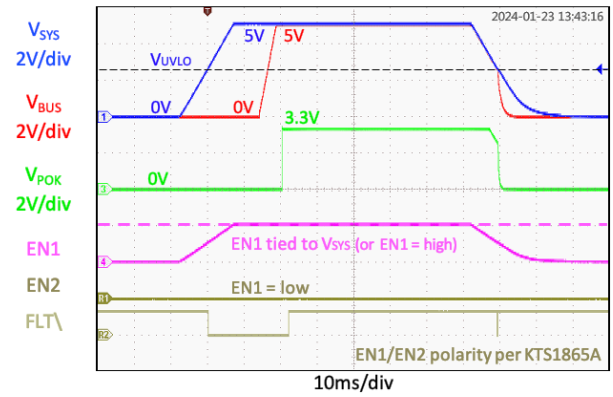
Active-Low Enable/Soft-Start in ISOURCE Mode
(VSYS = 5V, RLOAD_VBUS = 100Ω, RLOAD_POK = 300Ω)



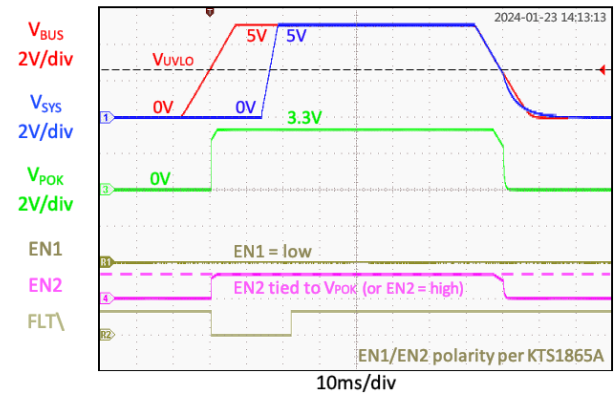
Active-Low Enable/Soft-Start in ISINK Mode
(VBUS = 5V, RLOAD_VSYS = 100Ω, RLOAD_POK = 300Ω)



Rising VSYS Enable/Soft-Start in ISOURCE Mode
(RLOAD_VBUS = 100Ω, RLOAD_POK = 300Ω)



Rising VBUS Enable/Soft-Start in ISINK Mode
(RLOAD_VSYS = 100Ω, RLOAD_POK = 300Ω)



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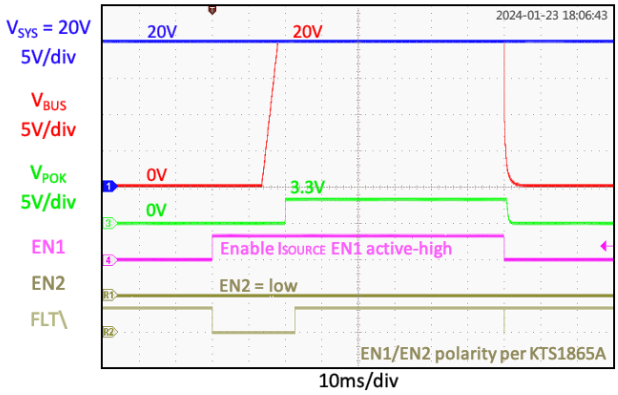
Typical Characteristics (continued)

C_{VSYS} = 2x 22µF, C_{VBUS} = 10µF, C_{POK} = 4.7µF, FON = 0, R_{ISET} = 14.7kΩ, T_A = 25°C, unless otherwise specified.

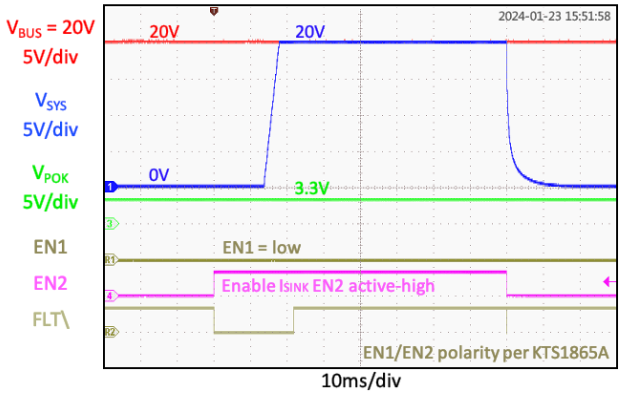
20V Enable/Soft-Start in ISOURCE Mode

(V_{SYS} = 20V, R_{LOAD_VBUS} = 100Ω, R_{LOAD_POK} = 300Ω)



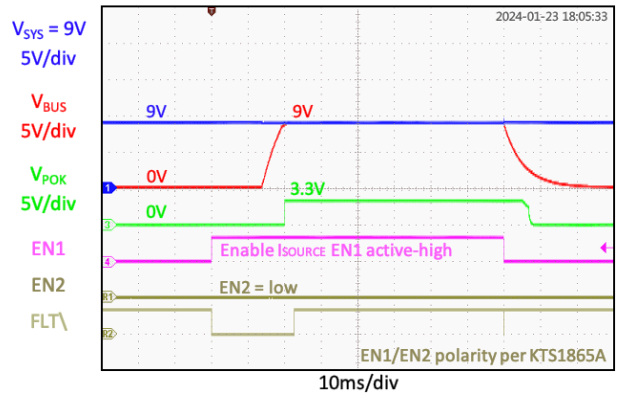
20V Enable/Soft-Start in ISINK Mode

(V_{BUS} = 20V, R_{LOAD_VSYS} = 100Ω, R_{LOAD_POK} = 300Ω)



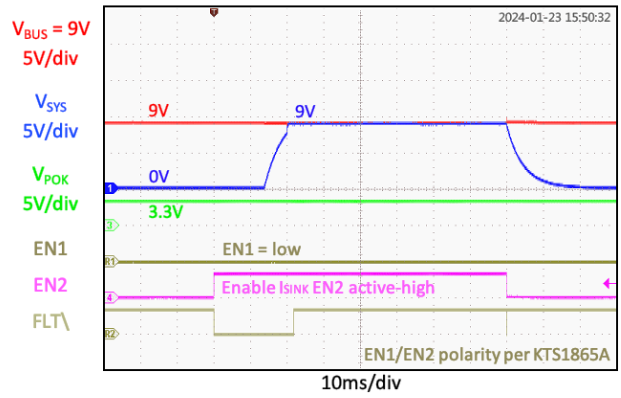
Heavy Load Enable/Soft-Start in ISOURCE Mode

(V_{SYS} = 9V, C_{VBUS} = 1000µF, R_{LOAD_VBUS} = 6Ω)



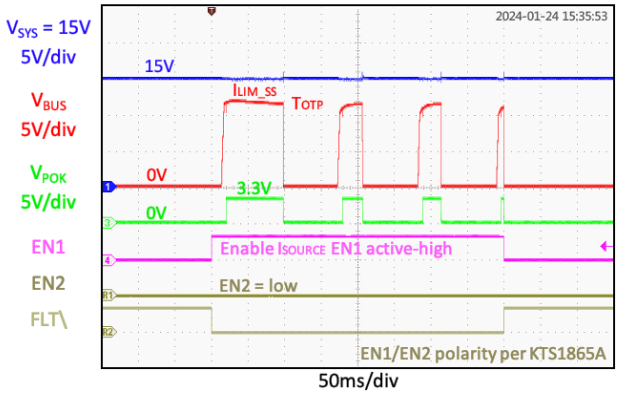
Heavy Load Enable/Soft-Start in ISINK Mode

(V_{BUS} = 9V, C_{VSYS} = 1000µF, R_{LOAD_VSYS} = 5Ω)



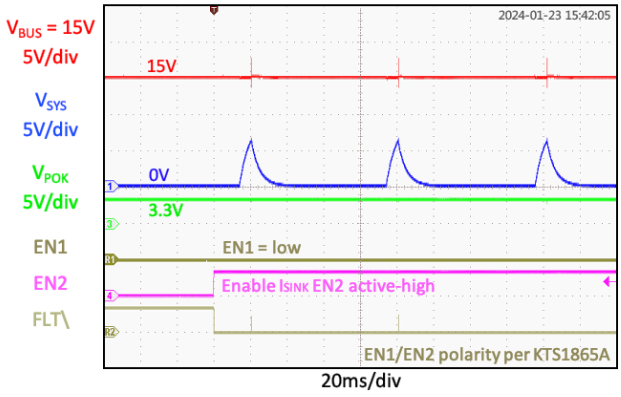
Over-Load Enable/Auto-Retry in ISOURCE Mode

(V_{SYS} = 15V, C_{VBUS} = 10µF, R_{LOAD_VBUS} = 6Ω)



Over-Load Enable/Auto-Retry in ISINK Mode

(V_{BUS} = 15V, C_{VSYS} = 1000µF, R_{LOAD_VSYS} = 5Ω)

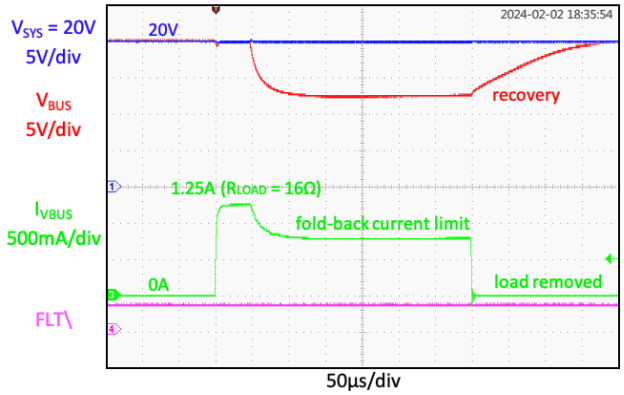


(continued next page)

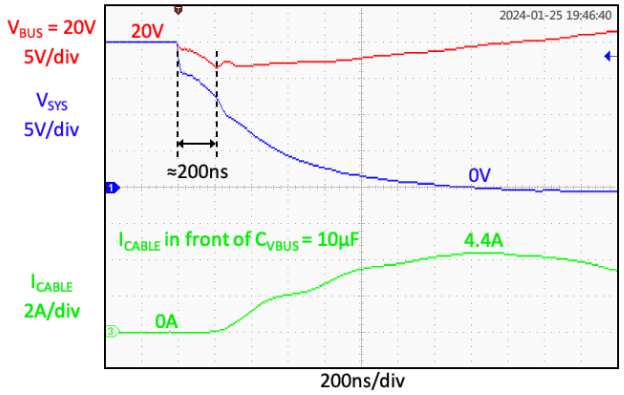
Typical Characteristics (continued)

C_{VSYS} = 2x 22µF, C_{VBUS} = 10µF, C_{POK} = 4.7µF, FON = 0, R_{ISET} = 14.7kΩ, T_A = 25°C, unless otherwise specified.

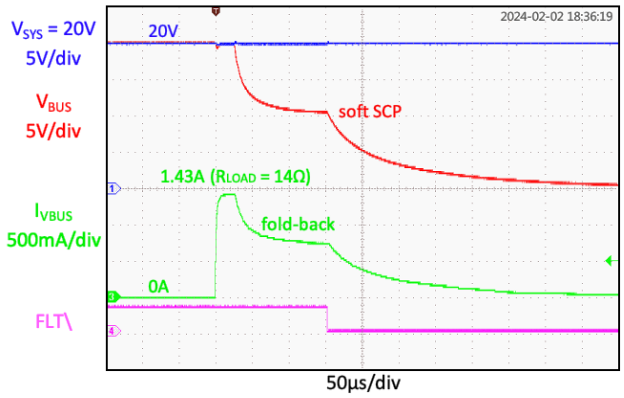
CLP Response in ISOURCE Mode
(VSYS = 20V, RISET = 51kΩ)



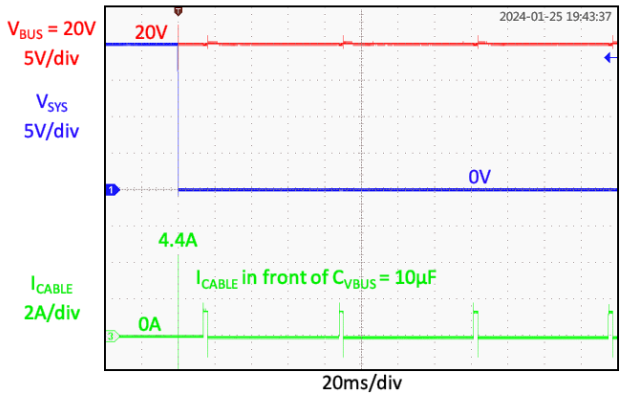
OCP/SCP Response in ISINK Mode
(VBUS = 20V, VSYS = sudden short circuit)



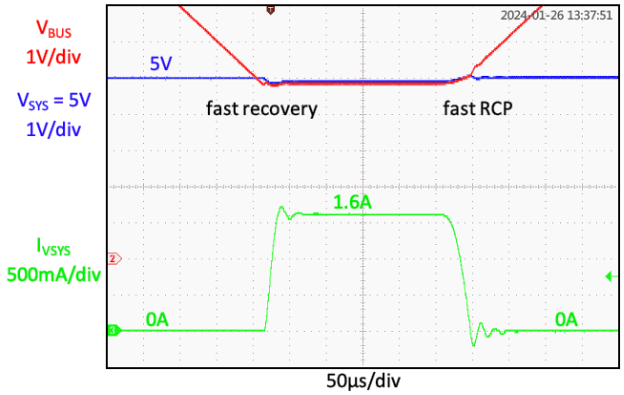
CLP & Soft SCP Response in ISOURCE Mode
(VSYS = 20V, RISET = 51kΩ)



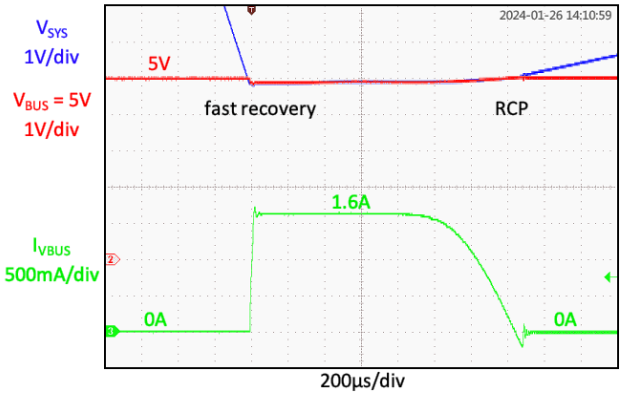
SCP & Auto-Retry Response in ISINK Mode
(VBUS = 20V, VSYS = sudden short circuit)



"Ideal Diode" RCP Response in ISOURCE Mode
(VSYS = 5V, VBUS = 9V → high-Z → 9V, RLOAD_VBUS = 3Ω)



"Ideal Diode" RCP Response in ISINK Mode
(VBUS = 5V, VSYS = 9V → high-Z → 9V, RLOAD_VSYS = 3Ω)



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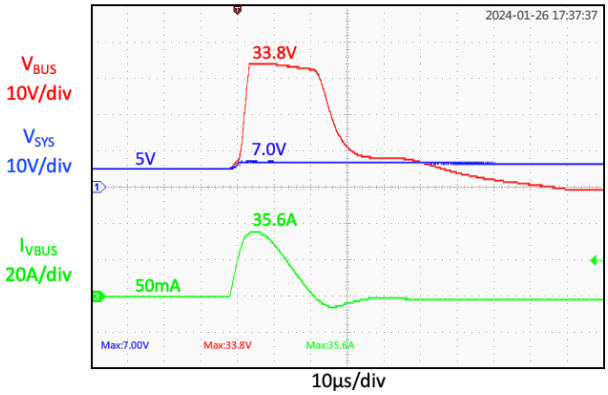
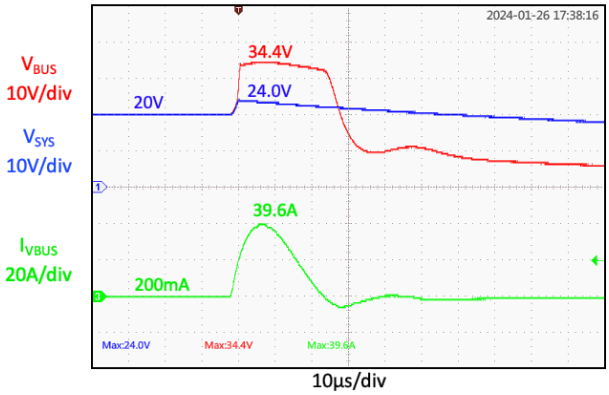
Typical Characteristics (continued)

C_{VSYS} = 2x 22µF, C_{VBUS} = 10µF, C_{POK} = 4.7µF, FON = 0, R_{ISET} = 14.7kΩ, T_A = 25°C, unless otherwise specified.

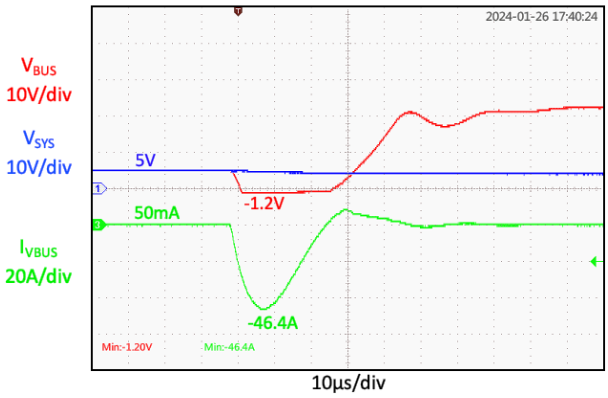
Surge Transient Response
(V_{BUS} = 5V_{DC} + 100V_{SURGE}, C_{VBUS} = 10µF, I_{SINK} Mode)



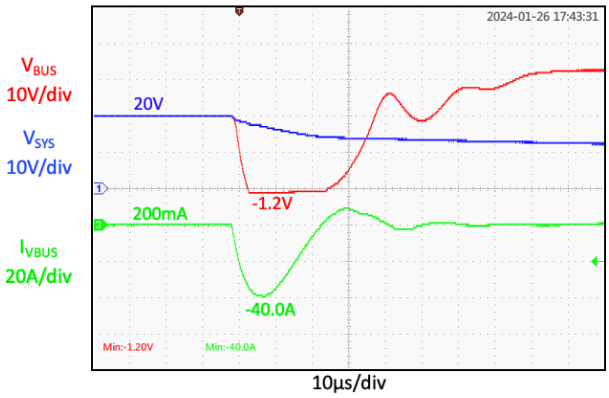
Surge Transient Response
(V_{BUS} = 20V_{DC} + 100V_{SURGE}, C_{VBUS} = 10µF, I_{SINK} Mode)



Surge Transient Response
(V_{BUS} = 5V_{DC} - 100V_{SURGE}, C_{VBUS} = 10µF, I_{SINK} Mode)



Surge Transient Response
(V_{BUS} = 20V_{DC} - 100V_{SURGE}, C_{VBUS} = 10µF, I_{SINK} Mode)



Functional Block Diagram

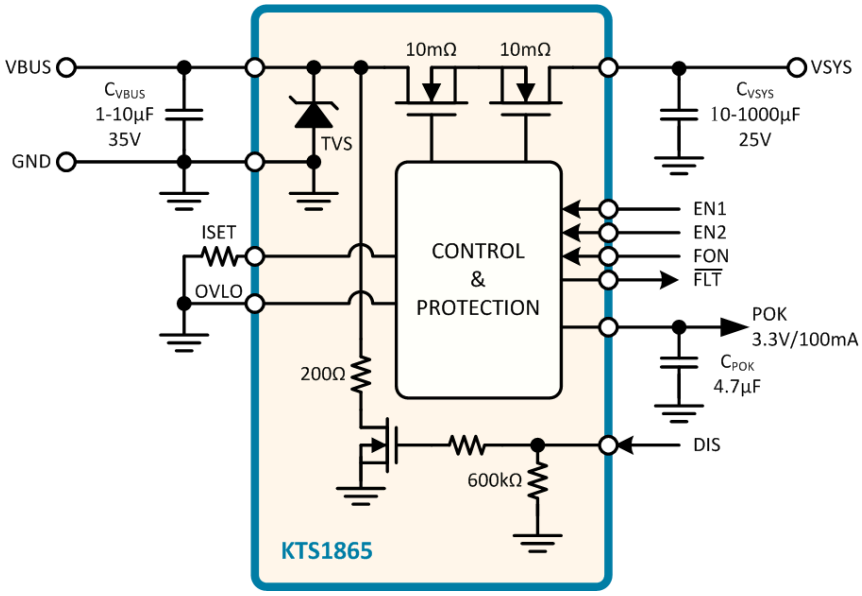


Figure 5. Functional Block Diagram

Functional Description

The KTS1865 is a bi-directional, slew-rate controlled, 20mΩ (typ) low resistance MOSFET switch intended to be inserted between a power source and a load to isolate and protect against abnormal voltage and current conditions. It is intended for USB Power Delivery up to 6.5A/130W current-sinks, up to 5A/100W current-sources, or dual-role power (DRP) applications. Featuring slew-rate controlled soft-start and soft-start current limit to prevent excessive large inrush current, the KTS1865 also features many additional protection functions. These include over-voltage protection, "ideal diode" reverse-current protection with fast recovery, output short-circuit protection, over-current protection, programmable current limit protection, over-temperature protection, and transient voltage suppression for ±100V surge, ±30kV contact ESD, and ±30kV air-gap ESD protections.

Operating from a wide input voltage range of 3V to 23V, the KTS1865 is optimized for USB Standard Power Range (SPR) Type-C Power Delivery (PD) applications that require essential protection and enhanced system reliability. While in the OFF state, the KTS1865 blocks voltages of up to 29V on the VBUS and VSYS pins and prevents current flow. While in the ON state, the KTS1865 withstands voltages of up to 29V on the VBUS and VSYS pins, passes valid input voltages and current from VBUS to VSYS in I_{SINK} mode or from VSYS to VBUS in I_{SOURCE} mode, and blocks reverse current flow in both modes using an "ideal diode" control circuit with fast recovery. Due to the ideal-diode behavior, two or more KTS1865 parts may be used in parallel in "diode-OR" configuration to support systems that are charged or powered from multiple ports.

EN1 and EN2 Inputs

The KTS1865 has EN1 and EN2 logic inputs which control the Shutdown vs. I_{SINK} vs. I_{SOURCE} modes and the POK LDO on/off status. See Table 1 in the *Ordering Information* section for various EN1/EN2 mode-control options.

Under-Voltage Lockout (UVLO)

When $V_{BUS} < V_{UVLO}$ in I_{SINK} mode or $V_{SYS} < V_{UVLO}$ in I_{SOURCE} mode, the power switch is disabled. Once V_{BUS} or V_{SYS}, respectively, exceeds V_{UVLO}, the power switch is controlled by the enable pins and fault detection circuits.

Soft-Start (SS)

The internal soft-start function allows the KTS1865 to charge a total output capacitance of 1000µF to 5V (or even 9V) without excessive in-rush current. Soft-start controls the output voltage slew-rate ramp time. Use the below formula to calculate the current required to charge a combination of load current and output capacitance:

$$I_{IN\_SS} = I_{LOAD} + C_{OUT}\left(\frac{V_{IN}}{t_R}\right)$$

where t_R = 3ms.

Note that in addition to the soft-start voltage ramp, the KTS1865 also limits soft-start current for 7ms in case of starting into large capacitance. The current limit is fixed at 2A in I_{SINK} mode. But in I_{SOURCE} mode, the current limit matches the fold-back current limit in normal operation, as set by external resistor R_{ISET}. When soft-start becomes current limited, use t_R = 7ms. Futhermore, if there is a large difference between the input and output voltages, such as when soft-starting with high input voltage, the current limit reduces by as much as 50% to reduce power dissipation during soft-start.

Also note that the KTS1865 safely starts into pre-charged output voltages (that are not fully discharged to ground prior to soft-start). The output voltage just rises from its pre-charged level once the soft-start ramp reaches that level.

Once the t_{LIM_SS} = 7ms phase of soft-start is completed, the KTS1865 enters normal operation. Then, after an additional 3ms delay, if the output voltage is near the input voltage, the $\overline{FLT}$ flag releases to indicate a power good condition.

Over-Voltage Protection (OVP)

To use the internal OVP function, tie the OVLO pin to ground. Then, once enabled, if the input voltage exceeds the internally-set V_{OVP} = 23V threshold, the power switch is disabled due to an OVP fault. Once the input voltage drops below V_{OVP} (and no other fault is detected and the device is still logically enabled via EN1/EN2), the power switch is re-enabled after the soft-start debounce and soft-start ramp time.

Adjustable Over-Voltage Lockout (OVLO)

The OVLO pin is used to adjust the OVP threshold externally. The default internal OVP threshold is 23V when the OVLO pin is tied to GND. Biasing the OVLO pin with a resistive voltage divider adjusts the over voltage threshold from 4V to 23V as in the below formula:

$$V_{OVP} = V_{OVLO}\left(1 + \frac{R1}{R2}\right)$$

where V_{OVLO} = 1.227V. Connect R1 from VBUS to OVLO. Connect R2 from OVLO to ground. In some applications, notably I_{SOURCE} mode only use, optionally tie R1 to VSYS (rather than VBUS) if over-voltage protection of VSYS is of value.

Over-Current Protection (OCP)

The KTS1865 includes over-current protection (OCP) that protects the IC from damage when an excessive over-current or short-circuit event suddenly appears. The OCP threshold is purposely high above the rated current

for the KTS1865 such that system load-pulses do not easily trigger OCP. The OCP circuit disables the power switch, so the current becomes zero. After an OCP event (and no other fault is detected and the device is still logically enabled via EN1/EN2), the power switch re-enables via the soft-start debounce and soft-start ramp time.

Short-Circuit Protection (SCP)

The KTS1865 includes output short-circuit protection (SCP). In virtually all conditions, the KTS1865 remains undamaged during continuous SCP events.

If an SCP event occurs while the KTS1865 is already enabled and working, OCP is the first line of defense and responds very quickly. In this case, the current from the input capacitor through the switch to the output increases very rapidly as the output voltage begins to collapse. The OCP threshold is purposely high above the rated current for the KTS1865 such that system load-pulses do not easily trigger OCP.

For softer over-load events that do not reach OCP, the power dissipation increases, raising the die temperature. If the die temperature becomes too high, an over-temperature protection (OTP) event is triggered, and the switch opens.

In case of auto-retry or simply starting into a pre-existing SCP condition, the KTS1865 furthermore includes hard and soft SCP detection during soft-start if the output voltage is not ramping up. Hard SCP checks if the output voltage has risen to more than 10% of the input voltage during the soft-start voltage ramp time. Then, at the end of the soft-start current limit time, soft-SCP checks again to see if the output voltage has risen to more than 60% of the input voltage. If either of these two conditions is not met, the KTS1865 terminates soft-start, turns off the switch, and auto-retries after the hiccup timer. The $\overline{FLT}$ flag remains low until a successful soft-start is completed.

"Ideal Diode" Reverse-Current Protection (RCP)

The KTS1865 offers reverse-current protection regardless of the enable logic status. In shutdown mode, all current flow is blocked. But in both I_{SINK} and I_{SOURCE} modes, the RCP acts as a voltage droop regulator. See Figure 6. When the voltage on the output is higher than the input voltage minus 15mV, the RCP circuit reduces the MOSFET gate drive to try and maintain a regulated 15mV droop, thereby acting as an "ideal diode" with Vf = 15mV. This control method blocks the reverse current even before there is any reverse voltage bias.

The RCP circuit has high loop-bandwidth for fast transient response. RCP also includes fast recovery with accelerated gate-driver charge pump operation whenever the output droops 50mV below the input. Note that RCP is not defined as a fault condition and has fast recovery without initiating the auto-retry soft-start sequence.

The RCP circuit makes it possible to connect two or more USB charging ports to a single battery charger IC input in a "diode-OR" configuration with autonomous reverse-current blocking. And during Fast Role Swap events, it allows the I_{SOURCE} mode to be enabled even before VBUS falls below 5V. With RCP, the current flows only in the intended direction as defined by the EN1 and EN2 logic status.

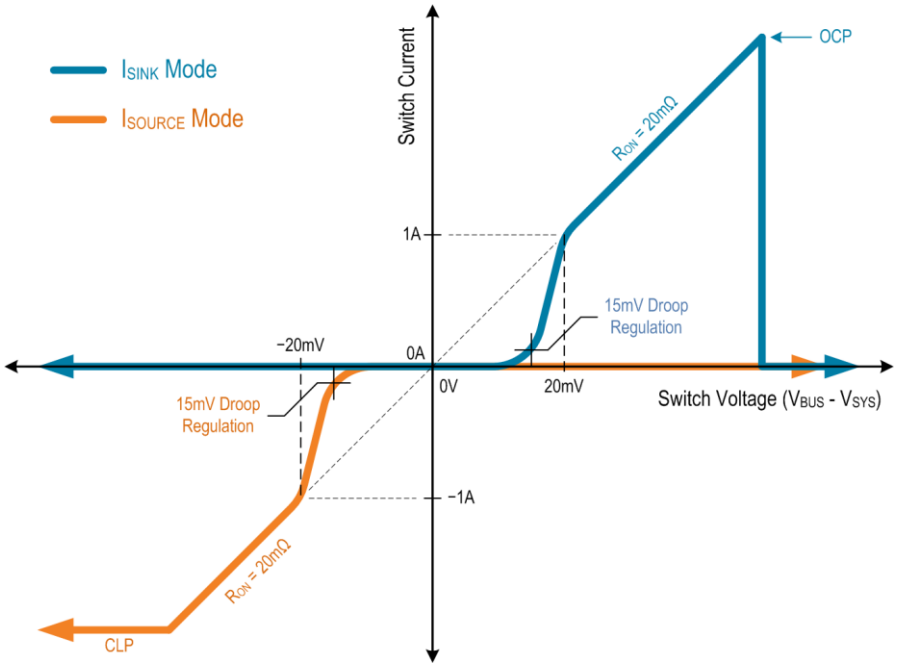


Figure 6. VBUS Switch Current vs. Voltage for RCP, R_{ON}, OCP, and CLP

Current-Limit Protection (CLP)

The CLP function operates only in I_{SOURCE} mode. Program the current limit using an external resistor, R_{ISET}, connected from the ISET pin to ground. See the *CLP Specifications* section of the *Electrical Characteristics* table. Calculate the value of R_{ISET} using the following formula:

$$R_{ISET} = \frac{51000}{I_{CLP\_LIM}}$$

When the switch current reaches the programmed current limit, the current-limit regulation loop takes control and reduces the gate drive to limit the switch current. During CLP, the switch acts as a constant current source, and the output voltage droops depending on the load current. If the load current reduces below the current limit, the output voltage recovers. Note that CLP is not a fault condition and has fast recovery without initiating the auto-retry soft-start sequence.

Fold-Back Current Limit in CLP

As the voltage droops during CLP, the CLP circuit engages fold-back current limit, which occurs when the CLP current increases to 110% of its setting. For this reason, it can make sense to optionally use the following formula for R_{ISET} so as to limit the peak current in CLP:

$$R_{ISET} = \frac{51000}{I_{CLP\_LIM}} \times 1.1$$

Once in fold-back, the current limit reduces to 80% of the CLP setting. As the output voltage droops more, the fold-back current limit reduces even more to limit power dissipation.

During fold-back CLP, if V_{BUS} droops to 60% of V_{SYS} for more than 64µs, the soft SCP triggers, and the switch opens. The device recovers and turns back on via the auto-retry soft-start sequence.

Additionally, during fold-back CLP, power dissipation increases, which may trigger an OTP fault if the die becomes too hot. When the chip temperature cools, the device recovers and turns back on via the auto-retry soft-start sequence.

Fast Role Swap (FRS) via Fast Turn On (FON)

To support USB power delivery (PD) fast role swap (FRS), set the FON pin to logic 1. With FON = 1, the soft-start sequence skips the debounce time, and the soft-start ramp time reduces to 50µs typ. There are two start-up sequences for Fast Turn On:

1. If $V_{OUT} < V_{IN}$, the switch performs a Fast Turn On, and the switch turns on in about 50µs.
2. If $V_{OUT} > V_{IN}$, the switch enters RCP mode and remains off. Later when V_{OUT} falls 20mV below V_{IN}, the RCP naturally recovers. But if V_{OUT} falls to 50mV below V_{IN} due to heavy loads, the RCP fast-recovery circuit turns the switch on more quickly with accelerated gate drive to limit further droop.

Note that during sequence 1 above, inrush current is much higher than during normal soft-start. For this reason, adjust C_{VSYS} accordingly to limit voltage droops within the tolerance of the system. Do not set FON = 1 unless FRS has been previously negotiated via PD communications. Under normal soft-start conditions, FON = 0 provides much lower in-rush current.

Over-Temperature Protection (OTP)

When device junction temperature exceeds 150°C, the OTP circuit disables the power switch. Once the device junction temperature decreases below 130°C (and no other fault is detected and the device is still logically enabled via EN1/EN2), the device recovers and turns back on via the auto-retry soft-start sequence.

Transient Voltage Suppression (TVS)

The KTS1865 integrates an active clamp transient voltage suppressor (TVS) from VBUS to GND. The TVS circuit provides protection to the KTS1865 and downstream circuits for IEC surge and ESD events. The protection is always active, whether the KTS1865 is in shutdown, I_{SINK} mode, I_{SOURCE} mode, or POK LDO only mode.

$\overline{FLT}$ Output Flag

The $\overline{FLT}$ output is an open-drain logic output that requires an external pull-up resistor with recommended value in the 10kΩ to 200kΩ range. The $\overline{FLT}$ pin indicates the fault status. During fault conditions (OVP, OCP, SCP, and OTP) and during soft-start, the $\overline{FLT}$ flag is active low. When there is no fault and after soft-start is finished, the power switch is on, then the $\overline{FLT}$ flag is high-Z and pulled up via the external resistor to indicate the power is good and there is no fault condition. CLP and RCP events are not faults, so the $\overline{FLT}$ flag remains high-Z during these events. Note that CLP and RCP also have fast recovery without initiating the auto-retry sequence.

Auto-Retry with Hiccup Timer

For all fault conditions that cause the switch to open, the KTS1865 will periodically auto-retry via the soft-start debounce and soft-start ramp time. If any fault or the same fault is detected again, the switch will open again, and auto-retry will repeat. This continues until the fault is removed (normal operation) or the device is shutdown via EN1 and EN2 or input power is removed (UVLO). Note that CLP and RCP events are not fault conditions and have fast recovery without initiating the auto-retry sequence.

After an unsuccessful soft-start or auto-retry event, the $\overline{FLT}$ flag remains low, and a 64ms hiccup time is inserted before the next auto-retry attempt. The hiccup timer provides additional cooling time to reduce average power

dissipation during prolonged fault conditions. Note that the hiccup time is not inserted before the first auto-retry attempt, but rather only during subsequent attempts.

VBUS Active Discharge (DIS)

The KTS1865 includes an active discharge circuit to pull V_{BUS} below vSafe0V within USB Type-C compliant discharge timing specifications. The pull-down resistance at VBUS depends upon the DIS pin voltage level. See the *DIS Specifications* section of the *Electrical Characteristics* table.

POK Safe LDO

When VBUS is above UVLO, the POK Safe LDO provides an "always on" 3.3V/100mA power source when enabled via EN1 and EN2 (see Table 1), regardless of the OVP, OVLO, OCP, and SCP fault states. The POK LDO may be used to power downstream components, thereby permitting operation without an installed battery or a dead battery. The POK output is disrupted during UVLO, OTP (thermal shutdown) and some IEC surge and ESD events.

The POK Safe LDO output can only source current; it cannot sink current. Therefore, its output may be safely tied to the outputs of other low-voltage regulators in the system that also only source current, such as the POK LDO output from another KTS1865, for example. In such configuration, the regulator with the highest output voltage provides current to the load.

At higher VBUS voltages, the POK LDO may dissipate considerable power, depending upon the load current. In such cases, care should be given to avoid excessive die temperature and heat in the system.

$$P_{D\_POK\_LDO} = (V_{BUS} - 3.3V) * I_{LOAD}$$

For example, at V_{BUS} = 20V and 100mA load, the power dissipation is 1.67W. For this example, it is necessary to switch the POK LDO's load to a different power rail before VBUS ramps from 5V to 20V.

Applications Information

VSYS Capacitor C_{VSYS} Selection

For most applications, connect from 10µF to 1000µF total capacitance to the VSYS. Typical applications use 30µF to 100µF as needed for system load-transients. At minimum, connect a 10µF ceramic capacitor as close as possible to the device from VSYS to GND to minimize the effect of parasitic trace inductance. 25V rated capacitors with X5R or better dielectric are recommended. Lower voltage ratings are acceptable when using the OVLO pin to set a lower over-voltage protection threshold.

VBUS Capacitor C_{BUS} Selection

For most applications, connect a 1µF to 10µF ceramic capacitor as close as possible to the device from VBUS to GND to minimize the effect of parasitic trace inductance. 35V or 50V rated capacitors with X5R or better dielectric are recommended. For optimal surge and ESD performance, 10µF is preferred. The USB specifications state that a maximum of 10µF is allowed on VBUS at the USB port connection.

Recommended PCB Layout

Good PCB thermal design is required to support heavy load currents. The KTS1865 EVB is designed with similar layout as Figure 7, but it extends the fill area for the VSYS, VBUS, and GND copper planes to over 4 square inches total area for increased thermal performance. Due to the number of bumps on VSYS and VBUS, these two planes are especially important for thermal conduction and should not be ignored. Adding back-side and/or buried-layer fill area with thermal vias also helps significantly.

Other than thermal concerns, the PCB layout for the KTS1865 is quite simple. Place the VSYS and VBUS capacitors near the IC. Connect the capacitor ground terminals together and to the GND pins using the top-side copper layer. Route the control signals on buried layers. With 0.5mm bump pitch, PCB signal traces may be routed between edge bumps to reach inner bumps. Or route the inner bumps using filled, in-pad micro-vias, as these have become more available even in low-cost, two-layer PCB manufacturing.

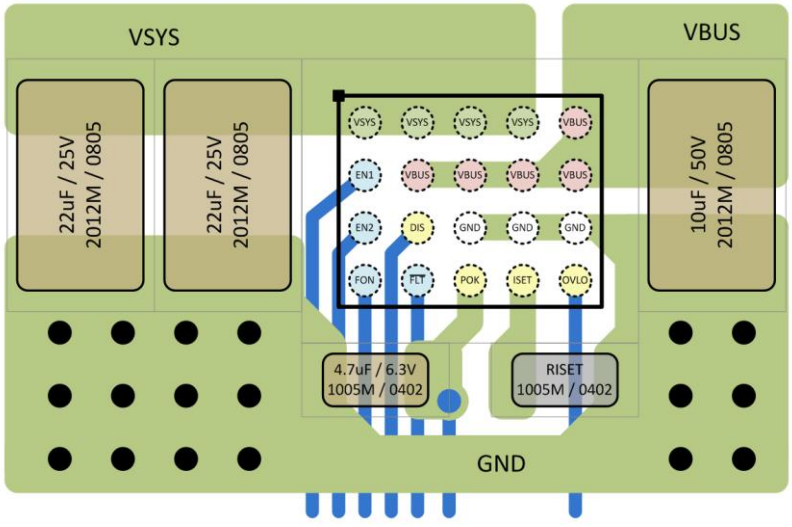


Figure 7. Recommended PCB Layout

Safe Operating Area (SOA)

See Figure 8 and Figure 9 for the SOA of the KTS1865. SOA curves are normally associated with discrete MOSFETs (which are sometimes co-package with a controller IC). In these competing systems, precautions are necessary to stay within the SOA area. However, the KTS1865 is a monolithic IC with multiple integrated protection features to *automatically* help keep its operation within the SOA area. For example, it includes over-voltage protection (OVP), over-current protection (OCP), and settable current limit protection (CLP). It also includes over-temperature protection (OTP) that is measured on the same monolithic die as the integrated power MOSFETs. Additionally, soft-start is controlled with a voltage ramp and current limit protection (Soft-Start CLP) to safely soft-start even in applications with very high capacitance at the output. Furthermore, the integrated TVS and back-to-back MOSFET switch are optimized to work together as a system, including their tolerances over temperature and process corners.

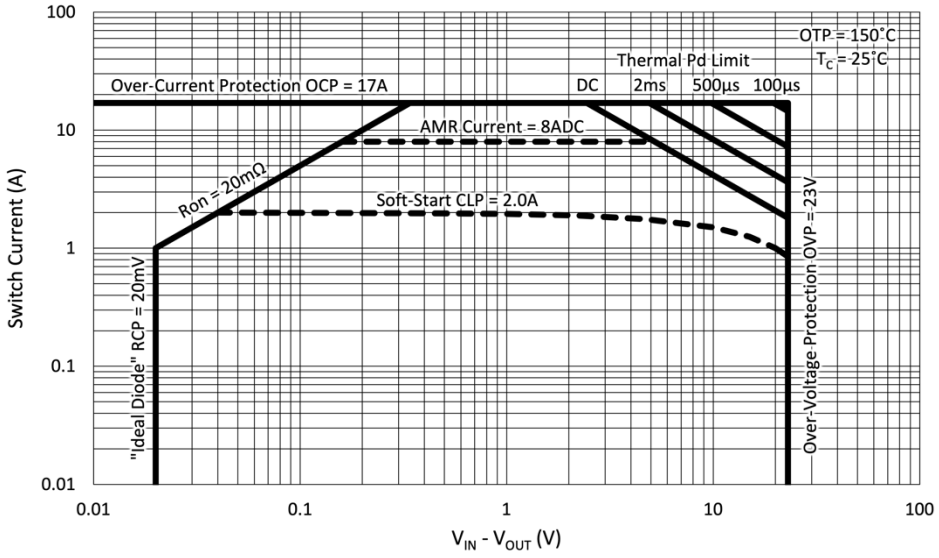


Figure 8. Safe Operating Area (SOA) for T_C = 25℃

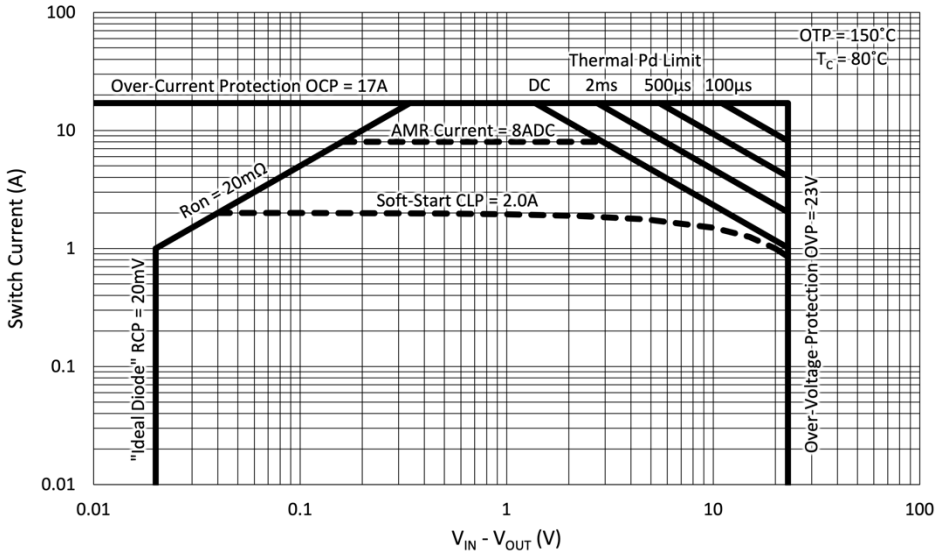
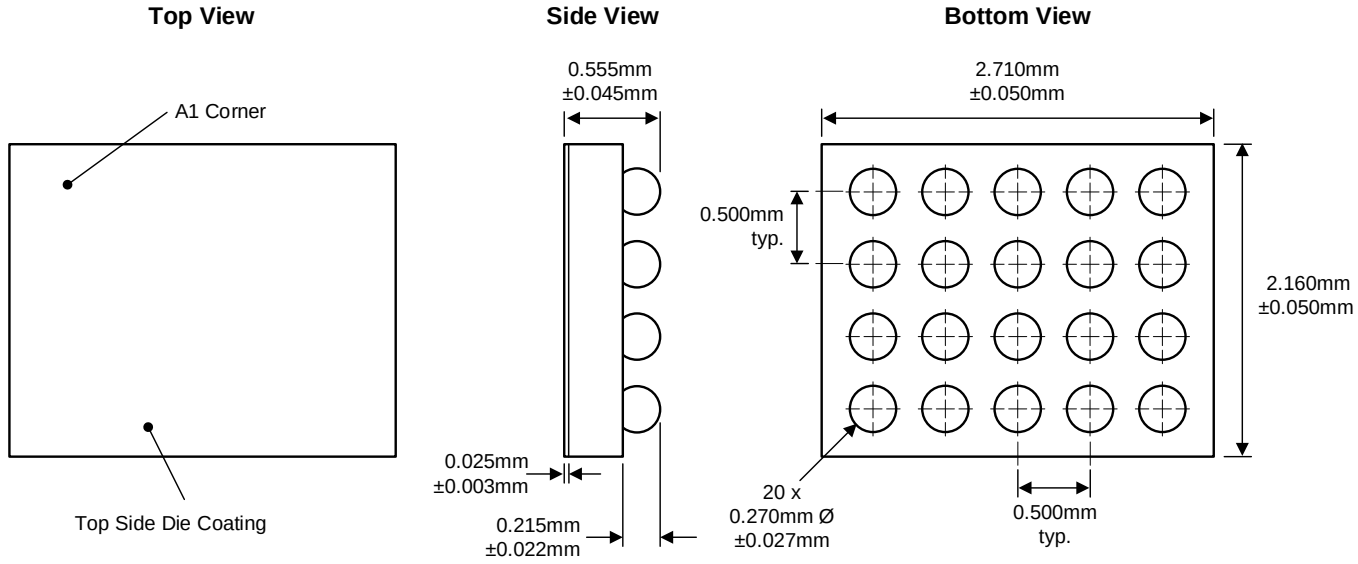


Figure 9. Safe Operating Area (SOA) for T_C = 80℃

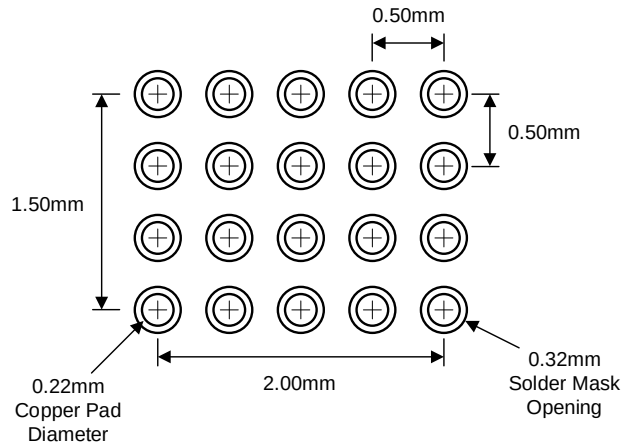
Packaging Information

WLCSP54-20 (2.710mm x 2.160mm x 0.555mm) (Package Code: IAA)



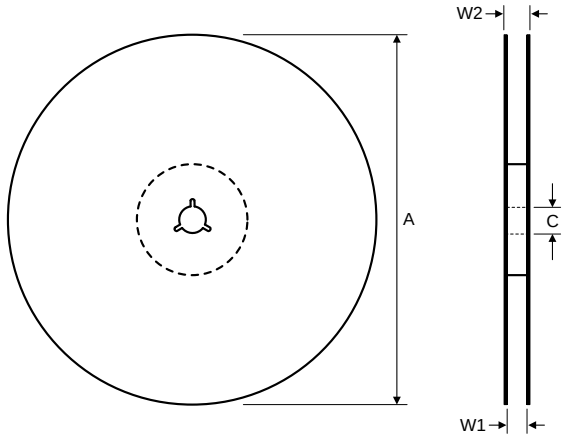
Recommended Footprint

(NSMD Pad Type)



Packaging Material Information

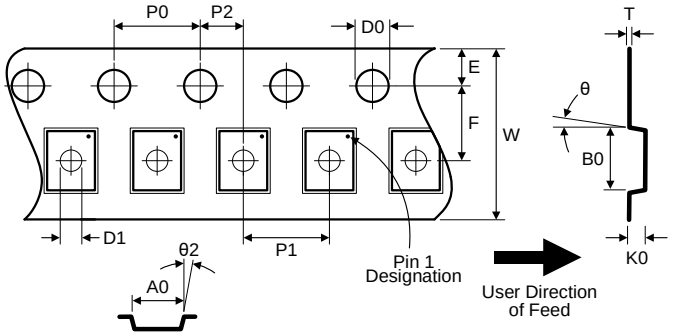
Reel Dimensions



Dimension	mm		
	Min.	Typ.	Max.
A	176	178	180
C	12.8	13.0	13.5
W1	8.4	8.4	9.9
W2	—	—	14.4

DWG-0260-01

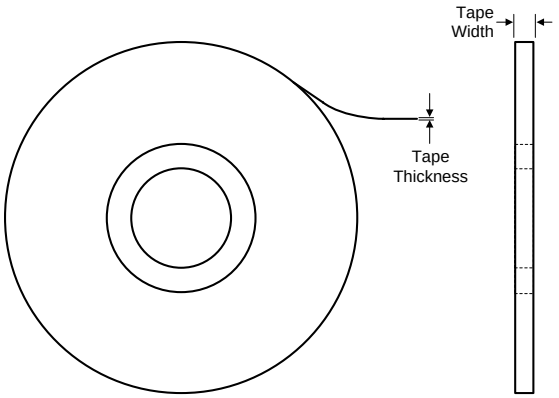
Carrier Tape Dimensions



Dimension	mm		
	Min.	Typ.	Max.
A0	2.17	2.30	2.35
B0	2.81	2.86	2.91
K0	0.77	0.82	0.87
P0	3.80	4.00	4.20
P1	—	4.00	—
P2	1.95	2.00	2.05
D0	1.50	1.50	1.60
D1	1.00	—	—
E	1.65	1.75	1.85
F	3.45	3.50	3.55
10P0	39.8	40.0	40.2
W	7.90	8.00	8.30
T	0.20	0.25	0.30
Θ	0°		5°
Θ2	0°		5°

DWG-0246-01

Cover Tape Dimensions



Dimensions	Dimension	mm		
		Min.	Typ.	Max.
	Tape Thickness	0.04	0.05	0.06
8mm	Tape Width	5.2	—	5.5

DWG-0259-01