

Flat-Clamp Mini TVS for High Voltage Surge & ESD Protection

Features

- Up to $\pm 200\text{V}$ Surge Protection (IEC61000-4-5)
- $\pm 30\text{kV}$ ESD Contact & Air-Gap (IEC61000-4-2)
- $28\text{V}_{\text{IN(TYP)}}$ for EPR 28V system ($V_{\text{RWM}}=33\text{V}$)
- Max clamping voltage of 39V at 80A of 8/20us Surge Current
- -40°C to 85°C Operating Temperature Range
- 6-bump WLCSP 1.66 x 1.56mm (0.5mm pitch)
 - Can co-layout with TVS3300 WLCSP Package
- 6-pin FCDFN 2mm x 2mm Package
 - Can co-layout with TVS3300 DFN Package

Applications

- Any USB or DC Input or Output Power Port
- Smartphones, Tablets, Computers, Docking Stations
- Terminals, Monitors, Cameras, Instrumentation
- Power-Banks, Generators, Rechargeable Devices

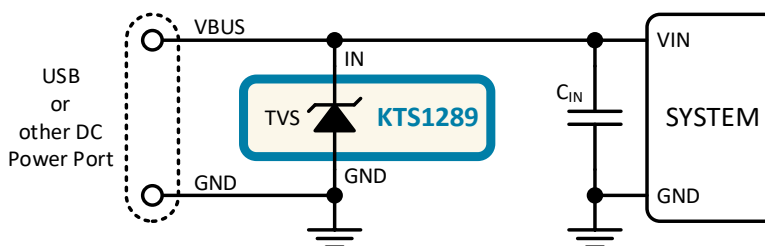
Brief Description

The KTS1289 provides robust transient voltage suppression (TVS) for ESD and surge events that occur at a system's USB or other DC power input or output port. The monolithic IC includes an active-clamp control circuit, a gate-driver, and a power MOSFET to provide higher performance in a smaller footprint compared to typical TVS diodes. The KTS1289 clamps both positive and negative ESD and surge events per IEC standards.

The maximum reverse working voltage and the breakdown voltage of KTS1289 are set appropriately just above the typical supply voltage. The active control circuit clamps the voltage nearly flat during ESD/Surge events while high current is shunted to ground through the integrated power MOSFET. Together, the tightly controlled breakdown voltage and the "flat-clamp" performance reduce the peak voltage seen by capacitors and downstream circuits, thereby easing system design and lowering costs.

The KTS1289 is packaged in advanced, fully "green" compliant, 1.66mm x 1.56mm, 6-bump Wafer-Level Chip-Scale Package (WLCSP) or FCDFN22-6 Package.

Typical Application

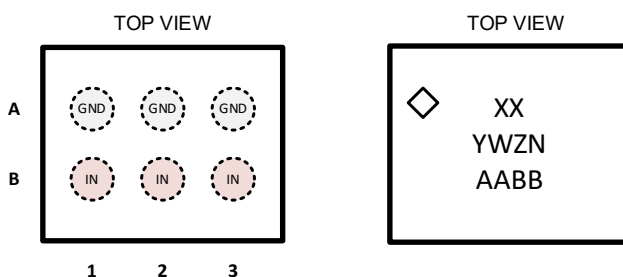


Ordering Information

Part Number	Marking	V _{IN(TYP)}	V _{RWM}	Package
KTS1289ECAE-TA	VHYWZNAABB ¹	28V	33V	WLCSP-6
KTS1289Exxx-Tx ²	XXYWZ ³			FCDFN22-6

Pinout Diagram

WLCSP32-6

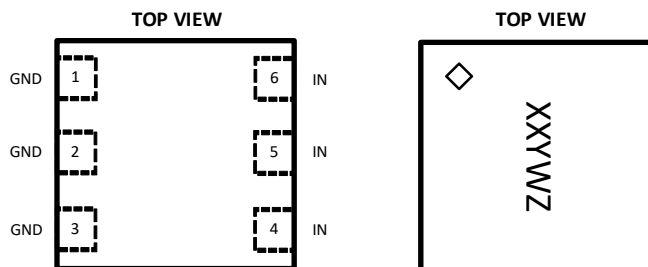


6-bump 1.66mm x 1.56mm x 0.555mm
WLCSP Package, 0.500mm pitch

Top Mark

XX = Device ID,
YW = Date Code, ZN = Assembly Code,
AABB = Serial Number

FCDFN22-6²



6-Lead 2.0mm x 2.0mm x 0.75mm
FCDFN Package, 0.650mm pitch

Top Mark

XX = Device ID, YW = Date Code, Z = Assembly Code

Pin Descriptions

Pin #		Name	Function
WLCSP32-6	FCDFN22-6 ²		
A1, A2, A3	1,2,3	GND	Ground – high current ground return path during Surge/ESD events
B1, B2, B3	4,5,6	IN	Power Input – connect to power input/output port (VBUS on USB port).

1. VH = Device ID Code, YW = Date Code, ZN = Assembly Code, AABB = Serial Number.

2. Consult Kinetic Technologies authorized representative for availability.

3. XX = Device ID Code, YW = Date Code, Z = Assembly Code.

Absolute Maximum Ratings⁴

Symbol	Description	Value	Units
V _{IN}	IN to GND (continuous)	-0.3 to V _{BR}	V
P _{PP}	IEC 61000-4-5 Peak Pulse Power (8/20 μs)	3300	W
T _J	Die Junction Operating Temperature Range	-40 to 150	°C
T _S	Storage Temperature Range	-55 to 150	°C
T _{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

ESD and Surge Ratings⁵

Symbol	Description	Value	Units
V _{ESD_HBM}	ANSI/ESDA/JEDEC JS-001 Human Body Model	±2	kV
V _{ESD_CD}	IEC61000-4-2 Contact Discharge	±30	kV
V _{ESD_AGD}	IEC61000-4-2 Air Gap Discharge	±30	kV
V _{SURGE}	IEC61000-4-5 (8/20μs) Surge	±200	V

Thermal Capabilities⁶

Symbol	Description	Value	Units
WLCSP32-6			
Θ _{JA}	Thermal Resistance – Junction to Ambient	95.1	°C/W
P _D	Maximum Power Dissipation at T _A ≤ 25°C (T _J = 150°C)	1.31	W
ΔP _D /ΔT	Derating Factor Above T _A = 25°C	-10.52	mW/°C

Recommended Operating Conditions⁷

Symbol	Description	Value	Units
V _{IN}	Input Supply Voltage (continuous)	0 to V _{RWM}	V
T _A	Ambient Operating Temperature Range	-40 to 85	°C
T _J	Die Junction Operating Temperature Range	-40 to 150	°C
C _{IN}	External Input Capacitor	1 to 10	μF

4. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
5. ESD and Surge Ratings conform to JEDEC and IEC industry standards. Some pins may have higher performance. Surge ratings apply with chip enabled, disabled, or unpowered, unless otherwise noted.
6. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.
7. The recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Kinetic does not recommend exceeding them or designing to Absolute Maximum Rating.

Electrical Characteristics⁸

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$. Typical values are specified at $T_A = +25^{\circ}\text{C}$.

KTS1289 Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Nominal Input Voltage Range		0	28	33	V
V_{RWM}	Maximum Reverse Working Voltage				33	V
I_Q	Quiescent Supply Current	$V_{IN} = 28\text{V}$ $V_{IN} = 30\text{V}$ $V_{IN} = 33\text{V}$		0.1 0.1 3	5 5 15	μA
V_{BR}	Reverse Breakdown Voltage	$I_{IN} = 1\text{mA}$	33.6	35.0	36.4	V
V_F	Forward Voltage	$I_{IN} = -1\text{mA}$	-0.7	-0.5	-0.4	V
R_{DYN}	8/20 μs Surge Dynamic Resistance	Calculated from V_{CLAMP} at 40A and 80 A surge current levels, 25°C		20	40	$\text{m}\Omega$
V_{CLAMP}	Clamping Voltage ⁹	40A IEC 61000-4-5 Surge (8/20 μs) from IN to GND, $V_{IN} = 0\text{V}$ before surge, 25°C		37	38	V
		80A IEC 61000-4-5 Surge (8/20 μs) from IN to GND, $V_{IN} = 0\text{V}$ before surge, 25°C		37.8	39	
		-100A IEC 61000-4-5 Surge (8/20 μs) from IN to GND, 25°C	-5	-3		

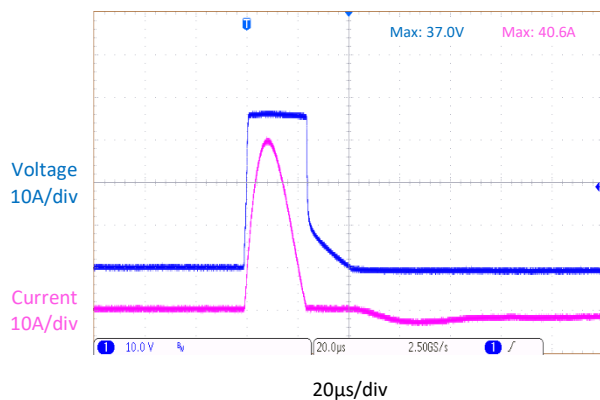
8. Device is guaranteed to meet performance specifications over the -40°C to $+85^{\circ}\text{C}$ operating temperature range by design, characterization, and correlation with statistical process controls.

9. Guaranteed by characterization and/or simulation. Bench characterized using IEC61000-4-5 (8/20 μs) surge with $V_{IN} = V_{IN}(\text{TYP})$.

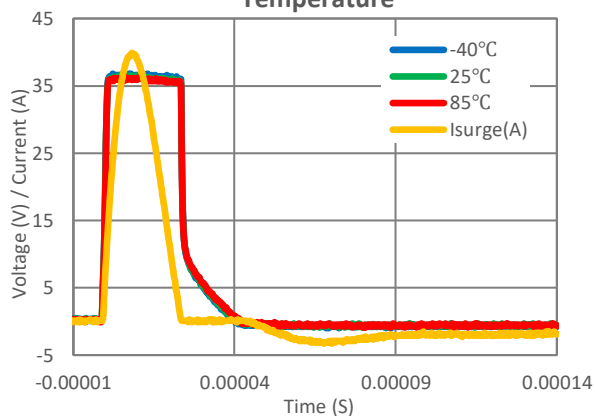
KTS1289 Typical Characteristics

$V_{IN} = 0V$ and $T_A = +25^{\circ}C$, unless otherwise noted.

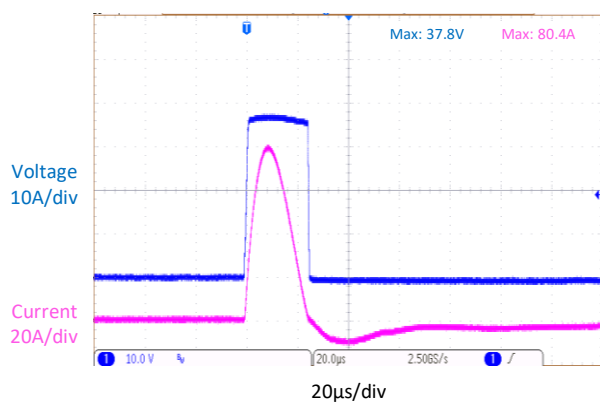
8/20 μ s Surge Response at 40A



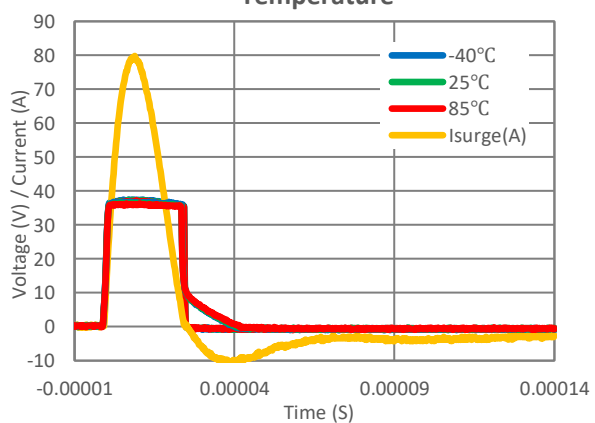
8/20 μ s Surge Response at 40A Across Temperature



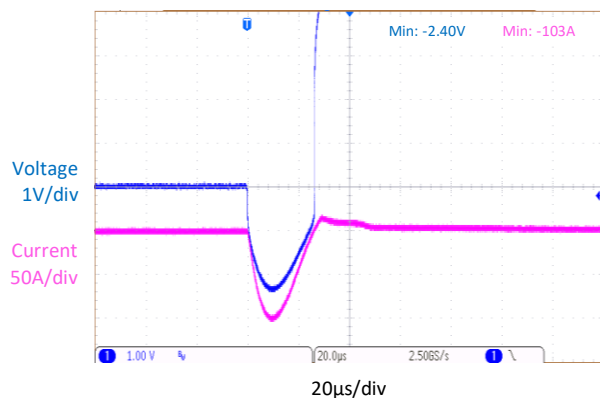
8/20 μ s Surge Response at 80A



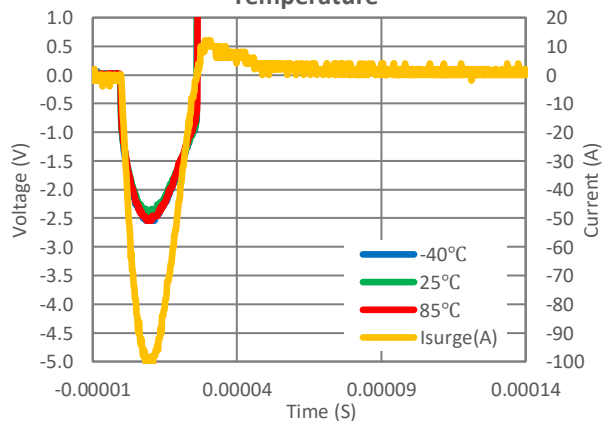
8/20 μ s Surge Response at 80A Across Temperature



8/20 μ s Surge Response at -100A



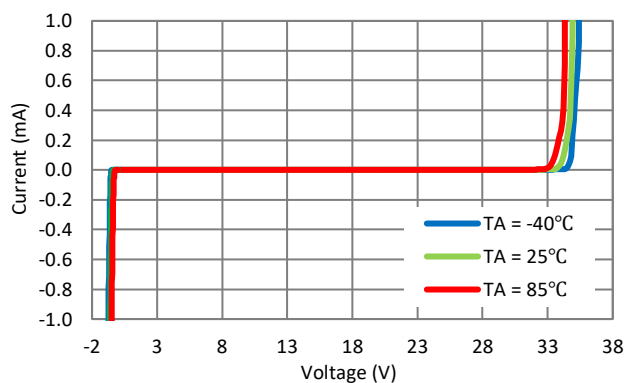
8/20 μ s Surge Response at -100A Across Temperature



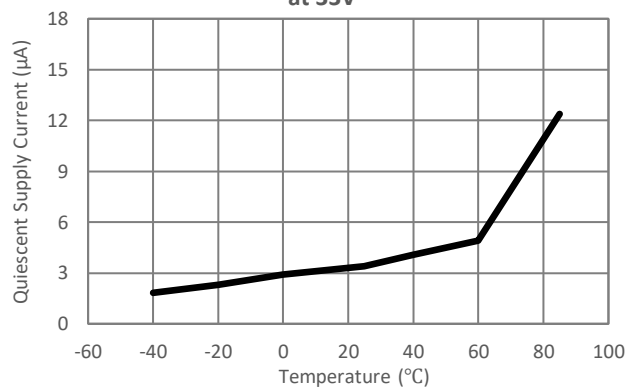
KTS1289 Typical Characteristics (continued)

$V_{IN} = 0V$ and $T_A = +25^{\circ}C$, unless otherwise noted.

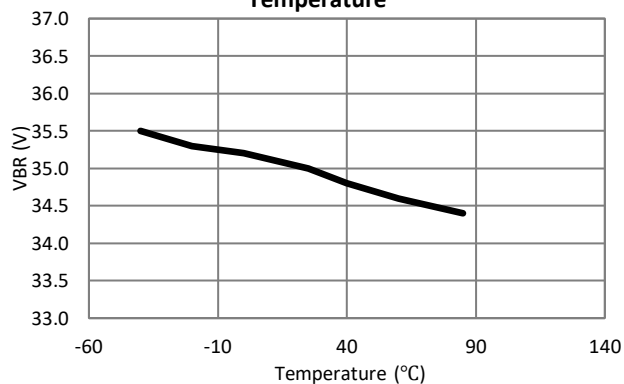
I/V Curve Across Temperature



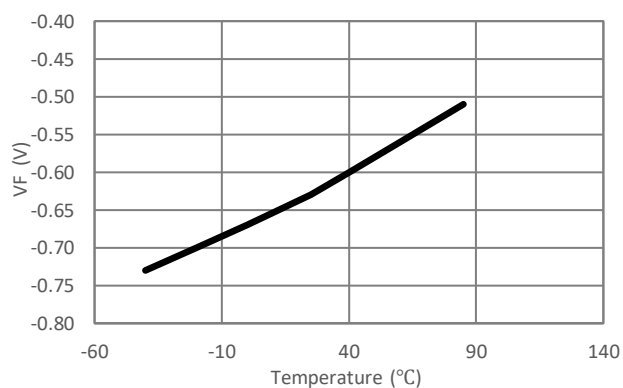
Quiescent Supply Current vs Temperature at 33V



Reverse Breakdown Voltage (1mA) vs Temperature



Forward Voltage (-1mA) vs Temperature



Functional Block Diagram

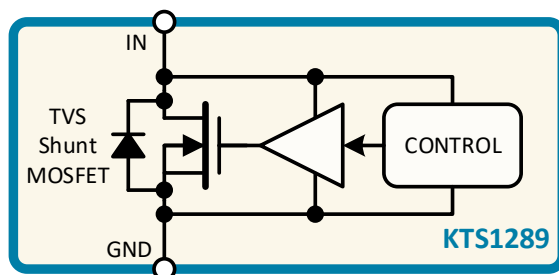


Figure 1. Functional Block Diagram

Functional Description

The KTS1289 is a flat-clamp, active-control transient voltage suppressor (TVS) optimized to protect DC power ports in the 28V nominal range from surge and electrostatic discharge (ESD) events. It is rated to IEC61000-4-5 standards for surge events beyond $\pm 200V_{\text{SURGE}}$ and can discharge up to $I_{\text{pp}}=80\text{A}$ surge current. It is rated to IEC61000-4-2 standards for ESD events up to $\pm 30\text{kV}$ contact and $\pm 30\text{kV}$ air-gap ESD.

The positive and negative surges are imposed to the KTS1289 by a combinational waveform generator (CWG) with a $2\text{-}\Omega$ coupling resistor at different peak voltage levels. For powered on transient tests that need power supply bias, inductances are usually used to decouple the transient stress and protect the power supply. The KTS1289 is post tested by assuring that there is no shift in device breakdown or leakage at V_{RWM} .

“Flat-Clamp” Active Control

The KTS1289 uses a proprietary control circuit to actively drive its integrated power MOSFET and hold the clamping voltage as flat as possible during surge and ESD events. See Figure 2. For comparison, typical TVS diodes suffer substantial rise in V_{CLAMP} at I_{PP} , which can add 10V or more to the absolute maximum voltage rating (V_{AMR}) required for downstream circuits, thereby adding to system costs. The KTS1289’s combination of flat-clamp technology and optimal V_{RWM} specification enables significant reduction in V_{AMR} and cost savings for the downstream system.

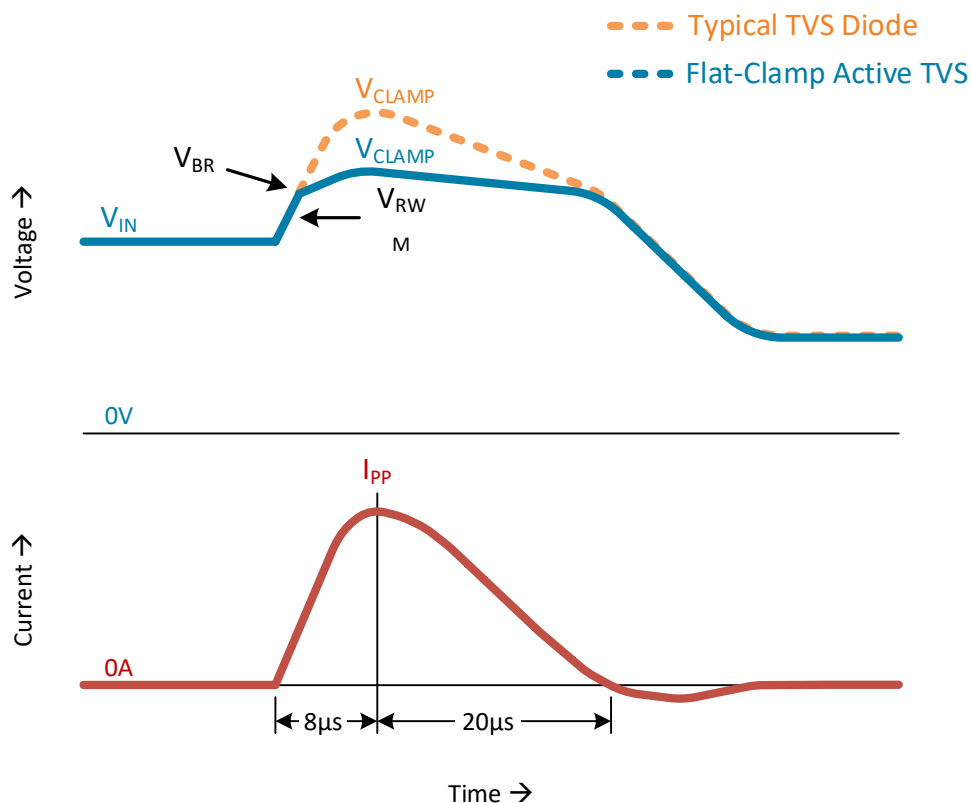


Figure 2. Flat-Clamp TVS vs. Typical TVS Diode during IEC61000-4-5 8/20 μ s Surge Event

Unidirectional TVS Polarity

The KTS1289 is a unidirectional TVS. However, it clamps both positive and negative surge and ESD events. See Figure 3. For positive events, the active control circuit drives the MOSFET gate to shunt current at the clamping voltage. During negative events, the MOSFET's body diode passively clamps the voltage at the body diode's forward voltage, which is one diode drop below ground. See the *Electrical Characteristics* section for detailed specifications.

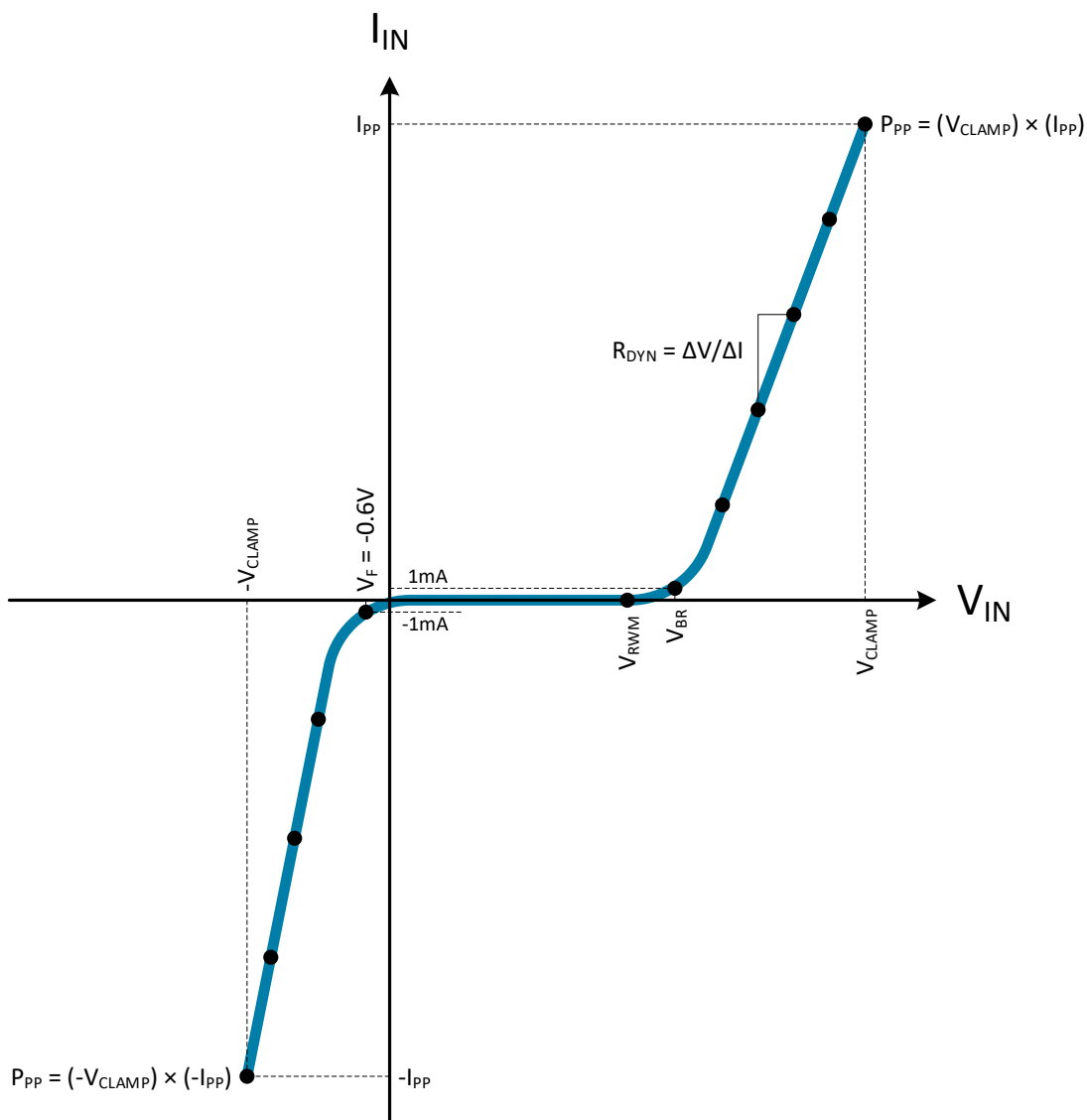


Figure 3. TVS V-I Curve

Applications Information

External Component Selection

Optional Input Capacitor C_{IN}

The KTS1289 works equally well with or without an input capacitor. However, in most cases, input capacitors are required to support other circuits within the application. The recommended voltage rating of the capacitor depends upon the clamping voltage of the TVS version during a surge event. For maximum surge protection, a 50V rated capacitor or higher is recommended.

USB standards limit the total capacitance from VBUS to GND to 10 μ F maximum. Various ICs in the host system may require local bypass capacitance; therefore, the total remaining capacitance available for use at the port may be reduced. If the total system capacitance on VBUS is not easily limited to 10 μ F or less, use a USB protection load-switch with soft-start, such as available from Kinetic Technologies, to isolate large capacitance from the port. These are available with or without integrated TVS, but the integrated solution guarantees that the TVS and load-switch are designed and specified to work together.

Recommended PCB Layout

The PCB layout for the KTS1289 is quite simple, as shown in Figure 4. Place the IC near the port connector. Connect the input capacitor positive terminal to the IN pins. Connect the capacitor ground terminal to the GND pins. Add back-side and/or buried-layer fill area with thermal vias to aid in thermal dissipation after surge events. In practice, there is no significant difference whether the capacitor or the IC is closer to the port, so long as both are next to each other and have short and wide conduction paths to the connector.

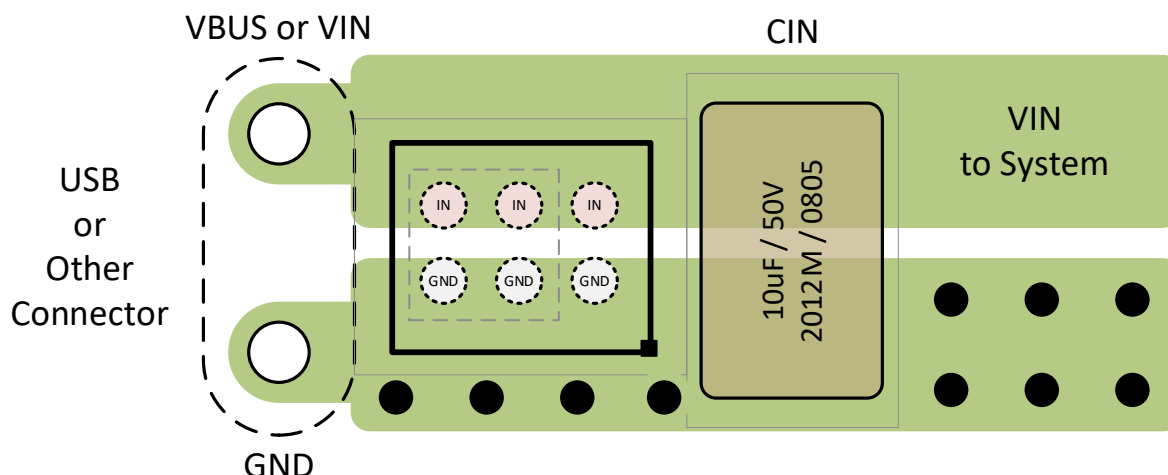


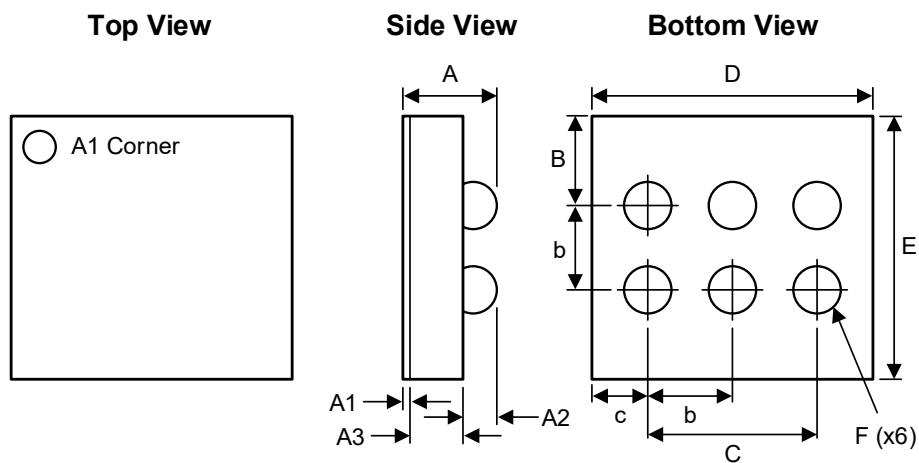
Figure 4. Recommended PCB Layout – the TVS and CIN may swap locations.

Bidirectional TVS Polarity Application

In applications that must withstand both positive and negative DC voltages, bidirectional TVS polarity is required. Use two KTS1289 devices in series, either nose-to-nose or back-to-back. By selecting two of the same KTS1289 version, symmetrical standoff voltages are realized for positive and negative. Note that the naming convention of the KTS1289's IN and GND pins may cause confusion when using the series connection; therefore, optionally treat them as CAT (cathode) and ANO (anode) pins.

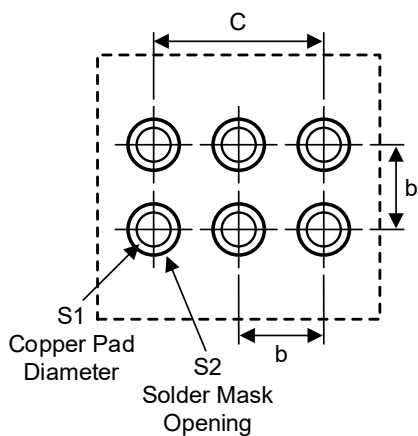
Packaging Information

WLCSP32-6 (1.660mm x 1.560mm x 0.555mm)



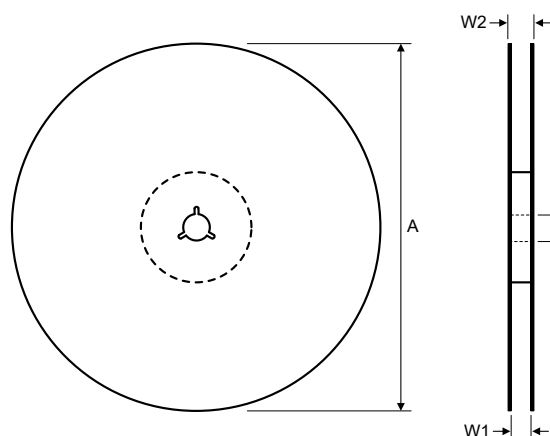
Dimension	mm		
	Min.	Typ.	Max.
A	0.518	0.555	0.592
A1	0.023	0.025	0.027
A2	0.180	0.200	0.220
A3	0.315	0.330	0.345
B	0.530 REF.		
b	0.500 REF.		
C	1.000 REF.		
c	0.330 REF.		
D	1.610	1.660	1.710
E	1.510	1.560	1.610
F	0.252	0.280	0.308
S1	—	0.200	—
S2	—	0.302	—

Recommended Footprint



Packing Material Information

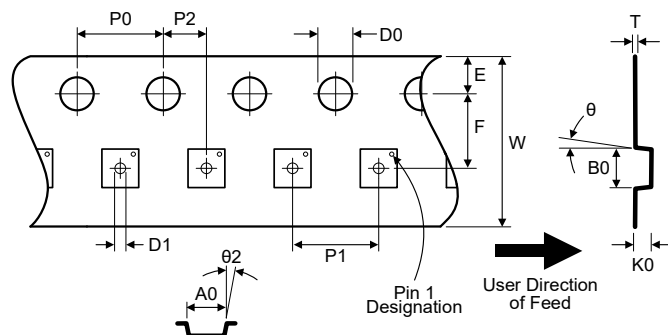
Reel Dimensions



Dimension	mm		
	Min.	Typ.	Max.
A	176	178	180
C	12.8	13.0	13.5
W1	8.4	8.4	9.9
W2	—	—	14.4

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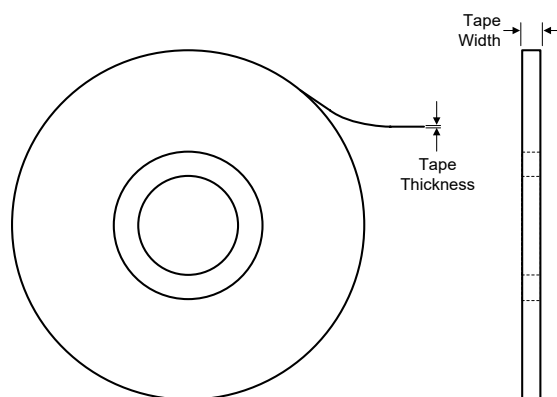
Carrier Tape Dimensions



Dimension	mm		
	Min.	Typ.	Max.
A0	1.66	1.71	1.76
B0	1.76	1.81	1.86
K0	0.655	0.705	0.755
P0	3.90	4.00	4.10
P1	3.90	4.00	4.10
P2	1.95	2.00	2.05
D0	1.50	1.55	1.60
D1	0.45	0.50	0.55
E	1.65	1.75	1.85
F	3.45	3.50	3.55
10P0	39.80	40.00	40.20
W	7.90	8.00	8.30
T	0.18	0.20	0.22
θ	0°		5°
θ2	0°		5°

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Cover Tape Dimensions



Dimensions	Dimension	mm		
		Min.	Typ.	Max.
8mm	Tape Thickness	0.04	0.05	0.06
	Tape Width	5.2	—	5.5

DWG-0042-02

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