MachXO4 Development Board

User Guide

FPGA-EB-02073 Version 1.1

April 2026

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

Contents 3
Abbreviations in This Document 6
1. Introduction 7
1.1. MachXO4 Development Board 7
1.2. Features 8
1.3. MachXO4 Device 8
1.4. L-ASC10 Device 9
2. Applying Power to the Board 10
3. JTAG/I2C Programming 12
3.1. JTAG Download Interface 12
3.2. I2C Download Interface 14
3.3. Alternate JTAG Download Interface 14
3.4. JTAG to MSPI Pass-through Interface 15
3.5. Other JTAG Configuration Pins 15
4. MachXO4 Device Clock Sources 16
5. Headers and Test Connections 17
5.1. Versa Headers 17
5.2. Arduino Board GPIO Headers 19
5.3. FX12 Headers (DNI) 20
5.4. Aardvark Header (DNI) 23
5.5. Raspberry Pi Board GPIO Header 24
6. I2C and SPI Buses 25
6.1. I2C Topology 25
6.2. SPI Topology 27
6.2.1. SPI Configuration 27
6.2.2. SPI Flash Access 27
7. LEDs and Switches 28
7.1. Four-Position DIP Switches 28
7.2. General-Purpose Push Buttons 29
7.3. General-Purpose LEDs 29
7.4. Seven-Segment Display 30
7.5. LVDS Output Pins 31
7.6. General-Purpose DDR Outputs 31
8. ASC Connections 32
8.1. ASC Interface 32
8.2. ASC Voltage Monitor 32
8.3. ASC Current Monitor 33
8.4. ASC Temperature Monitor 34
8.5. ASC LEDs 35
8.6. ASC HVOUT and Trim Pins 35
9. Software Requirements 36
10. Storage and Handling 36
11. Ordering Information 36
Appendix A. MachXO4 Development Board Schematics 37
Appendix B. MachXO4 Development Board Bill of Materials 47
Appendix C. User Defined Constraint File 53
References 57
Technical Support Assistance 58
Revision History 59

Figures

Figure 1.1. Top View of MachXO4 Development Board 7
Figure 1.2. Bottom View of MachXO4 Development Board 8
Figure 2.1. Board Power Supply 10
Figure 3.1. JTAG/I2C Programming Architecture 12
Figure 3.2. Starting Programmer 12
Figure 3.3. Device Selection in Lattice Radiant Programmer 13
Figure 3.4. Bit file programming 13
Figure 3.5. Program the device 14
Figure 3.6. Lattice Radiant Programmer Output Window 14
Figure 4.1. Optional Clock Circuit Design 16
Figure 5.1. Aardvark SS Pin Connections 23
Figure 6.1. I2C Topology 25
Figure 6.2. I2C MUX Circuits 26
Figure 7.1. Four-Position DIP Switch Circuits 28
Figure 7.2. Four-Position DIP Switch Photograph 28
Figure 7.3. Push Button SW5 Circuit Design 29
Figure 7.4. Board LEDs 30
Figure 8.1. POT Circuit Design for VMON7 33
Figure 8.2. POT Wiper Description 33
Figure 8.3. VCC Core Current Monitoring Circuit 34
Figure 8.4. PNP Temperature Sensor Circuit 34
Figure 8.5. NPN Temperature Sensor Circuit 34
Figure 8.6. ASC LEDs 35
Figure A.1. Title Page 37
Figure A.2. Block Diagram 38
Figure A.3. USB to JTAG I/F 39
Figure A.4. VERSA Headers (BANK0) 40
Figure A.5. Arduino Headers (BANK1) 41
Figure A.6. CrossLink Headers (BANK2) 42
Figure A.7. Raspberry Pi Header and Others (BANK3, BANK4, BANK5) 43
Figure A.8. Analog Sense and Control 44
Figure A.9. Power Decoupling and LEDs 45
Figure A.10. Power Regulators 46

Tables

Table 2.1. 5 V Sources and Connections 10
Table 2.2. MachXO4 Power Rail Options 11
Table 2.3. ASC Power Connections 11
Table 3.1. JTAG Connections 14
Table 3.2. Other JTAG Signals 15
Table 4.1. JTAG Connections 16
Table 5.1. Versa X2 Header Pin Connections 17
Table 5.2. Versa X3 Header Pin Connections 18
Table 5.3. Arduino J2 Pin Connections 19
Table 5.4. Arduino J3 Pin Connections 19
Table 5.5. Arduino J4 Pin Connections 20
Table 5.6. Arduino J5 Pin Connections 20
Table 5.7. FX12 U4 Header Pin Connections 20
Table 5.8. FX12 U5 Header Pin Connections 21
Table 5.9. Aardvark JP2 Header Pin Connections 23
Table 5.10. Raspberry Pi JP3 Header Pin Connections 24
Table 6.1. I2C MUX Function 25
Table 6.2. I2C Global Bus Connections 26
Table 6.3. MachXO4 SPI Connections 27
Table 6.4. MachXO4 SPI Configuration Options 27
Table 7.1. Four-Position DIP Switch Signals 28
Table 7.2. Push Button Switch Signals 29
Table 7.3. LED Signals 29
Table 7.4. 7 Segment Signals 30
Table 7.5. LVDS Test Points 31
Table 7.6. GDDR Test Points 31
Table 8.1. ASC to MachXO4 Connections 32
Table 8.2. ASC VMON Connections 32
Table 8.3. ASC IMON Connections 33
Table 8.4. ASC TMON Connections 34
Table 8.5. GPIO LED Connections 35
Table 8.6. ASC HVOUT and Trim Connections 35
Table 11.1 Ordering Information 36

Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
ASC	Analog Sense and Control
ASC-I/F	ASC Interface
CMOS	Complementary Metal-Oxide Semiconductor
CPLD	Complex Programmable Logic Device
DDR	Double Data Rate
DI	Do Install
DNI	Do Not Install
DIP	Dual-In-Line Package (Switch)
ESD	Electrostatic Discharge
GDDR	Graphics Double Data Rate
GPIO	General Purpose Input/Output
I/F	Interface
I2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LDO	Low Dropout Regulator
LVDS	Low-Voltage Differential Signaling
MUX	Multiplexer
OSC	Oscillator
PB	Push Button
POT	Potentiometer
SPI	Serial Peripheral Interface
WP	Write Protect

1. Introduction

The Lattice MachXO4™ Development Board allows you to evaluate and explore the features of the MachXO4 Field Programmable Gate Array (FPGA).The MachXO4 Development Board helps you prototype and test your designs quickly.

The MachXO4 Development Board is part of the MachXO4 Development Kit, which includes:

- MachXO4 Development Board (preloaded with a demo design)
- Mini USB cable
- Quick Start Guide

Key Features:

- Supports rapid prototyping and design validation
- Enables you to explore the MachXO4 devices capabilities

This user guide provides top-level functional descriptions of the MachXO4 Development Board, descriptions of the onboard headers, diodes, and switches, and a complete set of schematics.

1.1. MachXO4 Development Board

The MachXO4 Development Board features an L-ASC10 device that lets you evaluate hardware-management designs and expand the usability of the LFMXO4-110HC device through Arduino, Raspberry Pi, FX12, Versa, and Aardvark™ headers. Figure 1.1 shows the top view of the MachXO4 Development Board, and Figure 1.2 shows the bottom view of the board.

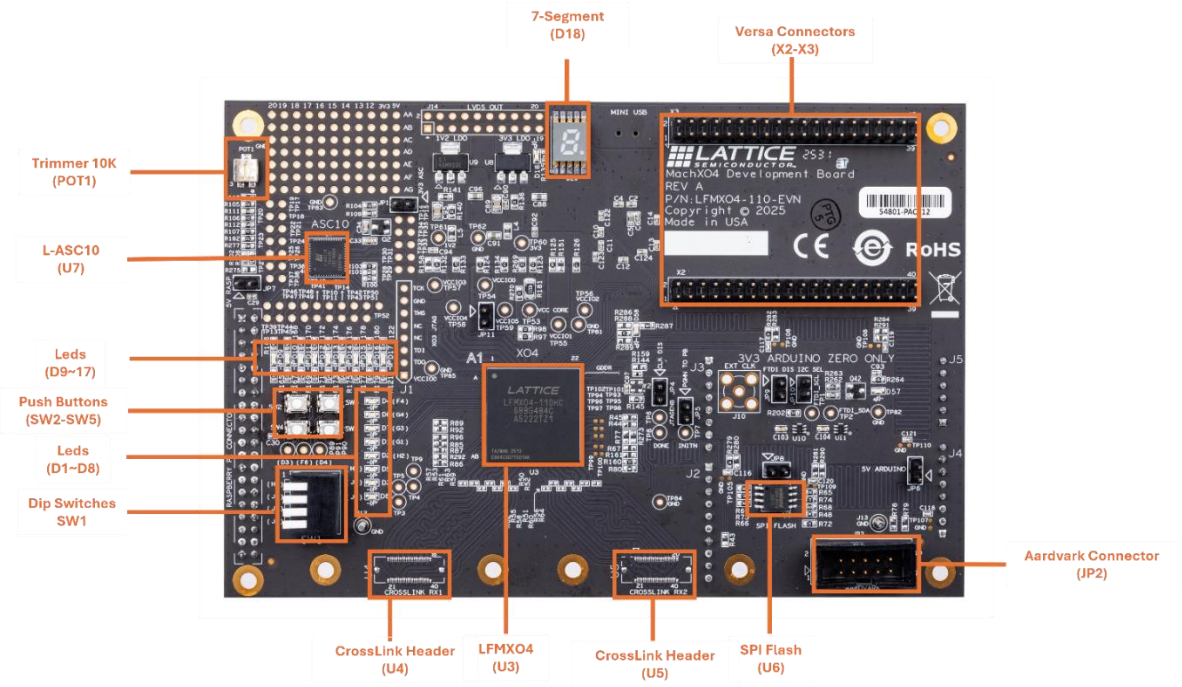

Figure 1.1. Top View of MachXO4 Development Board

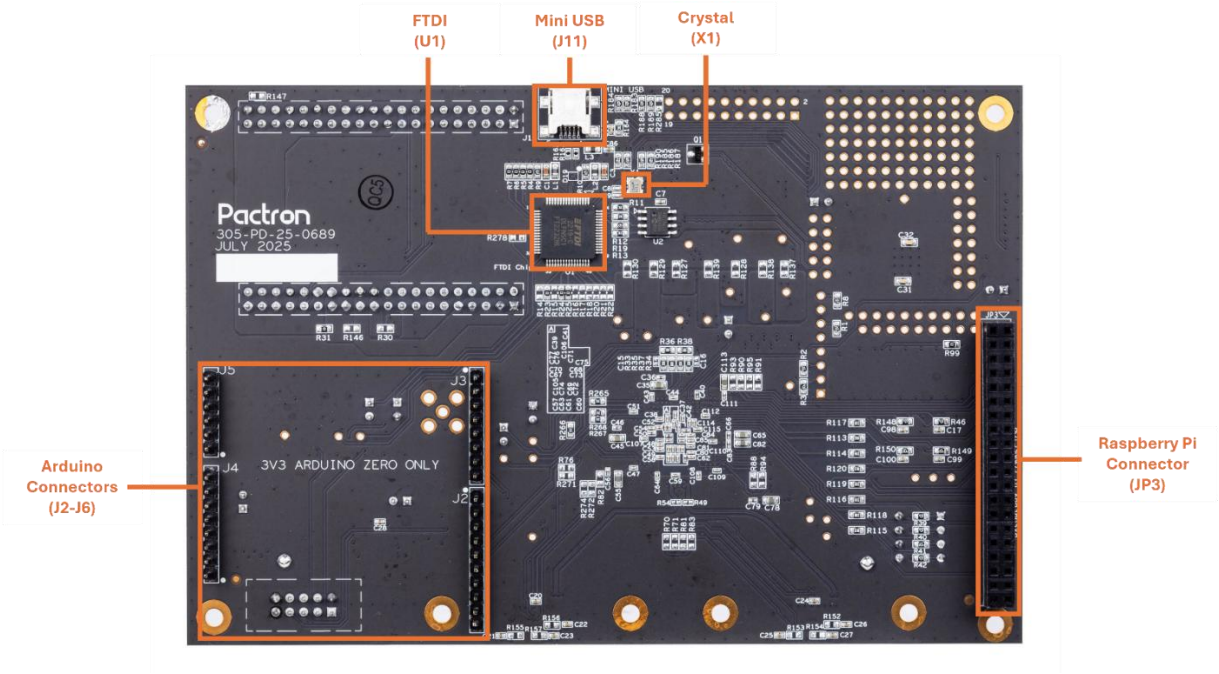

Figure 1.2. Bottom View of MachXO4 Development Board

1.2. Features

- LFMXO4-110HC demonstrates hardware design capabilities and supports expandability
- General-purpose input/output (GPIO) interface for connecting to Arduino and Raspberry Pi boards
- USB-B port for device programming and Inter-Integrated Circuit (I2C) communication
- Onboard boot flash – 16 Mbit Serial Peripheral Interface (SPI) flash with quad-read support
- 4-position DIP switches, 4 push buttons, and 16 LEDs for demonstration
- Lattice Radiant™ programming support
- Multiple reference clock sources
- Two Hirose FX12-40 header positions (DNI)
- Aardvark header (DNI)

Note: DNI stands for ***Do NOT Install***, and DI stands for ***Do Install*** parts for assembly.

Caution: The MachXO4 Development Board contains ESD-sensitive components. Follow ESD-safe practices when handling and using the Development Board.

1.3. MachXO4 Device

The MachXO4 Development Board features the LFMXO4-110HC in a 484-ball caBGA package. It has 9,400 LUTs and 432 kbits of embedded block RAM. The device offers multiple features and programmable options that you can configure. For more information on MachXO4 device capabilities, refer to the MachXO4 Family Data Sheet (FPGA-DS-02125).

1.4. L-ASC10 Device

The L-ASC10 (also referred to as ASC) is a hardware-management expander (power, thermal, and control-plane management) for use with Platform Manager 2, MachXO2, and MachXO4 FPGAs to implement hardware-management control on a circuit board. The L-ASC10 enables scalable power supply voltage and current monitoring, temperature monitoring, and sequence and margin control channels. ASC includes dedicated interfaces for exchanging monitor signal status and output control signals with centralized hardware management controllers. For more information on the capabilities of the ASC device, see the L-ASC10 In System Programmable Hardware Management Expander Data Sheet (FPGA-DS-02038).

2. Applying Power to the Board

The MachXO4 Development Board is powered using onboard low-dropout (LDO) regulators that are supplied by an external 5 V supply, as shown in Figure 2.1. The 5 V supply can come from the USB port (J11) and be routed to multiple onboard headers as listed in Table 2.1. Install a zero-ohm resistor or jumper to connect the 5 V supply path to the headers before you apply power to the mated board, as outlined in Table 2.1.

Table 2.1. 5 V Sources and Connections

Header (Reference)	5 V Power Pins	5 V Power Path (Assembly)
USB header (J11)	1	L3 (DI)
FX12 header 1 (U4)	23, 38	R153 (DNI)
FX12 header 2 (U5)	23, 38	R155 (DNI)
Aardvark header (JP2)	4, 6	R78(DNI), R79 (DNI)
Arduino header (J4)	5	JP6 (DNI)
Raspberry Pi header (JP3)	2, 4	JP7 (DNI)
Versa header (X2)	21	R30 (DNI)

Warning: Avoid power conflicts when the 5 V supply path is enabled between the MachXO4 Development Board and the mated board. Do not apply 5 V power from both boards if you have manually jumper the path.

Alternatively, you can supply 5 V power from onboard headers if J11 is not connected to a USB cable. Header power can power the LDOs and other mated boards.

In addition to the 3.3 V LDO (U8), which is the default power source for the MachXO4 device (U3), the board includes an additional LDO footprint (U9) for lower-power applications. For example, you can use the TLV1117LV12DCY to supply 1.2 V V_{CCIO}. Other SOT-223-compatible LDOs from 1.2 V to 3.3 V are also supported. V_{CCIO1} (Bank 1) and V_{CCIO3} (Bank 3) can also be supplied from mated boards. Use 3.3 V to better align GPIO voltages.

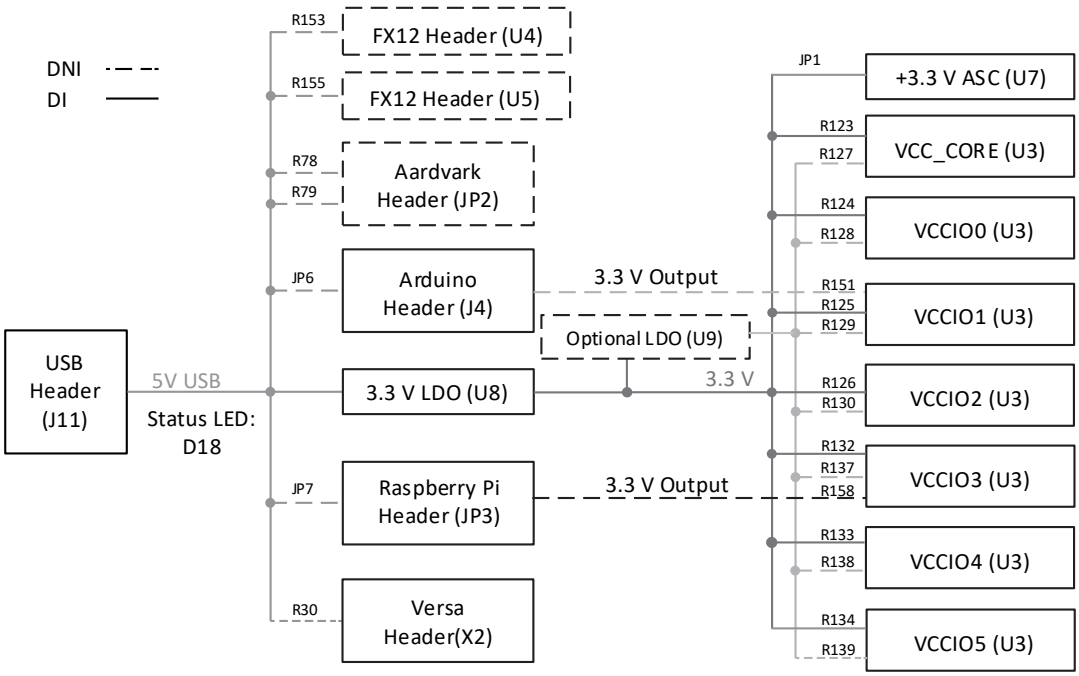

Figure 2.1. Board Power Supply

Table 2.2. MachXO4 Power Rail Options

MachXO4 Device Power (U3)	3.3 V Option (Assembly)	1.2V – 3.3 V Option (Assembly)	Mated Board Option (Assembly)
V_{CC} Core	R123 (DI)	R127 (DNI)[1]	NA
V_{CCIO0}	R124 (DI)	R128 (DNI)	NA
V_{CCIO1}	R125 (DI)	R129 (DNI)	R151 (DNI) for Arduino
V_{CCIO2}	R126 (DI)	R130 (DNI)	NA
V_{CCIO3}	R132 (DI)	R137 (DNI)	R158 (DNI) for Raspberry Pi
V_{CCIO4}	R133 (DI)	R138 (DNI)	NA
V_{CCIO5}	R134 (DI)	R139 (DNI)	NA

Note:

1. R127 applies only when the U9 is set to 2.5 V – 3.3 V for the LFMXO4-110HC device.

Warning: Enable only one option for each MachXO4 device power rail.

The ASC device (U7) draws power only from the 3.3 V LDO only. Install a jumper (JP1) to provide power; it also serve as a test point for measuring the current drawn by the ASC.

Table 2.3. ASC Power Connections

ASC Power	ASC Power Pins	ASC Power Isolation (Assembly)
3.3 V VCC	8, 33 of U7	JP1 (DI)

3. JTAG/I2C Programming

The JTAG/I2C programming architecture of the MachXO4 Development Board is shown in Figure 3.1.

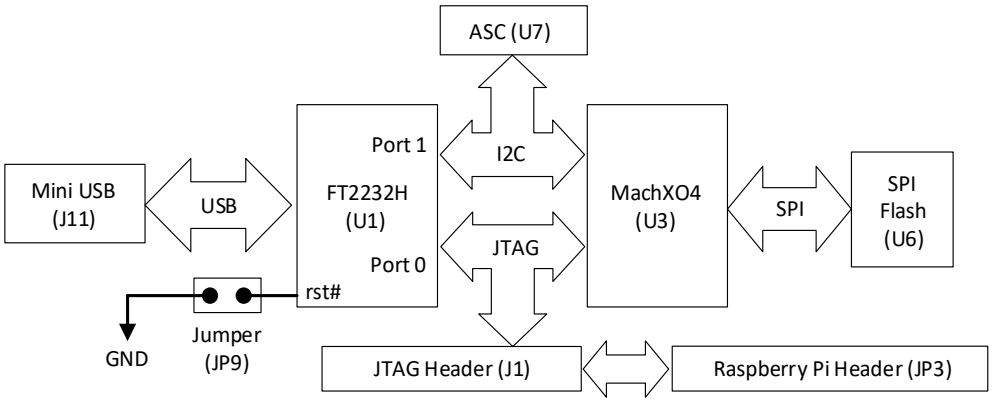

Figure 3.1. JTAG/I2C Programming Architecture

3.1. JTAG Download Interface

The MachXO4 Development Board includes a built-in download controller for programming the MachXO4 device. It uses an FT2232H chip from Future Technology Devices International (FTDI) to convert USB signals to JTAG. To program the MachXO4 device using the JTAG download interface, follow these steps:

1. Connect a USB cable from connector J11 to your PC, and ensure that Lattice Radiant is installed.
2. Use the included Mini-USB–to–USB-A cable provided with the MachXO4 Development Kit.
3. Verify that your PC's USB hub detects the cable on Port 0, making it available for use with the Lattice Radiant Programmer 2025.2 or later. See Figure 3.2.

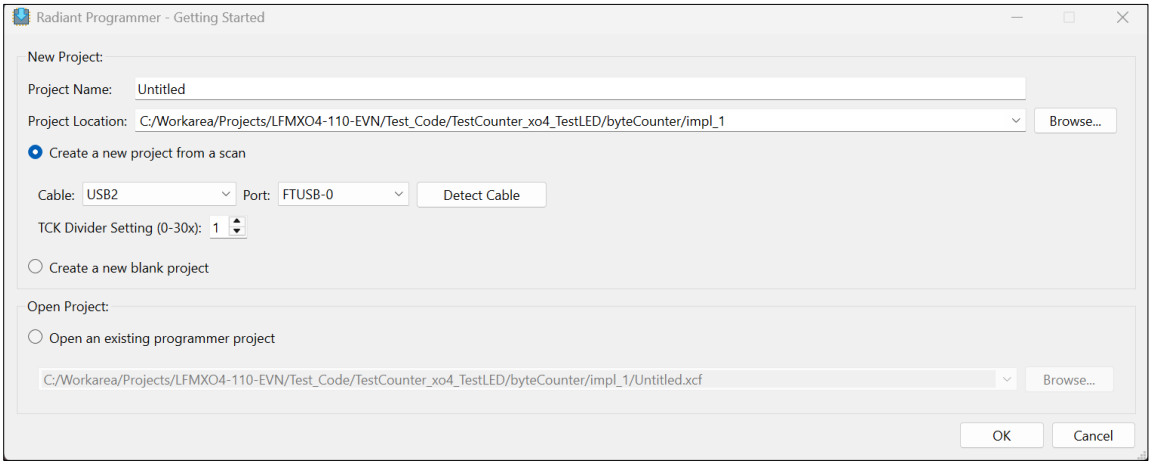

Figure 3.2. Starting Programmer

4. Once the board is scanned, the window shown in Figure 3.3 appears.

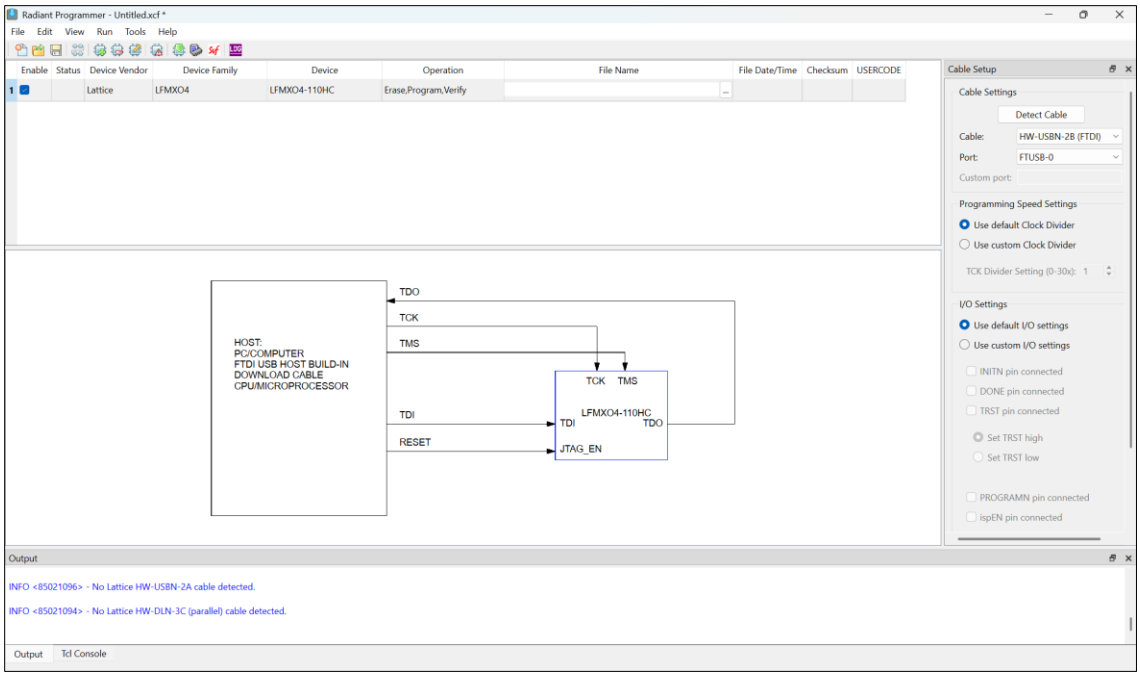

Figure 3.3. Device Selection in Lattice Radiant Programmer

5. Double-click the **Operation** field, then select the appropriate programming mode. For example, select **Non-Volatile Configuration Memory (FLASH)**. See Figure 3.4.

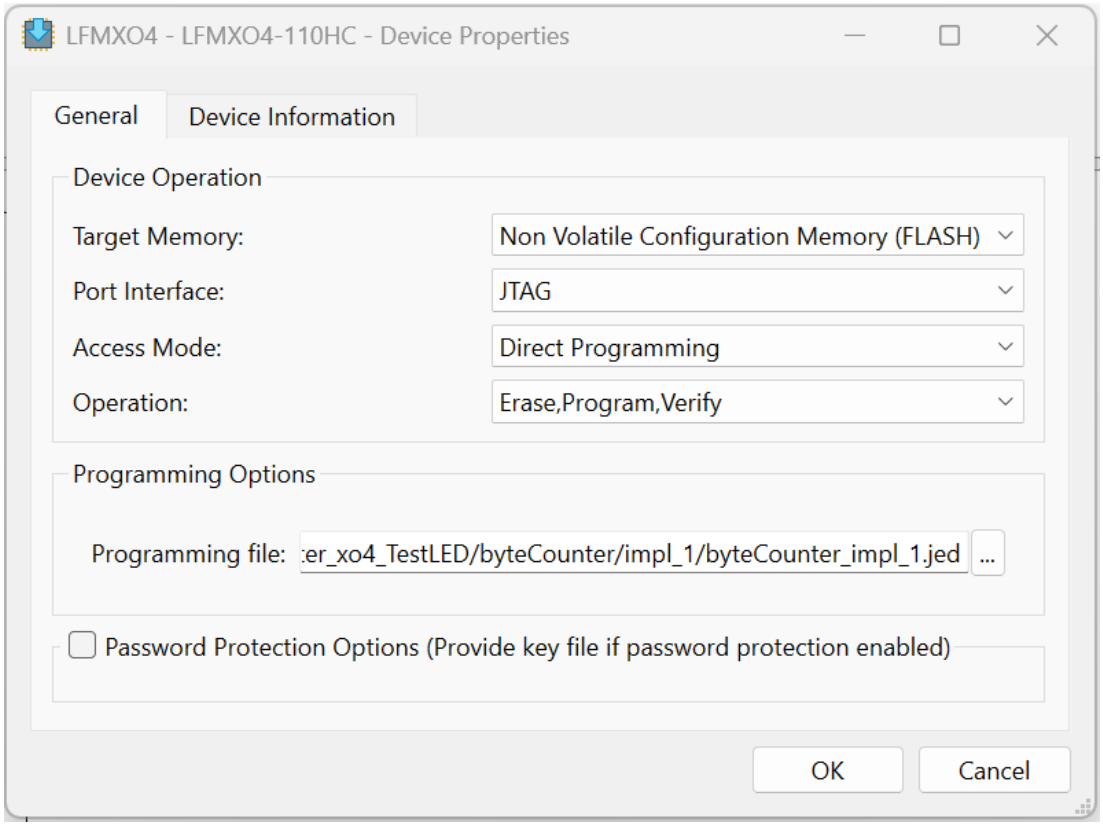

Figure 3.4. Bit file programming

6. Press **OK**, then click **Program Device** in the Programmer to complete programing. See Figure 3.5.

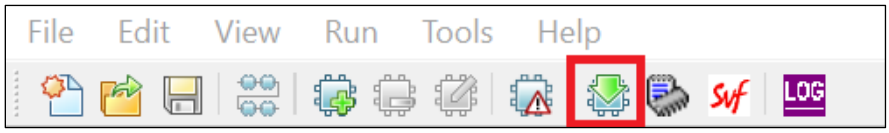

Figure 3.5. Program the device

7. Check the output console at the bottom of the Lattice Radiant Programmer for the programming results. You should see **Operation: Successful**. See Figure 3.6.

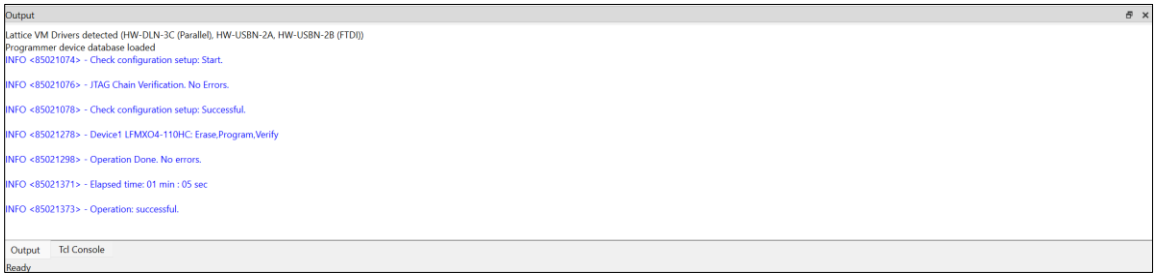

Figure 3.6. Lattice Radiant Programmer Output Window

3.2. I2C Download Interface

Your PC's USB hub detects the USB interface on Port 1. In the Programmer, select port FTUSB-1 and enable the I2C MUX path from the FTDI device to the I2C bus. To do this, install jumper JP10 (the red D57 LED turns on). You can also configure the MachXO4 device and ASC over the I2C interface.

3.3. Alternate JTAG Download Interface

J1 is an 8-pin standalone JTAG header for use with an external Lattice USB download cable (sold separately) when you disable the FTDI interface in the JTAG chain by installing jumper JP9. Attach the USB download cable to J1 to connect to the MachXO4 Development Board. For connection details, refer to the Programming Cables User Guide (FPGA-UG-02042).

J1 can also be used as a test point when USB-to-JTAG is active. Additionally, you can enable JTAG access through the Raspberry Pi header (JP3) for custom applications. To do this, connect JP3 to J1 through the onboard resistors. The JTAG connections between J1 and JP3 are listed in Table 3.1.

Table 3.1. JTAG Connections

J1 Pin Number	JTAG Signal Name	MachXO4 Ball Location for JTAG	JP3 Pin Number	J1 to JP3 Isolation (Assembly)	Raspberry Pi GPIO
1	VCCIO0	—	—	—	—
2	TDO	E8	10	R90 (DNI)	IO15
3	TDI	E9	11	R93 (DNI)	IO17
4	—	—	—	—	—
5	—	—	—	—	—
6	TMS	C10	12	R91 (DNI)	IO18
7	GND	—	—	—	—
8	TCK	D10	8	R95 (DNI)	IO14

3.4. JTAG to MSPI Pass-through Interface

The download controller can also be used to access the JTAG-to-MSPI pass-through circuit, which lets you erase, program, and read the target SPI flash using the Lattice Radiant Programmer.

3.5. Other JTAG Configuration Pins

The MachXO4 Development Board provides test points for other JTAG configuration pins, as shown in Table 3.2.

Table 3.2. Other JTAG Signals

Signal Name	MachXO4 Ball Location	Test Point
JTAGENB	E14	TP6
PROGRAMN	E15	Pin 1 of JP5
INITN	F16	TP7
DONE	E17	TP8

For more information on the MachXO4 JTAG/ I2C programming, refer to the MachXO4 Programming and Configuration User Guide (FPGA-TN-02393).

4. MachXO4 Device Clock Sources

The MachXO4 Development Board provides four clock sources:

- 12 MHz from U1
- 8 MHz from U7
- A user-defined frequency through the Y2 (DNI) oscillator footprint
- An off-board clock source through J10 (DNI)

The FT2232H (FTDI) provides another 12 MHz source. To use it, install JP11 to connect the 12 MHz clock to the MachXO4 I/O. To enable U1, do not install JP9.

Table 4.1. JTAG Connections

Clock Frequency	Signal Name	MachXO4 Ball Location	Clock Source	Comments
8 MHz	ASC_CLK	L1	U7	JP1 installed; test point TP14
12 MHz	12MHz	B10	U1	JP11 installed; JP9 removed
User defined	OSC_IN	D22	Y2 (DNI)	JP4 removed, and OSC_EN signal (MachXO4 ball L20) logic 1.
User defined	OSC_IN	D22	J10 (DNI)	Y2 not installed, or OSC_EN signal (MachXO4 ball L20) logic 0, or JP4 installed.

Additional information on optional clock sources:

- The board provides optional clock inputs for the MachXO4 device from either the oscillator footprint (Y2) or the SMA header (J10), as shown in Figure 4.1. Both are DNI (unpopulated).
- Install Y2 (user installed) in a 2.5 mm × 2.0 mm, 4-pad SMD package. Use an Abracon Ultra Miniature Pure Silicon™ ASDMB-series oscillator for compatibility. Use JP4 to disable the Y2 output by pulling OSC_EN low; the MachXO4 L20 pin can also control OSC_EN.
- Install J10, then connect a CMOS-compatible clock through an SMA cable.

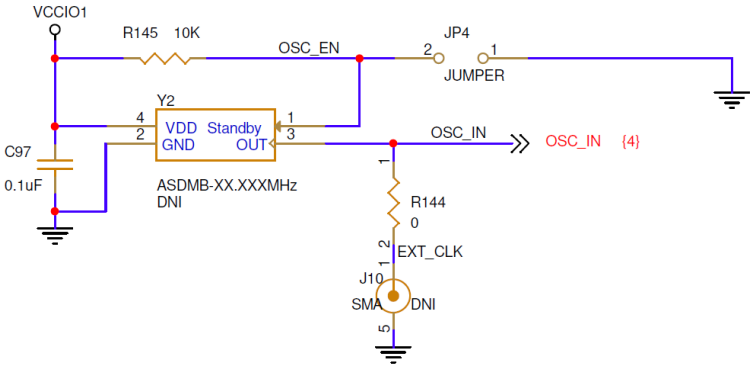

Figure 4.1. Optional Clock Circuit Design

5. Headers and Test Connections

This section describes the headers and test connections on the MachXO4 Development Board.

5.1. Versa Headers

The board provides two pin headers, X2 and X3, for expansion purposes.

Table 5.1. Versa X2 Header Pin Connections

X2 Pin Number	Signal Name	MachXO4 Ball Location
1	GND	—
2	NC	—
3	EXPCON_2V5[1]	—
4	EXPCON_IO29	E12
5	EXPCON_IO30	D14
6	EXPCON_IO31	C15
7	EXPCON_IO32	C17
8	EXPCON_IO33	D15
9	EXPCON_IO34	C18
10	EXPCON_IO35	D16
11	EXPCON_IO36	C19
12	EXPCON_IO37	D17
13	EXPCON_IO38	D18
14	EXPCON_IO39	C20
15	EXPCON_IO40	E16
16	EXPCON_IO41	E13
17	EXPCON_IO42	F13
18	EXPCON_IO43	F15
19	EXPCON_IO44	G15
20	EXPCON_IO45	G12
21	5VIN[1]	—
22	GND	—
23	EXPCON_2V5[1]	—
24	GND	—
25	VCCIO0	—
26	GND	—
27	VCCIO0	—
28	GND	—
29	EXPCON_OSC[1]	—
30	GND	—
31	EXPCON_CLKIN	A10
32	GND	—
33	EXPCON_CLKOUT	A21
34	GND	—
35	EXPCON_3V3[2]	—
36	GND	—
37	EXPCON_3V3[2]	—
38	GND	—

X2 Pin Number	Signal Name	MachXO4 Ball Location
39	EXPCON_3V3[2]	—
40	GND	—

Notes:

1. The signal is optionally connected to the power source through a resistor designated as DNI.
2. The signal is optionally connected to the power source through a resistor designated as DN.

Table 5.2. Versa X3 Header Pin Connections

X3 Pin Number	Signal Name	MachXO4 Ball Location
1	HPE_RESOUT#	G9
2	GND	—
3	EXPCON_IO0	F8
4	EXPCON_IO1	G8
5	EXPCON_IO2	F9
6	EXPCON_IO3	F7
7	EXPCON_IO4	E7
8	EXPCON_IO5	E6
9	EXPCON_IO6	D5
10	EXPCON_IO7	C3
11	EXPCON_IO8	D6
12	EXPCON_IO9	C4
13	EXPCON_IO10	F10
14	EXPCON_IO11	C5
15	EXPCON_IO12	C6
16	EXPCON_IO13	B12
17	EXPCON_IO14	D7
18	EXPCON_IO15	A12
19	GND	—
20	EXPCON_3V3[2]	—
21	EXPCON_IO16	D8
22	GND	—
23	EXPCON_IO17	C8
24	GND	—
25	EXPCON_IO18	D9
26	GND	—
27	EXPCON_IO19	E10
28	EXPCON_IO20	C9
29	EXPCON_IO21	G11
30	GND	—
31	EXPCON_IO22	E11
32	EXPCON_IO23	D11
33	EXPCON_IO24	F11
34	GND	—
35	EXPCON_IO25	D12
36	EXPCON_IO26	F12
37	EXPCON_IO27	D13
38	CARDSEL#[1]	—

X3 Pin Number	Signal Name	MachXO4 Ball Location
39	EXPCON_IO28	C14
40	GND	—

Notes:

1. The signal is optionally connected to the power source through a resistor designated as DNI.
2. The signal is optionally connected to the power source through a resistor designated as DN.

5.2. Arduino Board GPIO Headers

The board provides four headers. Headers J2, J3, J4, and J5 are used for Arduino Zero board adaptation.

Table 5.3. Arduino J2 Pin Connections

J2 Pin Number	Signal Name	Arduino ZERO Board Signal	MachXO4 Ball Location	Comments
1	AR_IO8	8	U21	—
2	AR_IO9	9	U22	—
3	AR_SS_IO10	10	W20	An Optional connection to SS through R67 for SPI access; DNI by default.
4	AR_MOSI_IO11	11	V18	An Optional connection to SISPI through R82 for SPI access; DNI by default.
5	AR_MISO_IO12	12	G16	An Optional connection to SPISO through R77 for SPI access; DNI by default.
6	AR_SCK_IO13	13	F17	An Optional connection to MCLK through R76 for SPI access,; DNI by default.
7	GND	GND	—	—
8	AR_AREF	AREF	U17	AR_AREF connection to AREF through R43; DNI by default.
9	AR_SDA	SDA	U19	An Optional connection to SDA0 through R44; DNI by default.
10	AR_SCL	SCL	U18	An Optional connection to SCL0 through R45; DNI by default.

Table 5.4. Arduino J3 Pin Connections

J3 Pin Number	Signal Name	Arduino ZERO Board Signal	MachXO4 Ball Location	Comments
1	AR_IO0	RX / 0	G19	—
2	AR_IO1	TX / 1	G20	—
3	AR_IO2	2	G21	—
4	AR_IO3	3	H20	—
5	AR_IO4	4	G18	—
6	AR_IO5	5	L21	—
7	AR_IO6	6	W22	—
8	AR_IO7	7	V22	—
9	AR_SDA	SDA	U19	—
10	AR_SCL	SCL	U18	—

Table 5.5. Arduino J4 Pin Connections

J4 Pin Number	Signal Name	Arduino ZERO Board Signal	MachXO4 Ball Location	Comments
1	AR_IO14	ATN	T17	—
2	NC	IOREF	—	—
3	AR_RESET	RESET	U20	Pin U20 should be set high by default to prevent the Arduino Zero board from entering a reset state when connected.
4	+3.3V_AR	3.3 V	—	3.3 V power supply from the Arduino Zero board.
5	AR_5V	5 V	—	Jumper to the 5 V main power through JP6.
6	GND	GND	—	—
7	GND	GND	—	—
8	+12V	VIN	—	12 V power supply from the Arduino Zero board.

Table 5.6. Arduino J5 Pin Connections

J5 Pin Number	Signal Name	Arduino ZERO Board Signal	MachXO4 Ball Location	Comments
1	AR_AD0	A0	P19	Used as a GPIO in digital mode.
2	AR_AD1	A1	P18	Used as a GPIO in digital mode.
3	AR_AD2	A2	P17	Used as a GPIO in digital mode.
4	AR_AD3	A3	P16	Used as a GPIO in digital mode.
5	AR_AD4	A4	K22	Used as a GPIO in digital mode.
6	AR_AD5	A5	G17	Used as a GPIO in digital mode.

Note: If JP6 is installed, 5 V power can be supplied from either the Arduino board or the MachXO4 Development Board. If JP6 is not removed, both boards require their own 5 V power sources.

5.3. FX12 Headers (DNI)

The board provides two headers—U4 and U5—for connecting to FX12-compatible boards or cables. Each header has eight pairs of Low-Voltage Differential Signaling (LVDS) signals for high-speed data reception.

Table 5.7. FX12 U4 Header Pin Connections

U4 Pin Number	Signal Name	MachXO4 Ball Location
1	CH0_DCK_P	AA10
2	CH0_DCK_N	AB10
3	GND	—
4	CH0_DATA0_P	AA4
5	CH0_DATA0_N	AB4
6	GND	—
7	CH0_DATA2_P	AA5
8	CH0_DATA2_N	AB5
9	GND	—
10	FX_SN[1]	—
11	FX_SCLK[1]	—
12	PWR_12V[2]	—
13	SDA2	AB13

U4 Pin Number	Signal Name	MachXO4 Ball Location
14	SCL2	AA13
15	GND	—
16	CH2_DATA0_P	AA6
17	CH2_DATA0_N	AB6
18	GND	—
19	CH2_DCK_P	AA7
20	CH2_DCK_N	AB7
21	PWR_12V[2]	—
22	RESETN	AB3
23	PWR_5-0V[1]	—
24	CH0_DATA1_P	AA2
25	CH0_DATA1_N	AB2
26	PWR_3-3V[1]	—
27	CH0_DATA3_P	AA8
28	CH0_DATA3_N	AB8
29	PWR_1-8V[1]	—
30	FX_MOSI[1]	—
31	FX_MISO[1]	—
32	PWR_1-8V[1]	—
33	GND	—
34	GND	—
35	PWR_3-3V[1]	—
36	CH2_DATA1_P	AA9
37	CH2_DATA1_N	AB9
38	PWR_5-0V[1]	–
39	SDA1	AA1
40	SCL1	AB11

Notes:

1. The signal is optionally connected to the power source through a resistor designated as DNI.
2. The 12 V power input requires an external supply provided through pin 8 of J4.

Table 5.8. FX12 U5 Header Pin Connections

U5 Pin Number	Signal Name	MachXO4 Ball Location
1	CH1_DCK_P	AB12
2	CH1_DCK_N	AA12
3	GND	—
4	CH1_DATA0_P	AB16
5	CH1_DATA0_N	AA16
6	GND	-
7	CH1_DATA2_P	AB17
8	CH1_DATA2_N	AA17
9	GND	—
10	FX_SN[1]	—
11	FX_SCLK[1]	—
12	PWR_12V[2]	—

U5 Pin Number	Signal Name	MachXO4 Ball Location
13	SDA2	AB13
14	SCL2	AA13
15	GND	— -
16	CH3_DATA0_P	AB18
17	CH3_DATA0_N	AA18
18	GND	— -
19	CH3_DCK_P	AB19
20	CH3_DCK_N	AA19
21	PWR_12V[2]	— -
22	RESETN	AB3
23	PWR_5-0V[1]	— -
24	CH1_DATA1_P	AB14
25	CH1_DATA1_N	AA14
26	PWR_3-3V[1]	— -
27	CH1_DATA3_P	AB15
28	CH1_DATA3_N	AA15
29	PWR_1-8V	—
30	FX_MOSI[1]	—
31	FX_MISO[1]	—
32	PWR_1-8V[1]	—
33	GND	—
34	GND	- —
35	PWR_3-3V[1]	— -
36	CH3_DATA1_P	AB20
37	CH3_DATA1_N	AA20
38	PWR_5-0V[1]	— -
39	SDA1	AA11
40	SCL1	AB11

Notes:

1. The signal is optionally connected to the power source through a resistor designated as DNI.
2. The 12 V power input requires an external supply provided through pin 8 of J4.

5.4. Aardvark Header (DNI)

The Aardvark I2C/SPI Host Adapter is a high-speed I2C and SPI host adapter that connects through a USB. It lets you interface a Windows, Linux, or Mac OS X computer with a downstream embedded system and transfer serial messages over I2C or SPI protocols.

The MachXO4 Development Board includes an Aardvark-compatible header for your applications. The I2C bus can connect to the board's global I2C bus if JP10 is not installed.

Table 5.9. Aardvark JP2 Header Pin Connections

JP2 Pin Number	Signal Name	MachXO4 Ball Location
1	JP2_SCL	To the I2C analog switch (U10).
2	—	GND
3	JP2_SDA	To the I2C analog switch (U11).
4	+5V_I2C	To VBUS_5V through R78; DNI.
5	SPISO	To the MachXO4 (U9).
6	+5V_SPI	To VBUS_5V through R79 (DNI).
7	MCLK	To the MachXO4 (T9).
8	SISPI	To the MachXO4 (AA21).
9	SS	Multiple options, refer to Figure 5.1.
10	—	—

Caution: V_{CCIO2} must be 3.3 V when you connect it to the Aardvark I2C/SPI Host Adapter.

Pin 9 on the Aardvark header is a chip-select (SS) signal, that can be routed to multiple devices or headers. By default, you can route SS to the MachXO4 device's Target SPI (controller SPI) through R160. You can route SS to the FX12 header, the Raspberry Pi header, and the onboard SPI flash by enabling R161. You can also route SS to the Arduino header by enabling R67.

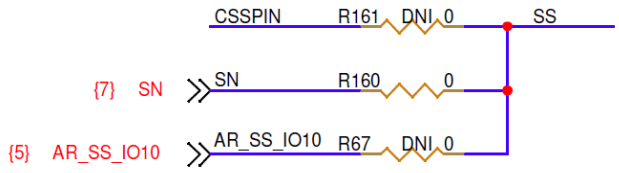

Figure 5.1. Aardvark SS Pin Connections

5.5. Raspberry Pi Board GPIO Header

The MachXO4 Development Board provides a 40-pin receptacle that is compatible with the GPIO header on Raspberry Pi 2/3 series models.

Table 5.10. Raspberry Pi JP3 Header Pin Connections

JP3 Pin Number	Signal Name	MachXO4 Ball Location
1	3.3V_RASP[1]	—
2	RASP_5V[2]	—
3	RASP_IO02	U2
4	RASP_5V[2]	—
5	RASP_IO03	V1
6	GND	—
7	RASP_IO04	T6
8	RASP_IO14	P4
9	GND	—
10	RASP_IO15	N5
11	RASP_IO17	N6
12	RASP_IO18	N7
13	RASP_IO27	P5
14	GND	—
15	RASP_IO22	P6
16	RASP_IO23	R3
17	3.3V_RASP[1]	—
18	RASP_IO24	R4
19	RASP_IO10	R6
20	GND	—
21	RASP_IO09	R7
22	RASP_IO25	R5
23	RASP_IO11	T3
24	RASP_IO08	T4
25	GND	—
26	RASP_IO07	T5
27	RASP_ID_SD	V5
28	RASP_ID_SC	T7
29	RASP_IO05	U3
30	GND	—
31	RASP_IO06	U4
32	RASP_IO12	V4
33	RASP_IO13	U5
34	GND	—
35	RASP_IO19	W3
36	RASP_IO16	W4
37	RASP_IO26	P7
38	RASP_IO20	Y2
39	GND	—
40	RASP_IO21	Y3

Notes:

1. The 3.3 V power input is supplied by the Raspberry Pi board.
2. When JP7 is installed, the 5 V supply can come from either the Raspberry Pi board or the MachXO4 Development Board. When JP7 is not installed, each board requires its own 5 V source.

6. I2C and SPI Buses

This section describes the I2C and SPI topology of the MachXO4 Development Board.

6.1. I2C Topology

The MachXO4 Development Board has a flexible I2C bus to support all optional connectors and devices on the board. The global I2C bus has the signal names SDA0 and SCL0, and these signals are routed near the devices and headers, as shown in Figure 6.1.

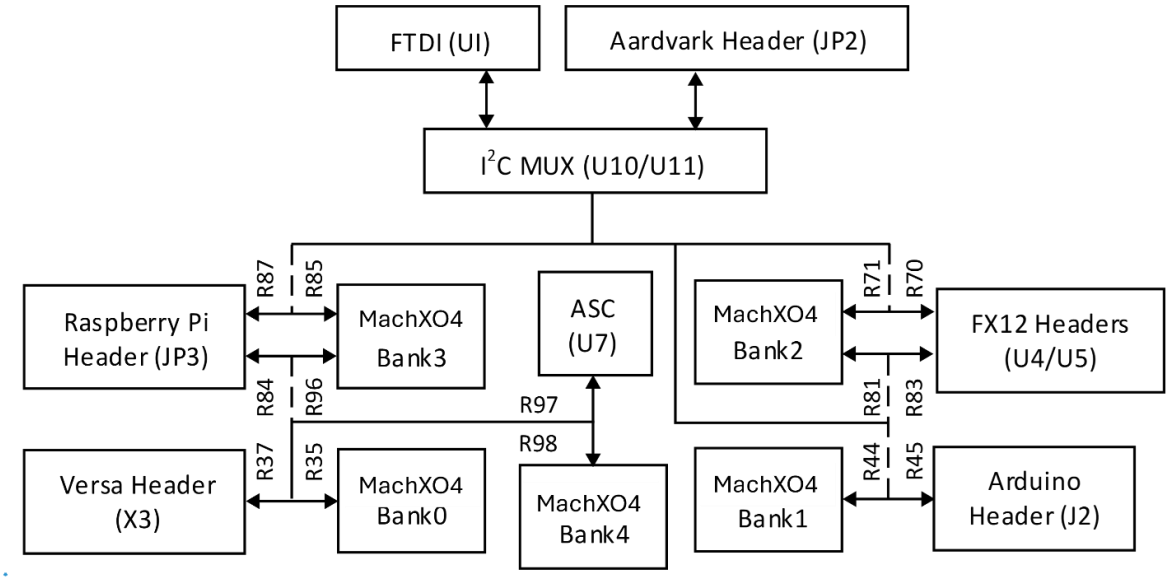

Figure 6.1. I2C Topology

The board provides two options for accessing the global I2C bus from external sources:

- Through the Mini-USB cable (J11) through FTDI (U1)
- Through the Aardvark header (JP2) using an Aardvark cable

Two analog multiplexers (Figure 6.2) are used to select between the USB and Aardvark paths. Both multiplexers are controlled by the signal USB_I2C_EN.

Table 6.1. I2C MUX Function

Global I2C Controller	USB_I2C_EN Logic Level	FSA4157 MUX Function	SCL0 Test Point	SDA0 Test Point
Aardvark Header (JP2)	0 (JP10 removed)	JP2_SCL <> SCL0 JP2_SDA <> SDA0	Pin 1 of JP2	Pin 3 of JP2
USB FTDI (U1)	1 (JP10 installed)	FTDI_SCL <> SCL0 FTDI_SDA <> SDA0	TP1	TP2

When you remove jumper JP10, USB_I2C_EN is low; JP2 (Aardvark header) connects to the global I2C bus. When you install jumper JP10, USB_I2C_EN is high; the USB connector (J11) connects to the global I2C bus through the FTDI device.

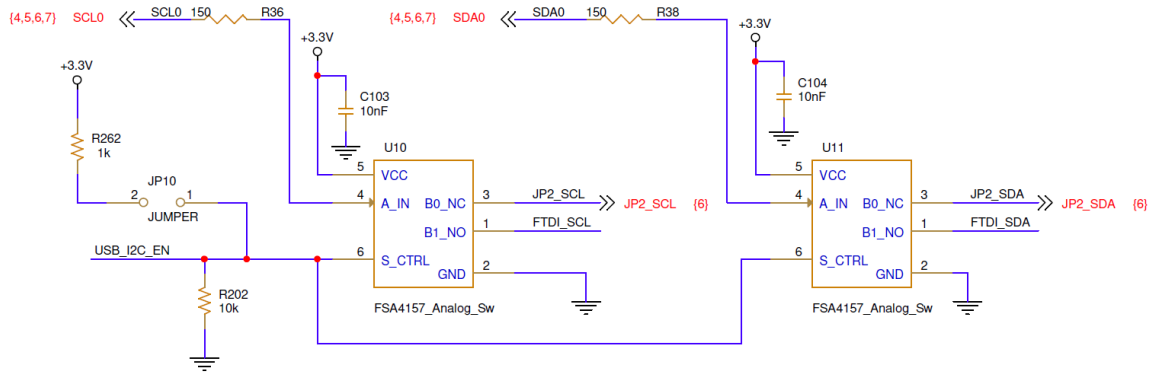

Figure 6.2. I2C MUX Circuits

To support a wide variety of I2C applications, each header or device connects to a dedicated MachXO4 GPIO bank through a local I2C bus. Each local I2C bus may also connect to the global I2C bus through resistors. Table 6.2 summarizes the local I2C connections.

Table 6.2. I2C Global Bus Connections

MachXO4 Bank	Component (Reference)	Header Pin	MachXO4 Ball Location	Local Signal Name (Global I2C Signal)	Resistor
0	Versa header (X3)	18	A12	EXPCON_IO15 (SDA0)	R37 (DI)[1]
		16	B12	EXPCON_IO13 (SCL0)	R35 (DI)[1]
1	Arduino header (J2)	9	U19	AR_SDA (SDA0)	R44 (DNI)
		10	U18	AR_SCL (SCL0)	R45 (DNI)
2	FX12 headers (U4/U5)	39	AA11	SDA1 (SDA0)	R81 (DNI)
		40	AB11	SCL1 (SCL0)	R83 (DNI)
	FX12 headers (U4/U5)	13	AB13	SDA2 (SDA0)	R71 (DNI)
		14	AA13	SCL2 (SCL0)	R70 (DNI)
3	Raspberry Pi header (JP3)	3	T6	RASP_IO02 (SDA0)	R84 (DNI)
		5	V1	RASP_IO03 (SCL0)	R96 (DNI)
		27	V5	RASP_ID_SD (SDA0)	R87 (DNI)
		28	T7	RASP_ID_SC (SCL0)	R85 (DNI)
4	ASC device (U7)	14	K2	I2C_SDA0 (SDA0)	R97 (DI)[1]
		15	K1	I2C_SCL0 (SDA0)	R98 (DI)[1]

Note:

1. Install a resistor to support ASC device programming. Configure balls K1 and K2 as input pins to support ASC device programming. Versa header X3 pins 16 and 18 must be high-impedance to support ASC device programming. Balls B12 and A12 should be used in Platform Manager designs. Balls K1 and K2 provide a connection for a user-instantiated I2C port in a separate system to communicate with the ASC device.

6.2. SPI Topology

6.2.1. SPI Configuration

A primary function of the board's SPI connections is MachXO4 device configuration through the SPI ports. The MachXO4 Development Board supports both Controller SPI (MSPI) and Target SPI (SSPI) modes for configuration.

Table 6.3. MachXO4 SPI Connections

Signal Name	MachXO4 Ball Location	MSPI Mode Direction	SSPI Mode Direction
MCLK	T9	Output	Input
SN	AB21	Input	Input
SISPI	AA21	Output	Input
SPISO	U9	Input	Output
CSSPIN	AA3	Output	Not used

You can configure the MachXO4 device through the ports listed in Table 6.4. By default, the MachXO4 device boots from onboard SPI flash.

Table 6.4. MachXO4 SPI Configuration Options

Controller SPI Device (Reference)	Controller CS (Pin Number of Reference Part)	Target SPI Device (Reference)	Target CS (Pin Number of Reference Part)
MachXO4 (U3)	CSSPIN (AA3)	SPI Flash (U6)	CS# (1)
MachXO4 (U3)	CSSPIN (AA3)	FX12 (U4, U5)	FX_SN (10)
Aardvark (JP2)	SS (9)	MachXO4 (U3)	SN (AB21)
Arduino (J2)	AR_SS_IO10 (3)	MachXO4 (U3)	SN (AB21)
Raspberry Pi (JP3)	Rasp_IO08 (24)	MachXO4 (U3)	SN (AB21)

Note: Use only one Controller SPI (MSPI) and one Target SPI (SSPI) at a time.

For detailed information on Controller SPI and Target SPI mode configuration, refer to the MachXO4 Programming and Configuration User Guide (FPGA-TN-02393).

6.2.2. SPI Flash Access

You can use onboard SPI flash to store the MachXO4 device configuration data in external-boot or dual-boot mode. It can also store user data for certain applications. The MachXO4 device includes a JTAG-to-MSPI pass-through circuit that allows the Target SPI flash to be erased, programmed, and read using the Lattice Radiant Programmer. For details on JTAG-to-MSPI pass-through for Target SPI flash access, refer to the MachXO4 Programming and Configuration User Guide (FPGA-TN-02393).

7. LEDs and Switches

This section describes the LEDs and switches on the MachXO4 Development Board used in demos and your designs.

7.1. Four-Position DIP Switches

Four MachXO4 pins connect to the switches on SW1, as shown in Figure 7.1. The CTS-side-actuated DIP switches are at logic-level low (**0**) when *On*, as shown in Figure 7.2.

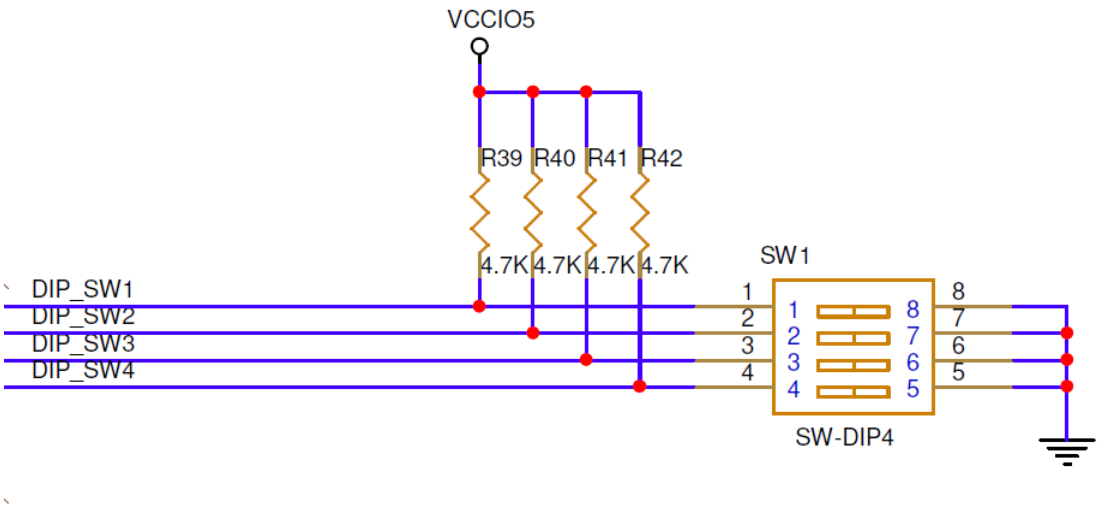

Figure 7.1. Four-Position DIP Switch Circuits

Figure 7.2. Four-Position DIP Switch Photograph

One side of each switch connects to GPIOs in the V_{CCIO5} bank and is pulled up through 4.7 kΩ resistors. The other side connects to ground. Table 7.1 shows the designated pin connections.

Table 7.1. Four-Position DIP Switch Signals

Signal Name	MachXO4 Ball Location	SW1 DIP Switch Position	4.7 kΩ Pull up Resistor	Logic Level at ON Position
DIP_SW1	H5	1	R39	0
DIP_SW2	J5	2	R40	0
DIP_SW3	J4	3	R41	0
DIP_SW4	J3	4	R42	0

7.2. General-Purpose Push Buttons

The MachXO4 Development Board provides four push-button switches—SW2, SW3, SW4, and SW5—for demos and user applications. Pressing these buttons drives a logic-level low (0) on the corresponding I/O pins.

Table 7.2. Push Button Switch Signals

Signal Name	MachXO4 Ball Location	Push Button Reference	Logic Level at Button Pressed
PB1	D3	SW2	0
PB2	D4	SW3	0
PB3	F6	SW4	0
PB4	G7	SW5	0

SW2, SW3, and SW4 are for general-purpose applications; SW5 includes an additional jumper (JP5) as shown in Figure 7.3. SW5 can serve as a PROGRAMN push button when JP5 is configured to trigger reconfiguration without a power cycle. For detailed information about PROGRAMN, refer to the MachXO4 Programming and Configuration User Guide (FPGA-TN-02393).

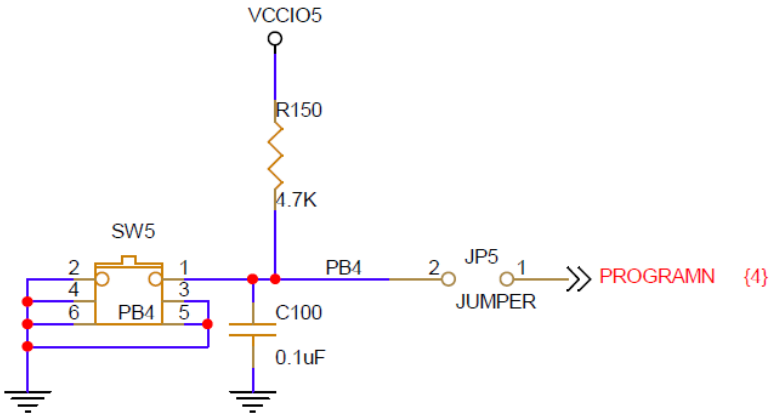

Figure 7.3. Push Button SW5 Circuit Design

7.3. General-Purpose LEDs

The MachXO4 Development Board includes eight red LEDs connected to I/Os in Bank 5. The LEDs are active-low; they turn on when the output is low. Table 7.3 lists the red LEDs and their associated pins.

Table 7.3. LED Signals

Red LEDs	Signal Name	MachXO4 Ball Location	Logic Level to Light
D1	XLED0	G1	0
D2	XLED1	H2	0
D3	XLED2	J2	0
D4	XLED3	F4	0
D5	XLED4	H1	0
D6	XLED5	J1	0
D7	XLED6	G3	0
D8	XLED7	G4	0

Caution: The MachXO4 Development Board contains ESD-sensitive components. Follow ESD-safe practices when handling and using the Development Board.

Note: The LEDs are not lined up in sequence, as shown in Figure 7.4.

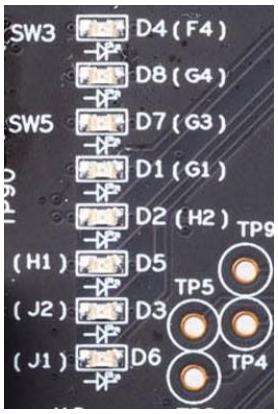

Figure 7.4. Board LEDs

7.4. Seven-Segment Display

The MachXO4 Development Board includes a common-anode, one-digit seven-segment display (D20) connected to I/Os in Bank 5. Table 7.4 lists the seven-segment pin assignments. The seven-segment display is active-low; it turns on when the output is low.

Table 7.4. 7 Segment Signals

Segment	Signal Name	MachXO4 Ball Location	Logic Level to Light
DP	SEG_DP	F1	0
G	SEG_G	E1	0
F	SEG_F	E3	0
E	SEG_E	E2	0
D	SEG_D	D2	0
C	SEG_C	C1	0
B	SEG_B	D1	0
A	SEG_A	G2	0

7.5. LVDS Output Pins

The MachXO4 Development Board includes nine pairs of unused LVDS outputs routed to test points for your applications. Table 7.5 lists the LVDS test points.

Table 7.5. LVDS Test Points

Signal Name	MachXO4 Ball Location	Test Point	Comments
LVDS_OUT0_P	B1	J14.1	LVDS output pair 0
LVDS_OUT0_N	A2	J14.2	
LVDS_OUT1_P	B2	J14.3	LVDS output pair 1
LVDS_OUT1_N	A3	J14.4	
LVDS_OUT3_P	B4	J14.7	LVDS output pair 3
LVDS_OUT3_N	A5	J14.8	
LVDS_OUT4_P	B5	J14.9	LVDS output pair 4
LVDS_OUT4_N	A6	J14.10	
LVDS_OUT5_P	B6	J14.11	LVDS output pair 5
LVDS_OUT5_N	A7	J14.12	
LVDS_OUT6_P	B8	J14.13	LVDS output pair 6
LVDS_OUT6_N	A8	J14.14	
LVDS_OUT7_P	B9	J14.15	LVDS output pair 7
LVDS_OUT7_N	A9	J14.16	
LVDS_OUT8_P	B11	J14.17	LVDS output pair 8
LVDS_OUT8_N	A11	J14.18	

7.6. General-Purpose DDR Outputs

Graphics Double Data Rate (GDDR) signals are routed to test pads for validation testing.

Table 7.6. GDDR Test Points

Signal Name	MachXO4 Ball Location	Test Point
GDDR_DQ0	R22	TP93
GDDR_DQ1	R21	TP94
GDDR_DQ2	T22	TP95
GDDR_DQ3	T21	TP96
GDDR_DQ4	Y22	TP97
GDDR_DQ5	W21	TP98
GDDR_DQ6	AA22	TP99
GDDR_DQ7	Y21	TP100
GDDR_DQS	N22	TP101
GDDR_DQSN	P21	TP102

8. ASC Connections

8.1. ASC Interface

The MachXO4 Development Board provides a dedicated ASC interface (ASC-I/F) between the onboard ASC device and MachXO4 Bank 4. The Platform Manager design in the MachXO4 monitors signal status and controls the output behavior of the ASC through the ASC-I/F. The ASC I2C interface is used by the FPGA, or an external microcontroller perform ASC background programming, configure the interface, and transfer additional data, such as parameter measurements or I/O status control.

Table 8.1. ASC to MachXO4 Connections

ASC Connections	MachXO4 Ball Location	ASC Pins	Description	ASC Breakout Test Point
I2C_SDA0	A12 (K2)	14	I2C data programming (user control)	TP2
I2C_SCL0	B12 (K1)	15	I2C clock programming (user control)	TP1
ASC_ CLK	L1	7	8 MHz clock output from ASC	TP14
ASC_RESETb	L3	43	ASC device reset (active Low)	TP13
ASC_WRCLK	M1	6	ASC-I/F clock signal to ASC	TP12
ASC_RDAT	N1	5	ASC-I/F data signal from ASC	TP11
ASC_WDAT	P1	4	ASC-I/F data signal to ASC	TP10
I2C_WRITE_PROTECT	N2	44	I2C configuration write control signal, when WP[1:0] = 10 in ASC WRITEPROTECT_USERTAG register, pull high to enable overwriting by I^2C instructions.	Share with TP44 for ASC_LED1 if R99 is DI

8.2. ASC Voltage Monitor

ASC Voltage Monitors (VMONs) are connected to various power sources on the board, as listed in Table 8.2.

Table 8.2. ASC VMON Connections

Power Name	ASC Signal Name	ASC Pin Number	ASC Breakout Test Point
+1.2V[2]	ASC_VMON1	26	TP15
GND[1]	ASC_GS_VMON1	25	TP16
VCC1_8FT[2]	ASC_VMON2	28	TP17
GND[1]	ASC_GS_VMON2	27	TP19
+3.3V_RASP[2]	ASC_VMON3	30	TP18
GND[1]	ASC_GS_VMON3	29	TP20
+3.3V_AR[2]	ASC_VMON4	32	TP21
GND[1]	ASC_GS_VMON4	31	TP22
VBUS_5V[2]	ASC_VMON5	34	TP23
—	ASC_VMON6	35	TP24
POT[3]	ASC_VMON7	36	TP25
—	ASC_VMON8	37	TP26
+3.3V_ASC[2]	ASC_VMON9	38	TP27

Notes:

1. Connection to GND is through a 100 Ω resistor (R109 – R112), so that the test point can overdrive the node.
2. Connection to the power supply is through a 270 Ω resistor (R1104 – R108, R182), so that the test point can overdrive the node.
3. Connection to the POT is through a 1 kΩ resistor (R277), so that the test point can overdrive the node.

A 10 kΩ potentiometer is used to provide a 0 V to 3.3 V voltage adjustment to ASC_VMON7, as shown in Figure 8.1.

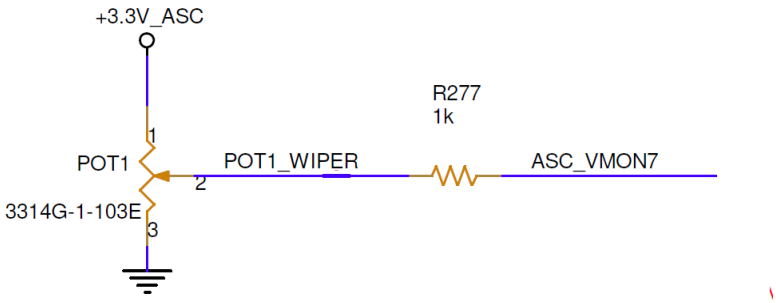

Figure 8.1. POT Circuit Design for VMON7

Rotate the potentiometer clockwise to decrease the voltage, as shown in Figure 8.2. To increase the voltage to VMON7, rotate it counterclockwise.

Figure 8.2. POT Wiper Description

8.3. ASC Current Monitor

One of the ASC current monitors (IMONs) monitors the MachXO4 core current using resistor R181 as a shunt. The IMON uses the differential voltage across R181 to monitor the current. The ASC has two IMONs: one is used for low-voltage (–0.3 V to 5.9 V) current monitoring (pins 19 and 20), and the other, HIMON (pins 17 and 18), is used for high-voltage (4.5 V to 13.2 V) current monitoring. Pin 18 is a shared input for both HIMON and HVMON (VMON10).

Table 8.3. ASC IMON Connections

Power Name	ASC Signal Name	ASC Pin Number	ASC Breakout Test Point	Comments
VCC_CORE	ASC_IMONP	19	TP30	R181 (0.020 Ω) is placed between P/N node for current measurement
	ASC_IMONN	20	TP31	
User Connected	ASC_HIMONP	17	TP28	HV IMON positive input
	ASC_HVMON	18	TP29	Dual Function: HV IMON negative input and VMON10 input

The V_{CC_CORE} current measurement circuit is shown in Figure 8.3.

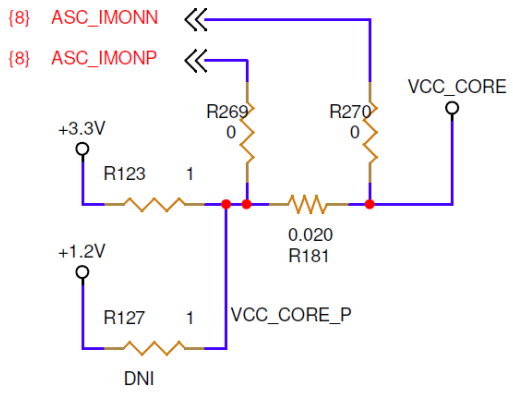

Figure 8.3. VCC Core Current Monitoring Circuit

8.4. ASC Temperature Monitor

The ASC has two external temperature monitors (TMONs), both connected to onboard temperature sensors, as listed in Table 8.4. One TMON is connected to a PNP transistor, as shown in Figure 8.4, and the other is connected to an NPN transistor, as shown in Figure 8.5. Noise-suppression capacitors (C33 and C34) are shown on the schematic near the transistors; however, they are physically located near the L-ASC10 (U7).

Table 8.4. ASC TMON Connections

Temperature Sensor (Reference)	ASC Signal Name	ASC Pin Number	ASC Breakout Test Point	Comments
Temperature Sensor 1 (Q1)	TEMP_SENSE1P	21	TP32	PNP Type
	TEMP_SENSE1N	22	TP33	
Temperature Sensor 1 (Q2)	TEMP_SENSE2P	23	TP34	NPN Type
	TEMP_SENSE2N	24	TP35	

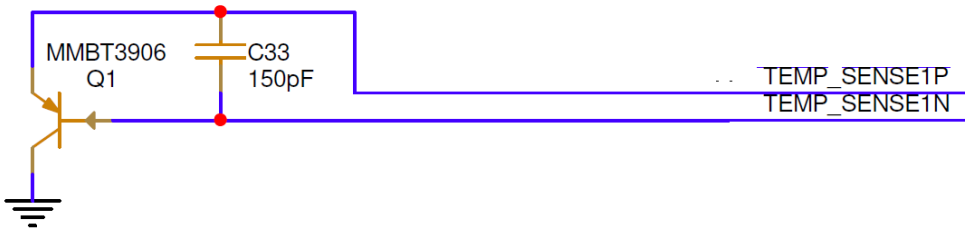

Figure 8.4. PNP Temperature Sensor Circuit

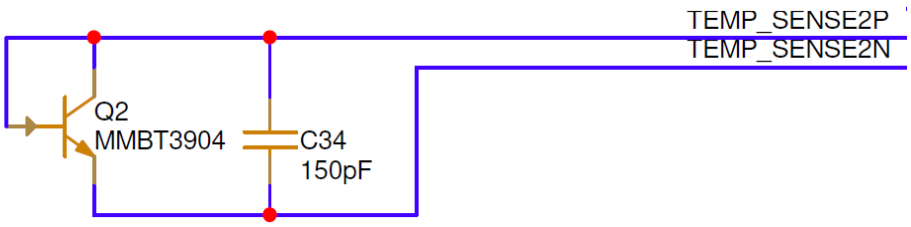

Figure 8.5. NPN Temperature Sensor Circuit

8.5. ASC LEDs

As shown in Figure 8.6, the board includes nine red LEDs to support ASC applications. They are connected to the ASC GPIOs, as listed in Table 8.5. The LEDs turn on when the GPIO is driven low.

Figure 8.6. ASC LEDs

Table 8.5. GPIO LED Connections

Signal Name	ASC Pin Number	LED	Breakout Test Point	Logic Level to Light
ASC_LED1	44	D9	TP44	0
ASC_LED2	45	D10	TP45	0
ASC_LED3	46	D11	TP46	0
ASC_LED4	47	D12	TP47	0
ASC_LED5	48	D13	TP48	0
ASC_LED6	1	D14	TP49	0
ASC_LED8	11	D15	TP50	0
ASC_LED9	12	D16	TP51	0
ASC_LED10	13	D17	TP52	0

Caution: The MachXO4 Development Board contains ESD-sensitive components. Follow ESD-safe practices when handling and using the Development Board.

Note: The LEDs are lined up in sequence, as shown in Figure 8.6.

8.6. ASC HVOUT and Trim Pins

The ASC has four high-voltage charge-pump outputs (HVOUTs) and four trim-DAC outputs (TRIMs), which are brought out to test pins for your convenience, as listed in Table 8.6. The HVOUTs are designed to drive the gates of MOSFETs to enable circuits and loads. The TRIMs are designed to drive the trim inputs of DC-DC converters to adjust the output voltage.

Table 8.6. ASC HVOUT and Trim Connections

Signal Name	ASC Pin Number	Breakout Test Point
ASC_HVOUT1	2	TP40
ASC_HVOUT2	3	TP41
ASC_HVOUT3	9	TP42
ASC_HVOUT4	10	TP43
ASC_TRIM1	39	TP36
ASC_TRIM2	40	TP37
ASC_TRIM3	41	TP38
ASC_TRIM4	42	TP39

9. Software Requirements

The following software packages are required to develop designs for the MachXO4 Development Board:

- Lattice Radiant Software 2025.2 or later
- Lattice Radiant Programmer 2025.2 or later

10. Storage and Handling

Static electricity can shorten the life of electronic components. Follow these tips to prevent electrostatic-discharge damage:

- Use ESD-safe practices, such as working on an antistatic mat and wearing an antistatic wrist strap.
- Store the development board in its original packaging.
- Touch a grounded metal surface (such as USB housing) to equalize the voltage potential between you and the board.

11. Ordering Information

Table 11.1 Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
MachXO4 Development Board	LFMXO4-110-EVN	

Appendix A. MachXO4 Development Board Schematics

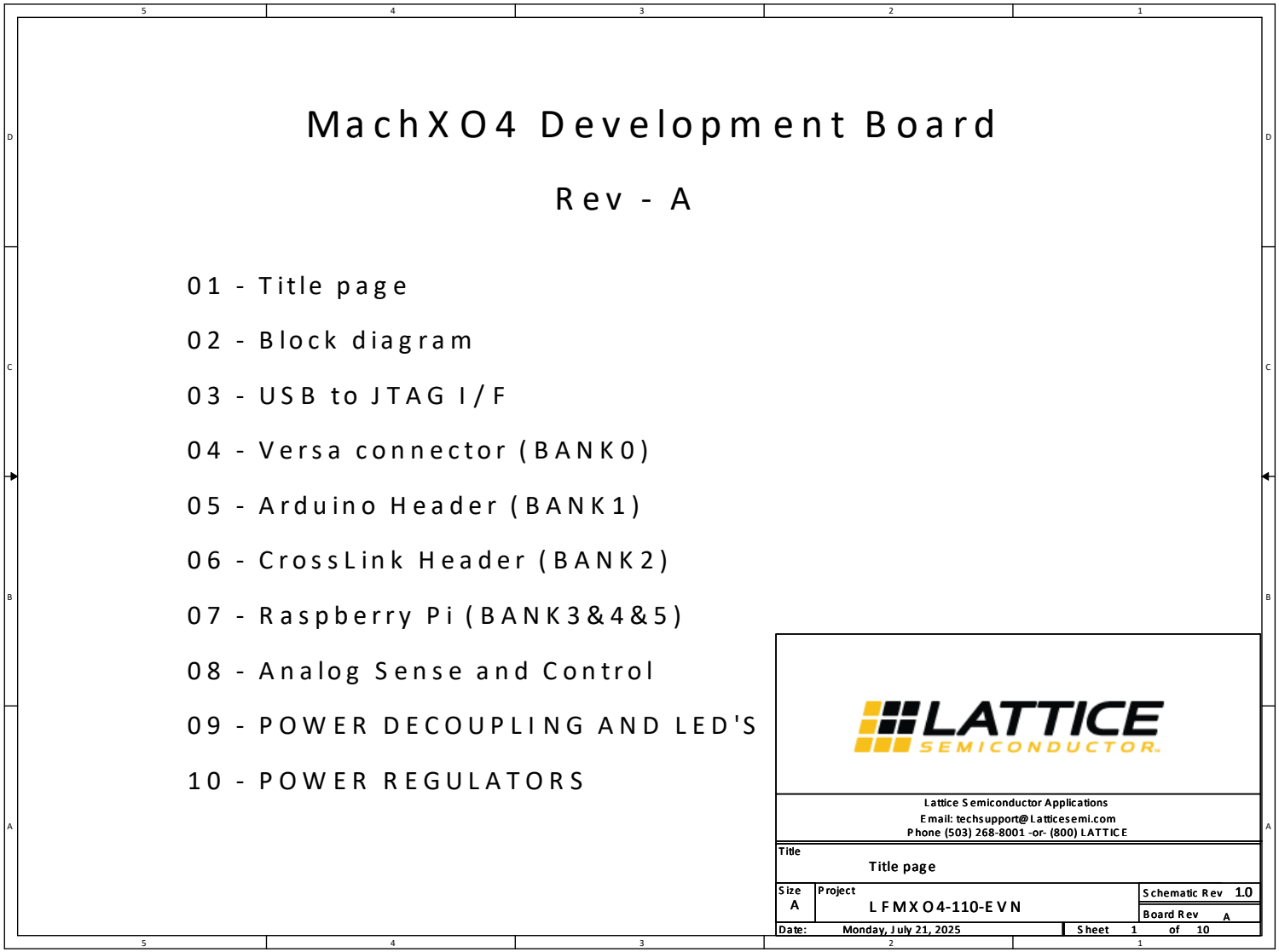

Figure A.1. Title Page

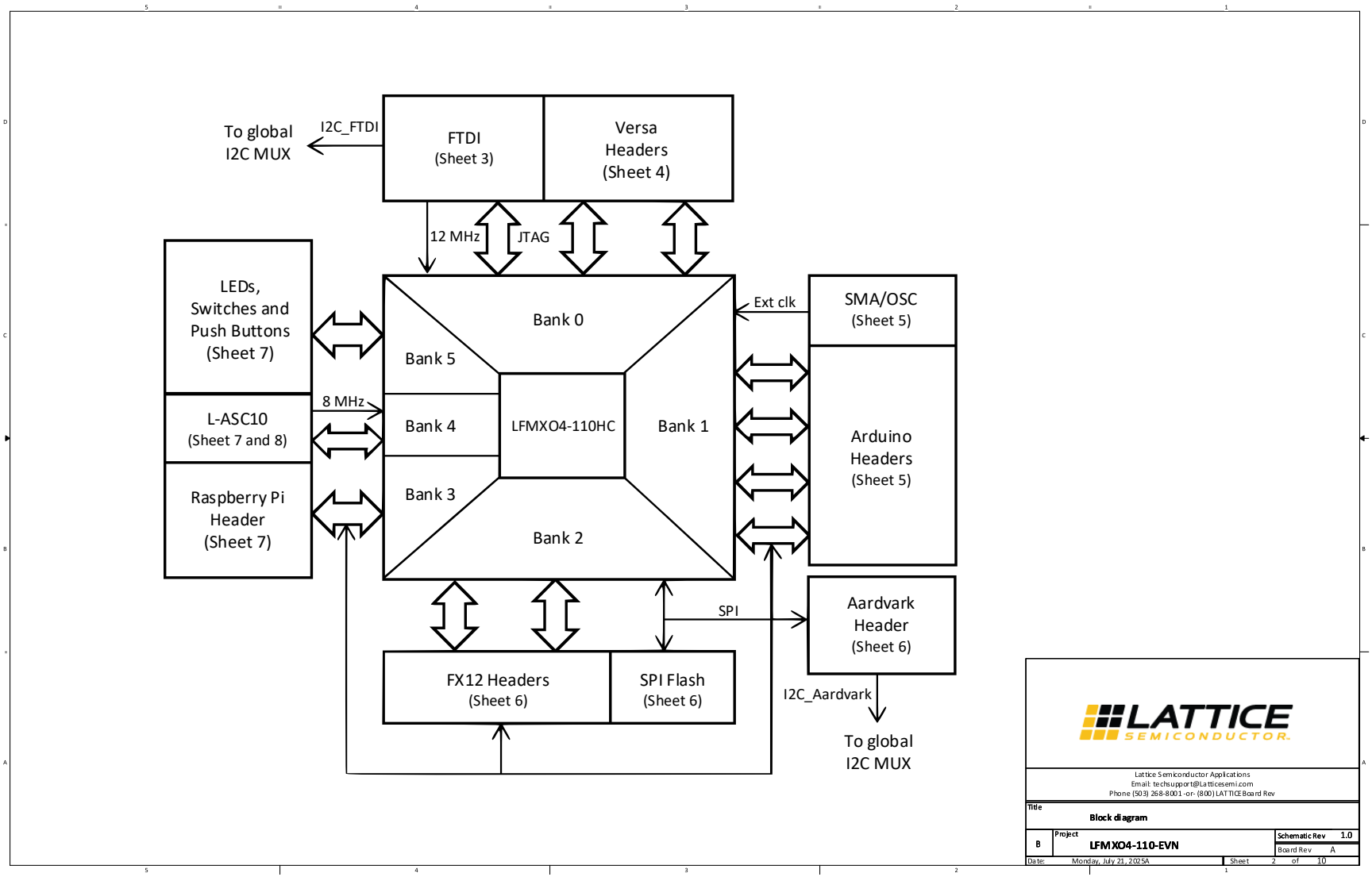

Figure A.2. Block Diagram

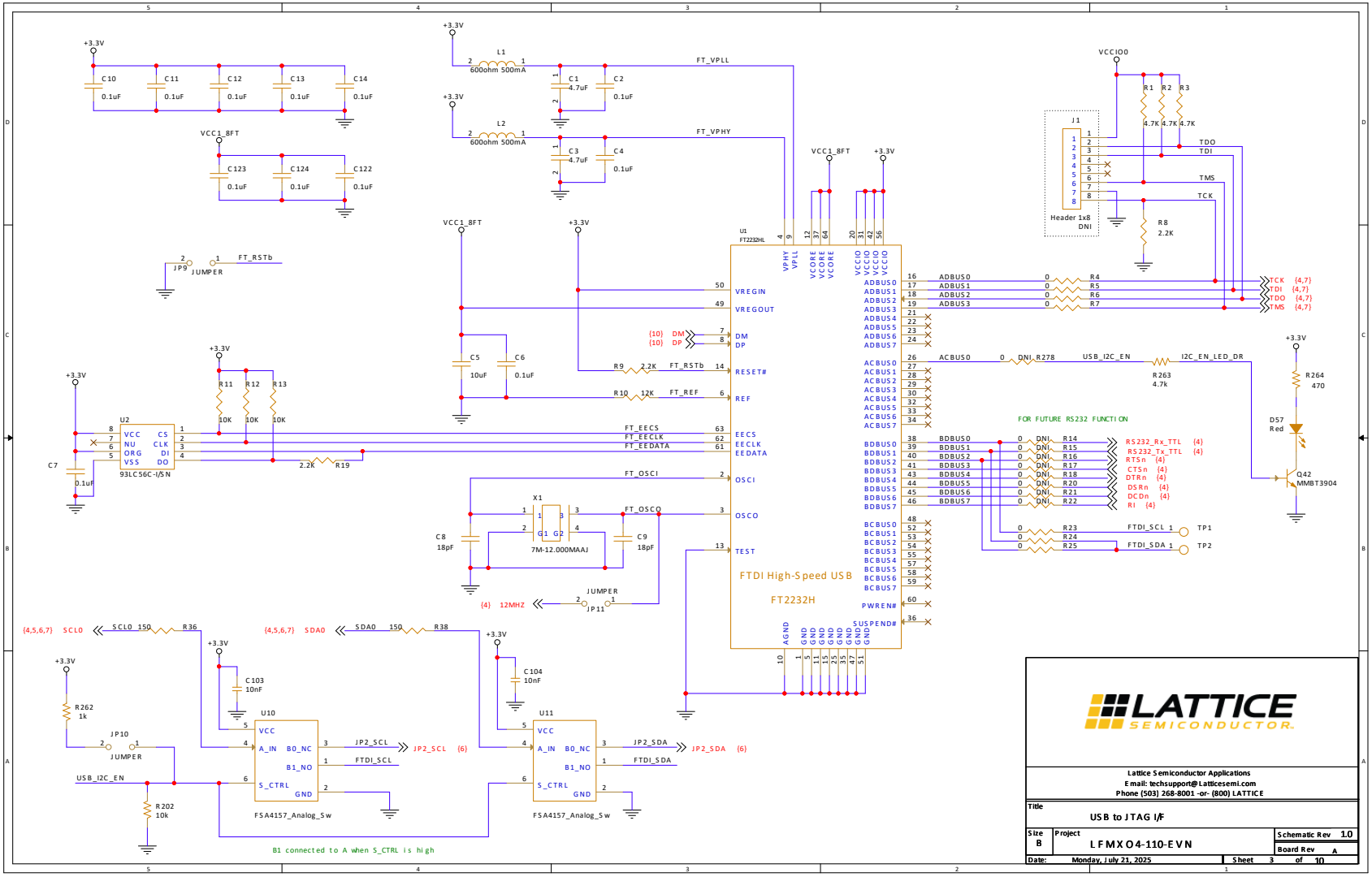

Figure A.3. USB to JTAG I/F

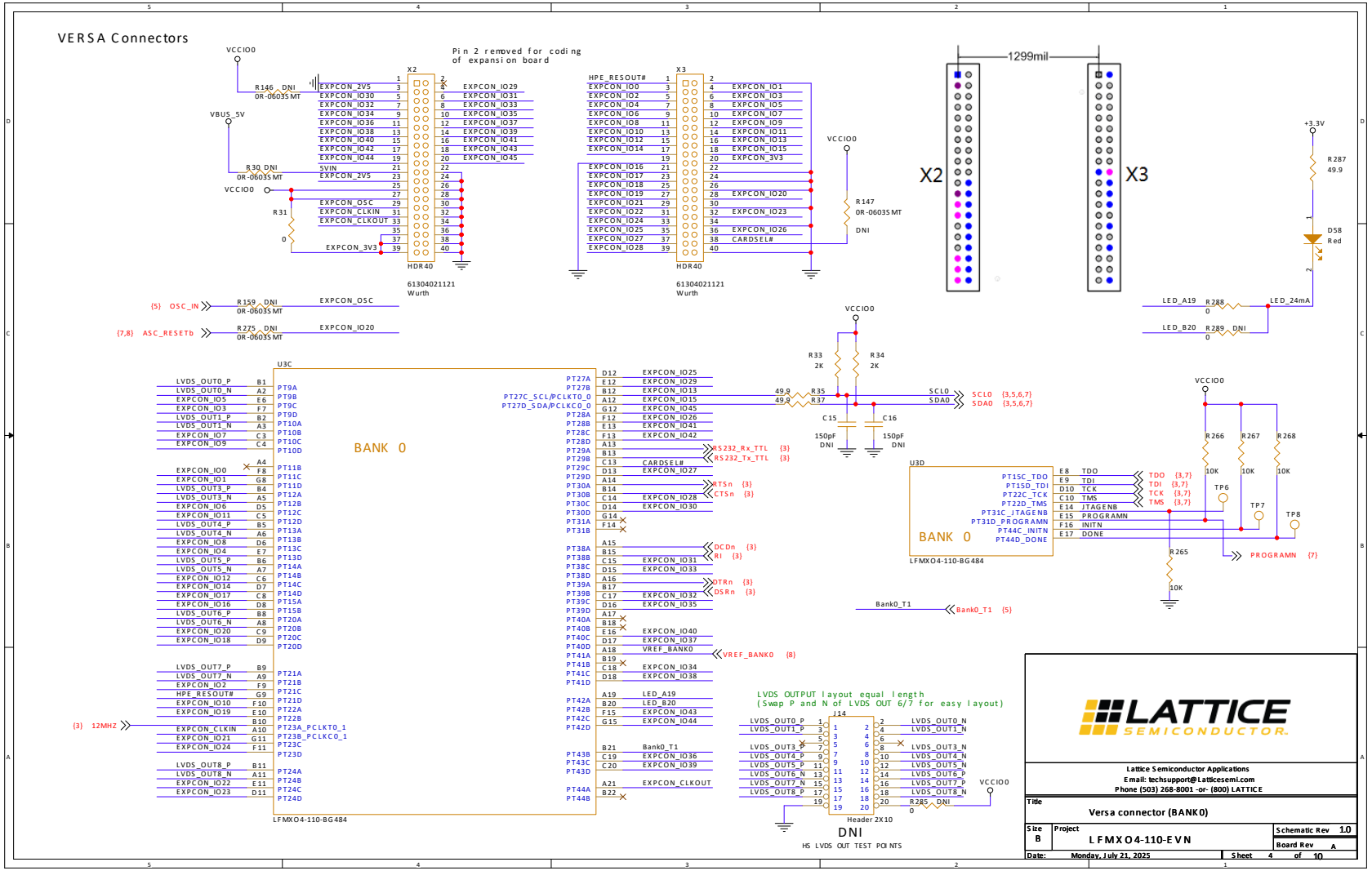

Figure A.4. VERSA Headers (BANK0)

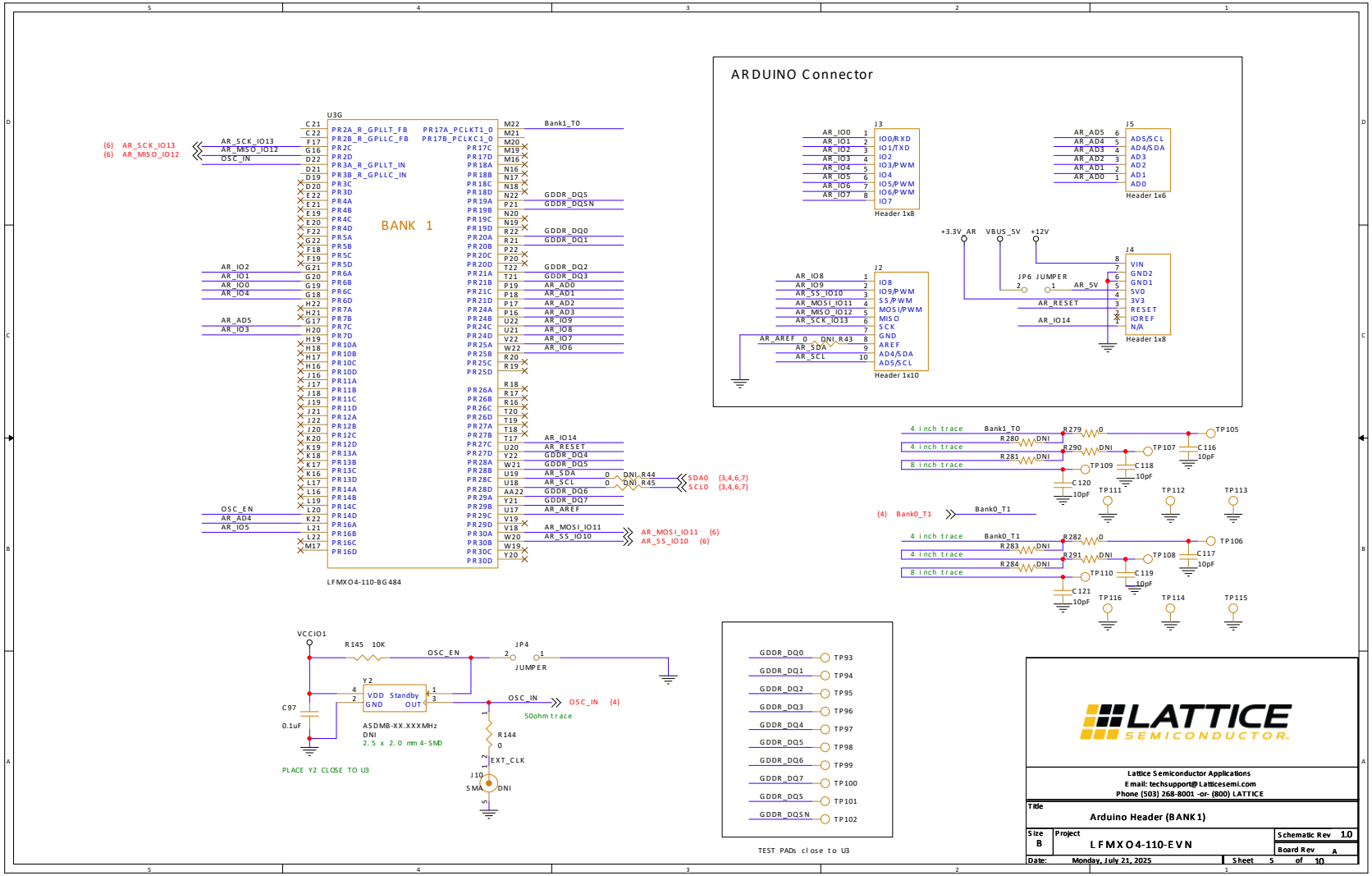

Figure A.5. Arduino Headers (BANK1)

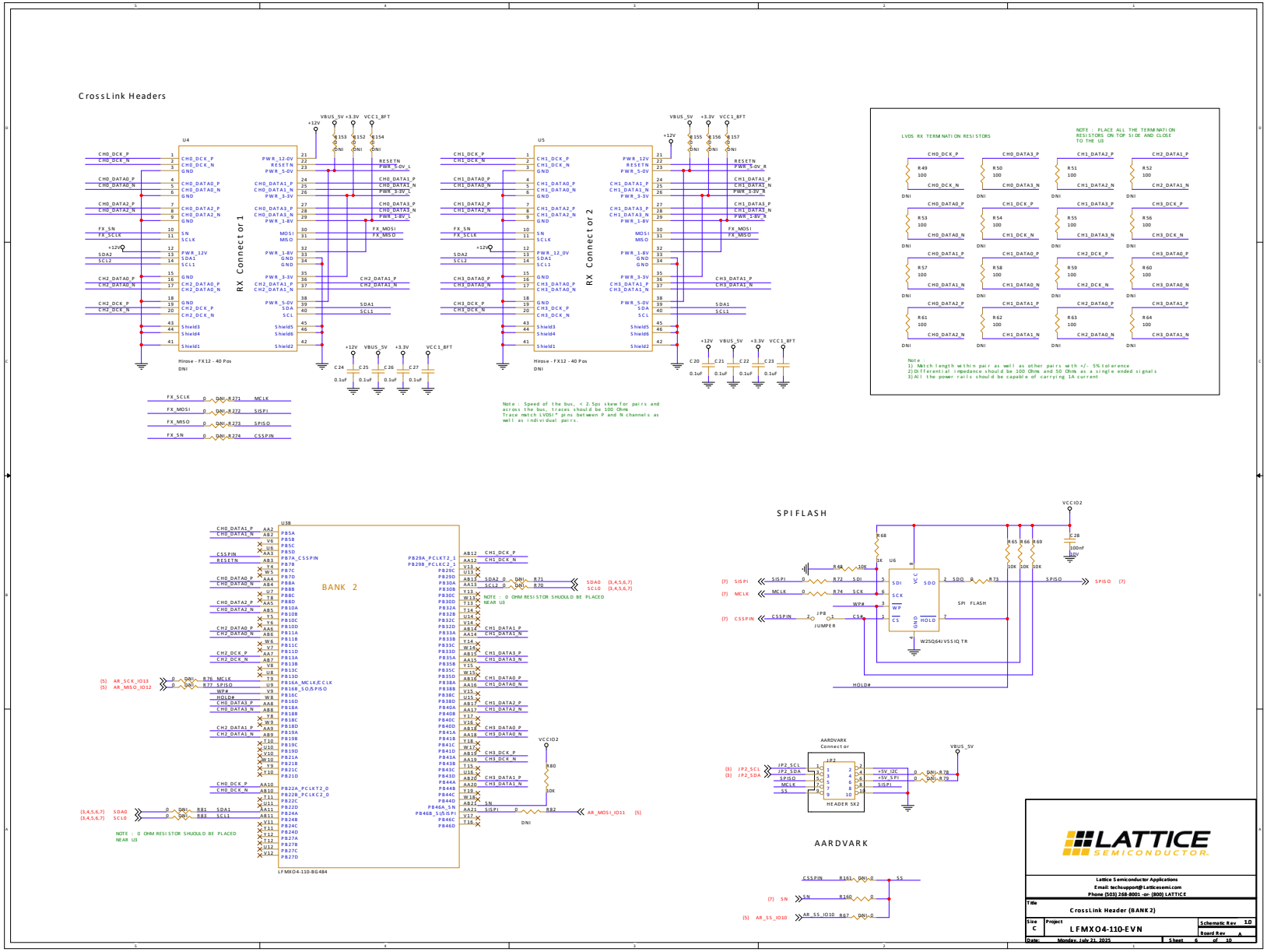

Figure A.6. CrossLink Headers (BANK2)

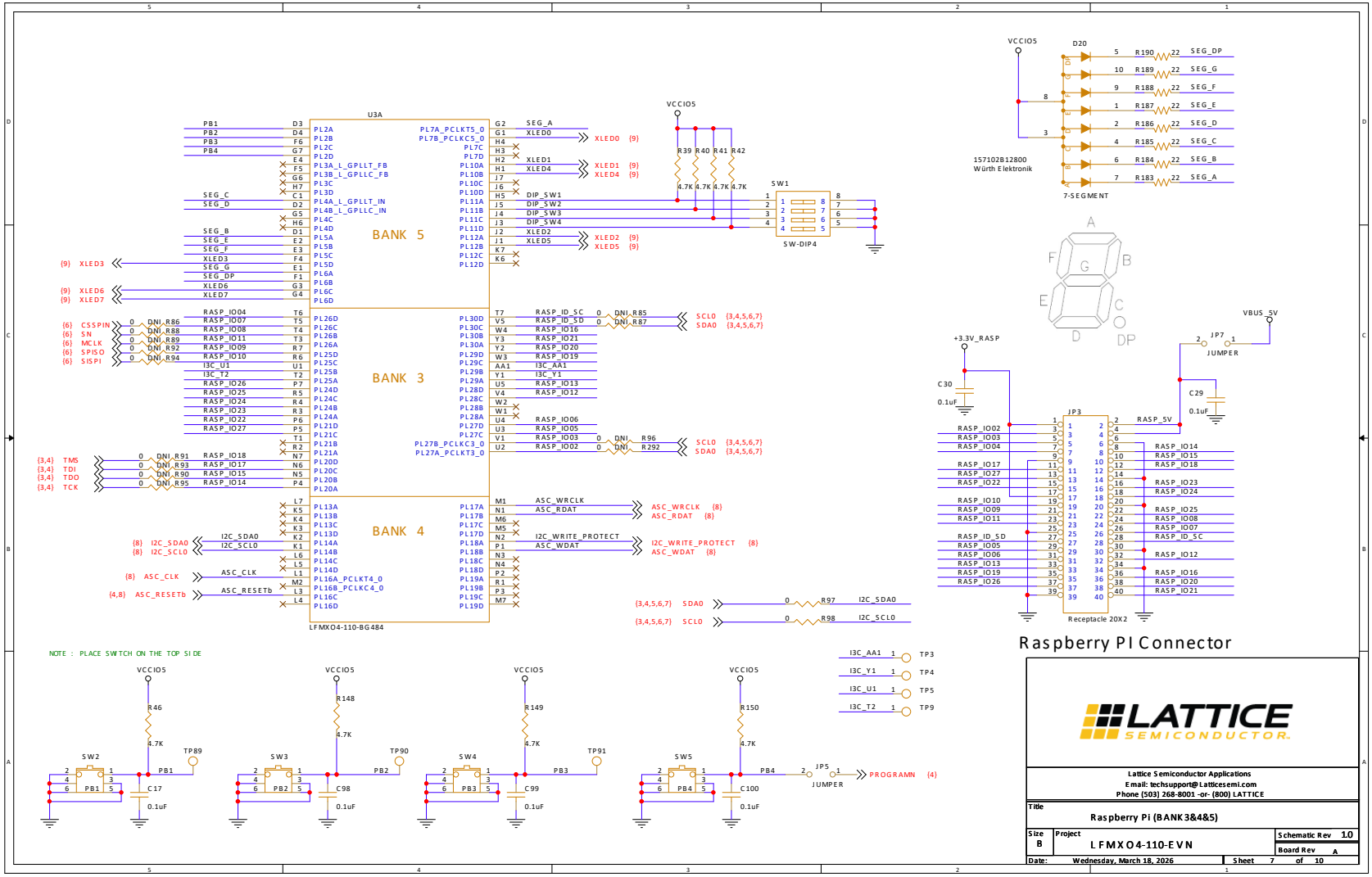

Figure A.7. Raspberry Pi Header and Others (BANK3, BANK4, BANK5)

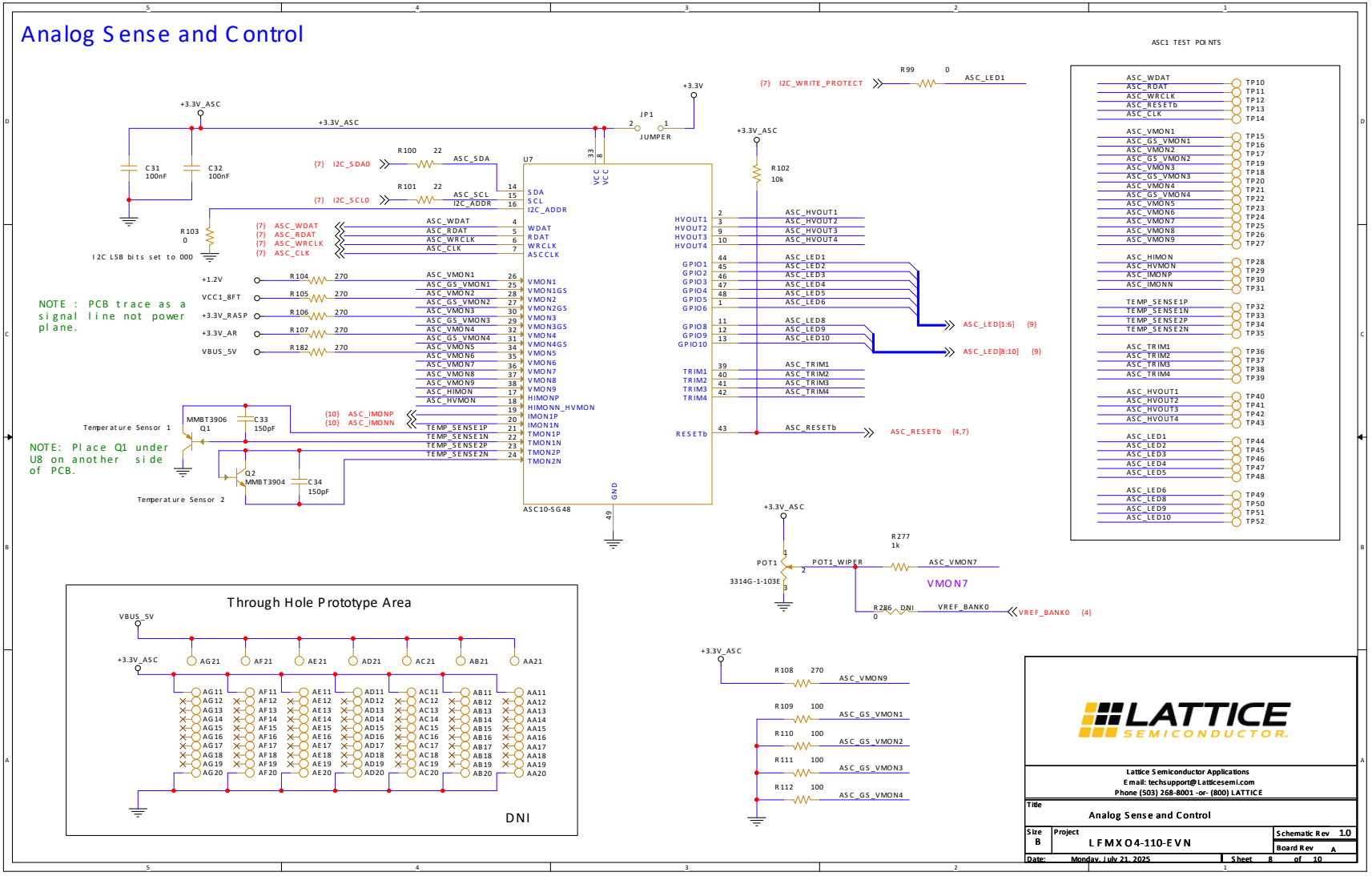

Figure A.8. Analog Sense and Control

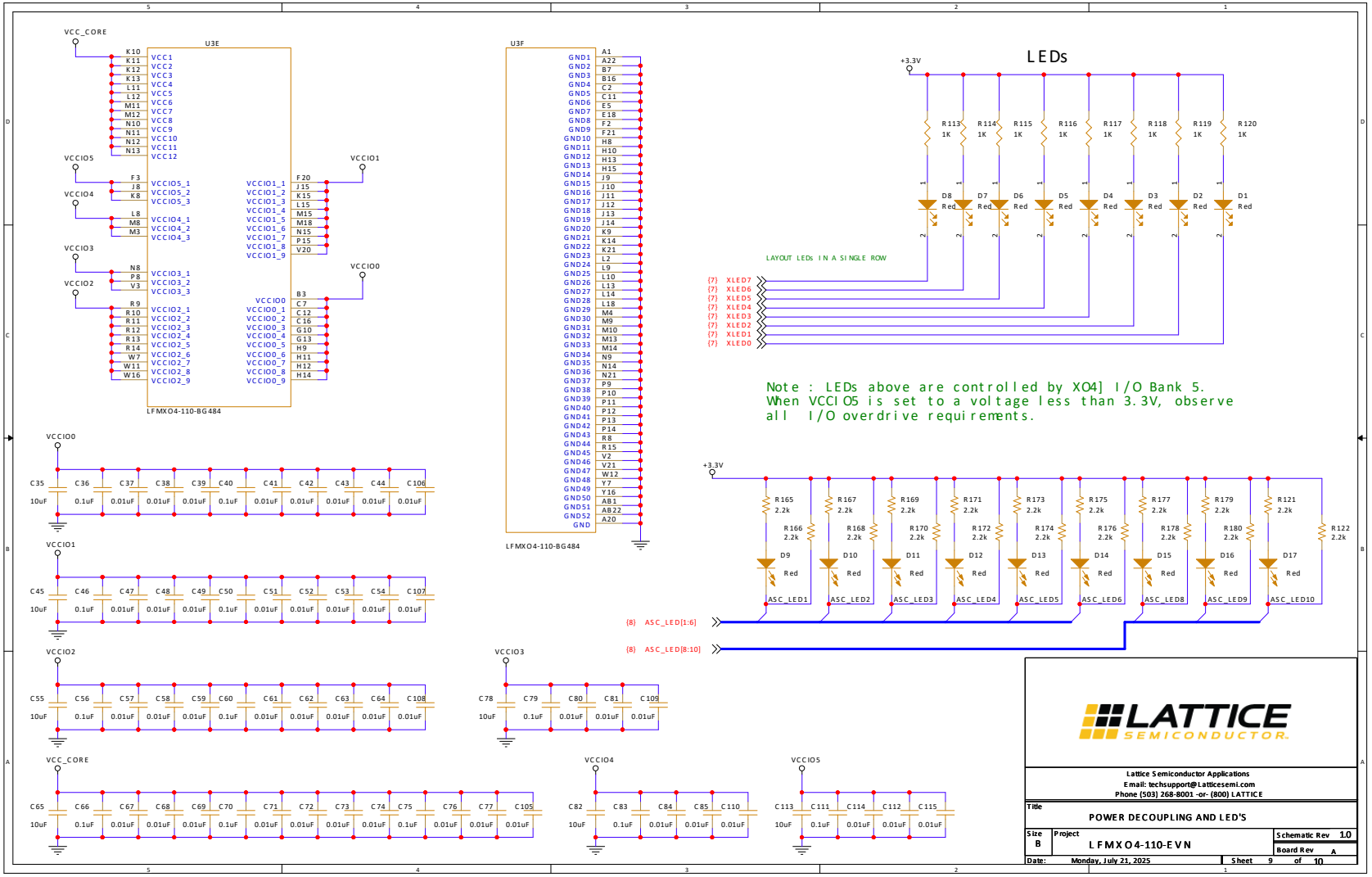

Figure A.9. Power Decoupling and LEDs

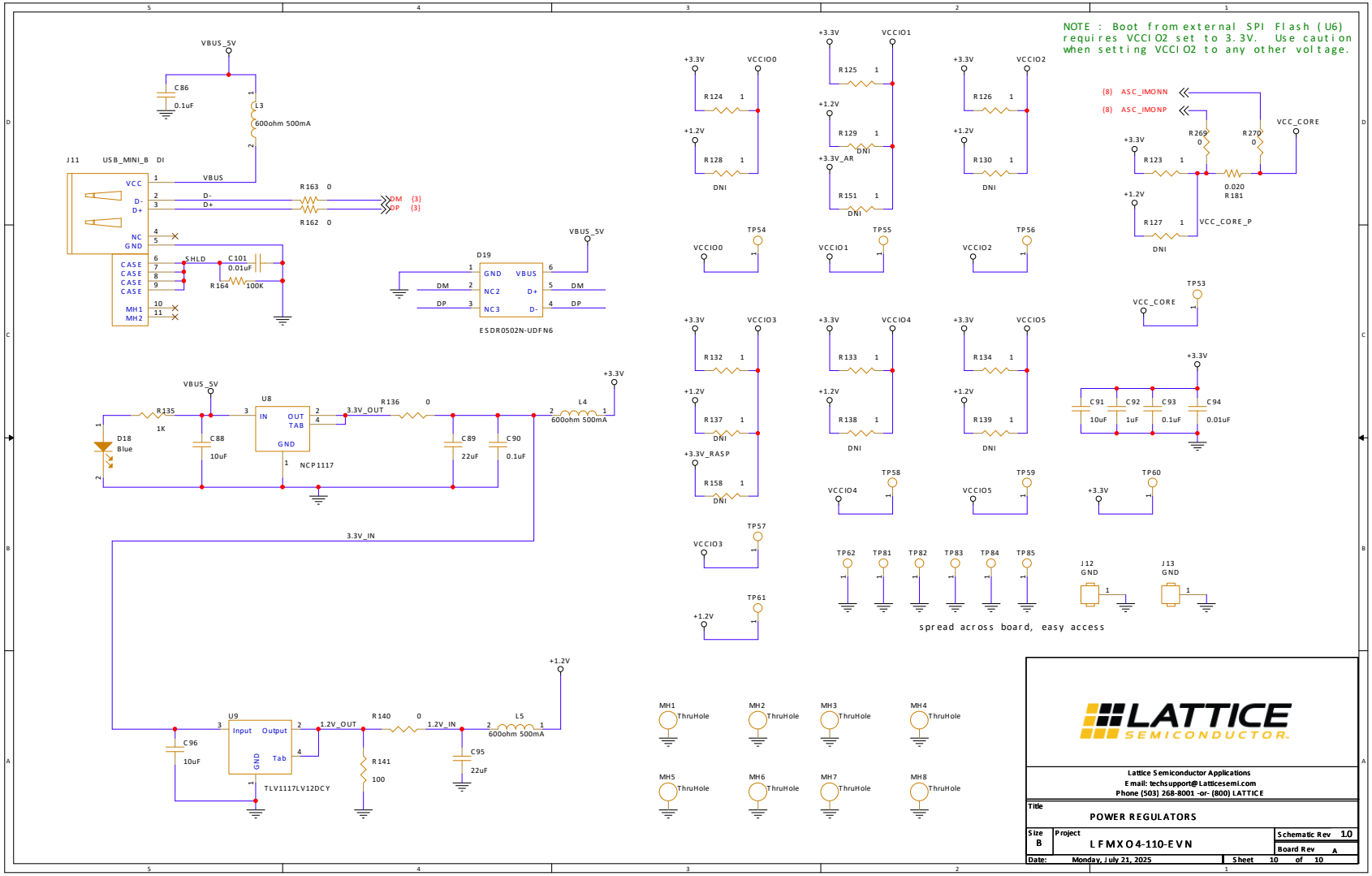

Figure A.10. Power Regulators

Appendix B. MachXO4 Development Board Bill of Materials

Item	Reference	Qty	Part	PCB Footprint	Part Number	Manufacturer	Description
1	AG11,AF11,AE11,AD11,AC11, AB11,AA11,AG12,AF12,AE12, AD12,AC12,AB12,AA12,AG13, AF13,AE13,AD13,AC13,AB13, AA13,AG14,AF14,AE14,AD14, AC14,AB14,AA14,AG15,AF15, AE15,AD15,AC15,AB15,AA15, AG16,AF16,AE16,AD16,AC16, AB16,AA16,AG17,AF17,AE17, AD17,AC17,AB17,AA17,AG18, AF18,AE18,AD18,AC18,AB18, AA18,AG19,AF19,AE19,AD19, AC19,AB19,AA19,AG20,AF20, AE20,AD20,AC20,AB20,AA20, AG21,AF21,AE21,AD21,AC21, AB21,AA21	77	T POINT R	TP	—	—	—
2	C1,C3	2	4.7uF	C0603	CL10A475KA8NQNC	Samsung	CAP CER 4.7UF 25V 10% X5R 0603
3	C2,C4,C6,C7,C10,C11,C12,C13 ,C14,C17,C86,C90,C93,C97,C9 8,C99,C100,C122,C123,C124	20	0.1uF	C0402	CL05B104KA5NNNC	Samsung	CAP CER 0.1UF 25V 10% X7R 0402
4	C5,C88,C91,C96	4	10uF	C0603	LMK107BJ106MALT D	Taiyo Yuden	CAP CER 10UF 10V X5R 0603
5	C8,C9	2	18pF	C0402	C0402C180K3GACT U	Kemet	CAP CER 18PF 25V C0G/NP0 0402
6	C15,C16	2	150pF	C0402	—	—	—
7	C20,C21,C22,C23,C24,C25,C2 6,C27,C29,C30	10	0.1uF	C0402	CL05B104KA5NNNC	Samsung	CAP CER 0.1UF 25V 10% X7R 0402
8	C28	1	100nF	C0402	CL05B104KA5NNNC	Samsung	CAP CER 0.1UF 25V 10% X7R 0402
9	C31,C32	2	100nF	C0603	CL10B104KA8NNNC	Samsung	CAP CER 0.1UF 25V X7R 0603
10	C33,C34	2	150pF	C0603	CL10B151KB8NNNC	Samsung	CAP CER 150PF 50V X7R 0603
11	C35,C45,C55,C65,C78,C82,C1 13	7	10uF	C0603	LMK107BJ106MALT D	Taiyo Yuden	CAP CER 10UF 10V X5R 0603
12	C36,C40,C46,C50,C56,C60,C6 6,C70,C75,C79,C83,C111	12	0.1uF	C0201	CL03A104KA3NNNC	Samsung	CAP CER 0.1UF 25V X5R 0201

Item	Reference	Qty	Part	PCB Footprint	Part Number	Manufacturer	Description
13	C37,C38,C39,C41,C42,C43,C44,C47,C48,C49,C51,C52,C53,C54,C57,C58,C59,C61,C62,C63,C64,C67,C68,C69,C71,C72,C73,C74,C76,C77,C80,C81,C84,C85,C105,C106,C107,C108,C109,C110,C112,C114,C115	43	0.01uF	C0201	CL03A103KA3NNNC	Samsung	CAP CER 10000PF 25V X5R 0201
14	C89,C95	2	22uF	cc0805	CL21A226KOQNNNE	Samsung	CAP CER 22UF 16V X5R 0805
15	C92	1	1uF	C0402	CL05A105KO5NNNC	Samsung	CAP CER 1UF 16V X5R 0402
16	C94,C101	2	0.01uF	C0402	CL05B103KA5NNNC	Samsung	CAP CER 10000PF 25V X7R 0402
17	C103,C104	2	10nF	SM_C_0603	KGM15AR51H103KT	KYOCERA AVX	CAP CER 10000PF 50V X5R 0603
18	C116,C117,C118,C119,C120,C121	6	10pF	C0402	CC0402KRNPO8BN100	YAGEO	CAP CER 10PF 25V C0G/NPO 0402
19	D1,D2,D3,D4,D5,D6,D7,D8,D58	9	Red	led_0603	LTST-C190KRKT	LITE-On INC	LED RED CLEAR 0603 SMD
20	D9,D10,D11,D12,D13,D14,D15,D16,D17,D57	10	Red	led_0603	LTST-C190KRKT	LITE-On INC	LED RED CLEAR 0603 SMD
21	D18	1	Blue	led_0603	LTST-C190TBKT	LITE-On INC	LED 468NM BLUE CLEAR 0603 SMD
22	D19	1	ESDR0502N-UDFN6	UDFN6_040	ESDR0502NMUTBG	ON semi	TVS DIODE 5.5VWM 6UDFN
23	D20	1	7-SEGMENT	LED_157102B12800	157102B12800	Würth Elektronik	WL-S7DS 7 SEGMENTS DISPLAY SMT S
24	JP1,JP4,JP5,JP6,JP7,JP8,JP9,JP10,JP11	9	JUMPER	Header_1x2	—	—	—
25	JP2	1	HEADER 5X2	HDR254-2X5_SHROUDED	70246-1003	Molex	CONN HEADER VERT 10POS 2.54MM
26	JP3	1	Receptacle 20X2	HDR254-2X20_socket	PPTC202LFBN-RC	Sullins	CONN HEADER FEM 40POS .1" DL TIN
27	J1	1	Header 1x8	hdr_amp_87220_8_1x8_100	22284081	Molex	CONN HEADER 8POS .100 VERT TIN
28	J2	1	Header 1x10	CONF1X10-254P_2612X240X850H_TH	—	—	—

Item	Reference	Qty	Part	PCB Footprint	Part Number	Manufacturer	Description
29	J3,J4	2	Header 1x8	CONF1X8-254P_2104X240X850H_TH	—	—	—
30	J5	1	Header 1x6	CONF1X6-254P_1596X240X850H_TH	—	—	—
31	J10	1	SMA	bnc5-100-280t	5-1814832-1	TE Connectivity	CONN SMA JACK STR 50 OHM PCB
32	J11	1	USB_MINI_B	usb2-0-rec-240-0001-9	UX60-MB-5ST	Hirose	CONN RECEPT MINI USB2.0 5POS
33	J12,J13	2	GND	TUR_TH	1573-2	Keystone Electronics	Terminal Turret Connector Single End 0.186" (4.72mm) Tin
34	J14	1	Header 2X10	HDR100-10X2	—	—	—
35	L1,L2,L3,L4,L5	5	600ohm 500mA	fb0603	BLM18AG601SN1D	Murata	FERRITE CHIP 600 OHM 500MA 0603
36	MH1,MH2,MH3,MH4,MH5,MH6,MH7,MH8	8	ThruHole	MTG125	—	—	—
37	POT1	1	3314G-1-103E	sot23-3314G-1	3314G-1-103E	Bourns Inc.	TRIMMER 10K OHM 0.25W SMD
38	Q1	1	MMBT3906	MMBT3906	MMBT3906	Fairchild	TRANS PNP 40V 0.2A SOT-23
39	Q2,Q42	2	MMBT3904	MMBT3904	MMBT3904	Fairchild	TRANS NPN 40V 0.2A SOT-23
40	R1,R2,R3,R39,R40,R41,R42,R46,R148,R149,R150	11	4.7K	R0603	RC0603FR-074K7L	Yageo	RES 4.70K OHM 1/10W 1% 0603 SMD
41	R4,R5,R6,R7,R23,R24,R25,R72,R73,R74,R136,R140,R269,R270	14	0	R0603	RC0603FR-070RL	Yageo	RES 0.0 OHM 1/10W JUMP 0603 SMD
42	R8,R9,R19	3	2.2K	R0603	RC0603FR-072K2L	Yageo	RES 2.2K OHM 1% 1/10W 0603
43	R10	1	12K	R0603	RC0603FR-0712KL	Yageo	RES 12K OHM 1/10W 1% 0603 SMD
44	R11,R12,R13,R65,R66,R69,R80,R265,R266,R267,R268	11	10K	R0603	RC0603FR-0710KL	Yageo	RES 10K OHM 1/10W 1% 0603
45	R14,R15,R16,R17,R18,R20,R21,R22,R85,R86,R87,R88,R89,R90,R91,R92,R93,R94,R95,R96,R278,R292	22	0	R0603	—	—	—
46	R30,R146,R147,R159,R275	5	0R-0603SMT	R0603	—	—	—
47	R31,R99,R103	3	0	R0603	RC0603FR-070RL	Yageo	RES 0.0 OHM 1/10W JUMP 0603 SMD
48	R33,R34	2	2K	R0603	RC0603FR-072KL	Yageo	RES 2.0K OHM 1/10W 1% 0603 SMD

Item	Reference	Qty	Part	PCB Footprint	Part Number	Manufacturer	Description
49	R35,R37	2	49.9	R0603	RC0603FR-0749R9L	Yageo	RES 49.9 OHM 1/10W 1% 0603 SMD
50	R36,R38	2	150	R0603	RC0603FR-07150RL	Yageo	RES 150 OHM 1% 1/10W 0603
51	R43,R44,R45,R67,R70,R71,R76,R77,R78,R79,R81,R82,R83,R152,R153,R154,R155,R156,R157,R161,R271,R272,R273,R274	24	0	R0603	RC0603FR-070RL	Yageo	RES 0.0 OHM 1/10W JUMP 0603 SMD
52	R48	1	10K	R0603	RC0603FR-0710KL	Yageo	RES 10K OHM 1/10W 1% 0603
53	R49,R50,R51,R52,R53,R54,R55,R56,R57,R58,R59,R60,R61,R62,R63,R64	16	100	R0402	—	—	—
54	R68,R113,R114,R115,R116,R117,R118,R119,R120,R135	10	1K	R0603	RC0603FR-071KL	Yageo	RES 1K OHM 1/10W 1% 0603 SMD
55	R97,R98,R160	3	0	R0603	RC0603FR-070RL	Yageo	RES 0.0 OHM 1/10W JUMP 0603 SMD
56	R100,R101,R183,R184,R185,R186,R187,R188,R189,R190	10	22	R0603	RC0603FR-0722RL	Yageo	RES 22 OHM 1% 1/10W 0603
57	R102,R145,R202	3	10k	R0603	RC0603FR-0710KL	Yageo	RES 10K OHM 1/10W 1% 0603
58	R104,R105,R106,R107,R108,R182	6	270	R0603	RC0603FR-07270RL	Yageo	RES 270 OHM 1% 1/10W 0603
59	R109,R110,R111,R112	4	100	R0603	RC0603FR-07100RL	Yageo	RES 100 OHM 1% 1/10W 0603
60	R121,R122,R165,R166,R167,R168,R169,R170,R171,R172,R173,R174,R175,R176,R177,R178,R179,R180	18	2.2k	R0603	RC0603FR-072K2L	Yageo	RES 2.2K OHM 1% 1/10W 0603
61	R123,R124,R125,R126,R132,R133,R134	7	1	R0603	RC0603FR-071RL	Yageo	RES 1 OHM 1% 1/10W 0603
62	R127,R128,R129,R130,R137,R138,R139,R151,R158	9	1	R0603	RC0603FR-071RL	Yageo	RES 1 OHM 1% 1/10W 0603
63	R141	1	100	R0603	RC0603FR-07100RL	Yageo	RES 100 OHM 1% 1/10W 0603
64	R144,R162,R163	3	0	R0402	RC0402FR-070RL	Yageo	RES 0 OHM JUMPER 1/16W 0402
65	R164	1	100K	R0603	RC0603FR-07100KL	Yageo	RES 100K OHM 1% 1/10W 0603
66	R181	1	0.02	SM_R_1206	RL1206FR-070R02L	Yageo	RES 0.02 OHM 1% 1/4W 1206
67	R262,R277	2	1k	R0603	RC0603FR-071KL	Yageo	RES 1K OHM 1/10W 1% 0603 SMD
68	R263	1	4.7k	R0603	RC0603FR-074K7L	Yageo	RES 4.7K OHM 1% 1/10W 0603
69	R264	1	470	R0603	RC0603FR-07470RL	Yageo	RES 470 OHM 1% 1/10W 0603
70	R279,R282,R288	3	0	R0603	RC0603FR-070RL	Yageo	RES 0.0 OHM 1/10W JUMP 0603 SMD

Item	Reference	Qty	Part	PCB Footprint	Part Number	Manufacturer	Description
71	R280,R281,R283,R284,R290,R291	6	DNI	R0603	—	—	—
72	R285,R286,R289	3	0	R0603	—	—	—
73	R287	1	49.9	R0603	RC0603FR-0749R9L	Yageo	RES 49.9 OHM 1/10W 1% 0603 SMD
74	SW1	1	SW-DIP4	sw_sp_st_cts_195-4mst	195-4MST	CTS	SWITCH PIANO DIP SPST 50MA 24V
75	SW2	1	PB1	sw_sp_st_eswitch_tl1015	TL1015AF160QG	E-Switch	SWITCH TACTILE SPST-NO 0.05A 12V
76	SW3	1	PB2	sw_sp_st_eswitch_tl1015	TL1015AF160QG	E-Switch	SWITCH TACTILE SPST-NO 0.05A 12V
77	SW4	1	PB3	sw_sp_st_eswitch_tl1015	TL1015AF160QG	E-Switch	SWITCH TACTILE SPST-NO 0.05A 12V
78	SW5	1	PB4	sw_sp_st_eswitch_tl1015	TL1015AF160QG	E-Switch	SWITCH TACTILE SPST-NO 0.05A 12V
79	TP1,TP2,TP3,TP4,TP5,TP9,TP53,TP54,TP55,TP56,TP57,TP58,TP59,TP60,TP61,TP62,TP81,TP82,TP83,TP84,TP85	21	TP_S_40_63	TP	—	—	Square test point, 40mil inner diameter, 63mil outer diameter
80	TP6,TP7,TP8	3	TestPoint	TP	—	—	—
81	TP10,TP11,TP12,TP13,TP14,TP15,TP16,TP17,TP18,TP19,TP20,TP21,TP22,TP23,TP24,TP25,TP26,TP27,TP28,TP29,TP30,TP31,TP32,TP33,TP34,TP35,TP36,TP37,TP38,TP39,TP40,TP41,TP42,TP43,TP44,TP45,TP46,TP47,TP48,TP49,TP50,TP51,TP52	43	T POINT R	TP	—	—	—
82	TP89,TP90,TP91	3	TestPoint	TP	—	—	—
83	TP93,TP94,TP95,TP96,TP97,TP98,TP99,TP100,TP101,TP102,TP105,TP106,TP107,TP108,TP109,TP110,TP111,TP112,TP113,TP114,TP115,TP116	22	T POINT R	TPC32	—	—	—
84	U1	1	FT2232HL	tqfp64_0p5_12p2x12p2_h1p6	FT2232HL	FTDI	IC USB HS DUAL UART/FIFO 64-LQFP
85	U2	1	93LC56C-I/SN	so8_50_244	93LC56C-I/SN	Microchip	IC EEPROM 2KBIT 3MHZ 8SOIC

Item	Reference	Qty	Part	PCB Footprint	Part Number	Manufacturer	Description
86	U3	1	LFMXO4-110-BG484	BGA484-080	LFMXO4-110-BG484	Lattice	—
87	U4,U5	2	Hirose - FX12 - 40 Pos	Hirose-FX12	FX12B-40P-0.4SV	Hirose Electric Co Ltd	Conn Board to Board PL 40 POS 0.4mm Solder ST SMD T/R
88	U6	1	W25Q64JV SSIQ TR	SOIC8_W25Q64JV	W25Q64JVSSIQ TR	Winbond Electronics	IC FLASH 64MBIT SPI/QUAD 8SOIC
89	U7	1	ASC10-SG48	TQFN_48	L-ASC10-1SG48I	Lattice	ASC Device
90	U8	1	NCP1117	sot223_4p	NCP1117ST33T3G	On Semi	IC REG LDO 3.3V 1A SOT223
91	U9	1	TLV1117LV 12DCY	sot223_4p	TLV1117LV12DCYR	TI	IC REG LDO 1.2V 1A SOT223-3
92	U10,U11	2	FSA4157_Analog_Sw	SOP-6-26	FSA4157P6X	Fairchild	IC SWITCH SPDT SC70-6
93	X1	1	7M-12.000MAAJ	xtal_4p_7m	7M-12.000MAAJ-T	TXC	CRYSTAL 12MHZ 18PF SMD
94	X2,X3	2	HDR40	HDR-20x2	61304021121	Wurth	CONN HEADER VERT 40POS 2.54
95	Y2	1	ASDMB-XX.XXXMHz	x4-2520	ASDMB-25.000MHZ-XY-T	Abracon LLC	MEMS OSC XO 25.0000MHZ LVCMOS
96	LFMXO4-110-EVN Brd Rev A PCB	1	–	–	305-PD-25-0689	PACTRON	–

Appendix C. User Defined Constraint File

```
// These names follow the MachXO4 Development Board schematic but,
// they may be defined by the user.  Thus, they can be copied into the
// pdc file and edited to match a different naming convention if needed

// XO4 LED Connections
// Note: The following order matches the LED locations on the board
ldc_set_location -site {F4} [get_ports {led[0]}]
ldc_set_location -site {G4} [get_ports {led[1]}]
ldc_set_location -site {G3} [get_ports {led[2]}]
ldc_set_location -site {G1} [get_ports {led[3]}]
ldc_set_location -site {H2} [get_ports {led[4]}]
ldc_set_location -site {H1} [get_ports {led[5]}]
ldc_set_location -site {J2} [get_ports {led[6]}]
ldc_set_location -site {J1} [get_ports {led[7]}]

// XO4 DIP Switch Connections
ldc_set_location -site {H5} [get_ports {DIP_SW[1]}]
ldc_set_location -site {J5} [get_ports {DIP_SW[2]}]
ldc_set_location -site {J4} [get_ports {DIP_SW[3]}]
ldc_set_location -site {J3} [get_ports {DIP_SW[4]}]

// XO4 Push Button Switch Connections
ldc_set_location -site {D3} [get_ports {PB[1]}]
ldc_set_location -site {D4} [get_ports {PB[2]}]
ldc_set_location -site {F6} [get_ports {PB[3]}]
ldc_set_location -site {G7} [get_ports {PB[4]}]

//SEG LED Connections
ldc_set_location -site {F1} [get_ports SEG_LED_DP]
ldc_set_location -site {E1} [get_ports SEG_LED_G]
ldc_set_location -site {E3} [get_ports SEG_LED_F]
ldc_set_location -site {E2} [get_ports SEG_LED_E]
ldc_set_location -site {D2} [get_ports SEG_LED_D]
ldc_set_location -site {C1} [get_ports SEG_LED_C]
ldc_set_location -site {D1} [get_ports SEG_LED_B]
ldc_set_location -site {G2} [get_ports SEG_LED_A]

//Clock inputs
ldc_set_location -site {B10} [get_ports CLK_12MHz]
ldc_set_location -site {D22} [get_ports OSC_IN]
ldc_set_location -site {L20} [get_ports OSC_EN]

// XO4 SPI Flash Connections
ldc_set_location -site {AA3} [CSSPIN]
ldc_set_location -site {T9} [MCLK]
ldc_set_location -site {AA21} [SISPI]
ldc_set_location -site {U9} [SPISO]
ldc_set_location -site {V9} [WP#]
ldc_set_location -site {W8} [HOLD#]

// XO4 ARDUINO Connections
```

```
ldc_set_location -site {P19} [AR_AD0]
ldc_set_location -site {P18} [AR_AD1]
ldc_set_location -site {P17} [AR_AD2]
ldc_set_location -site {P16} [AR_AD3]
ldc_set_location -site {K22} [AR_AD4]
ldc_set_location -site {G17} [AR_AD5]
```

```
ldc_set_location -site {G19} [AR_IO0]
ldc_set_location -site {G20} [AR_IO1]
ldc_set_location -site {G21} [AR_IO2]
ldc_set_location -site {H20} [AR_IO3]
ldc_set_location -site {G18} [AR_IO4]
// XO4 ARDUINO Connections continued
ldc_set_location -site {L21} [AR_IO5]
ldc_set_location -site {W22} [AR_IO6]
ldc_set_location -site {V22} [AR_IO7]
ldc_set_location -site {U21} [AR_IO8]
ldc_set_location -site {U22} [AR_IO9]
```

```
ldc_set_location -site {W20} [AR_SS_IO10]
ldc_set_location -site {V18} [AR_MOSI_IO11]
ldc_set_location -site {G16} [AR_MISO_IO12]
ldc_set_location -site {F17} [AR_SCK_IO13]
ldc_set_location -site {T17} [AR_IO14]
ldc_set_location -site {U17} [AR_AREF]
ldc_set_location -site {U19} [AR_SDA]
ldc_set_location -site {U18} [AR_SCL]
ldc_set_location -site {U20} [AR_RESET]
```

```
// XO4 Raspberry Pi Connections
ldc_set_location -site {T6} [get_ports RASP_IO02]
ldc_set_location -site {V1} [get_ports RASP_IO03]
ldc_set_location -site {U2} [get_ports RASP_IO04]
ldc_set_location -site {U3} [get_ports RASP_IO05]
ldc_set_location -site {U4} [get_ports RASP_IO06]
ldc_set_location -site {T5} [get_ports RASP_IO07]
ldc_set_location -site {T4} [get_ports RASP_IO08]
ldc_set_location -site {R7} [get_ports RASP_IO09]
ldc_set_location -site {R6} [get_ports RASP_IO10]
ldc_set_location -site {T3} [get_ports RASP_IO11]
ldc_set_location -site {V4} [get_ports RASP_IO12]
ldc_set_location -site {U5} [get_ports RASP_IO13]
ldc_set_location -site {P4} [get_ports RASP_IO14]
ldc_set_location -site {N5} [get_ports RASP_IO15]

ldc_set_location -site {W4} [get_ports RASP_IO16]
ldc_set_location -site {N6} [get_ports RASP_IO17]
ldc_set_location -site {N7} [get_ports RASP_IO18]
ldc_set_location -site {W3} [get_ports RASP_IO19]
ldc_set_location -site {Y2} [get_ports RASP_IO20]
ldc_set_location -site {Y3} [get_ports RASP_IO21]
ldc_set_location -site {P6} [get_ports RASP_IO22]
ldc_set_location -site {R3} [get_ports RASP_IO23]
```

```
ldc_set_location -site {R4} [get_ports RASP_IO24]
ldc_set_location -site {R5} [get_ports RASP_IO25]
ldc_set_location -site {P7} [get_ports RASP_IO26]
ldc_set_location -site {P5} [get_ports RASP_IO27]
ldc_set_location -site {T7} [get_ports RASP_ID_SC]
ldc_set_location -site {V5} [get_ports RASP_ID_SD]
```

```
// XO4 VERSA Connections
ldc_set_location -site {F8} [get_ports EXPCON_IO0]
ldc_set_location -site {G8} [get_ports EXPCON_IO1]
ldc_set_location -site {F9} [get_ports EXPCON_IO2]
ldc_set_location -site {F7} [get_ports EXPCON_IO3]
ldc_set_location -site {E7} [get_ports EXPCON_IO4]
ldc_set_location -site {E6} [get_ports EXPCON_IO5]
ldc_set_location -site {D5} [get_ports EXPCON_IO6]
ldc_set_location -site {C3} [get_ports EXPCON_IO7]
ldc_set_location -site {D6} [get_ports EXPCON_IO8]
ldc_set_location -site {C4} [get_ports EXPCON_IO9]
ldc_set_location -site {F10} [get_ports EXPCON_IO10]
// XO4 VERSA Connections Continued
ldc_set_location -site {C5} [get_ports EXPCON_IO11]
ldc_set_location -site {C6} [get_ports EXPCON_IO12]
ldc_set_location -site {B2} [get_ports EXPCON_IO13]
ldc_set_location -site {D7} [get_ports EXPCON_IO14]
ldc_set_location -site {A12} [get_ports EXPCON_IO15]
ldc_set_location -site {D8} [get_ports EXPCON_IO16]
ldc_set_location -site {C8} [get_ports EXPCON_IO17]
ldc_set_location -site {D9} [get_ports EXPCON_IO18]
ldc_set_location -site {E10} [get_ports EXPCON_IO19]
ldc_set_location -site {C9} [get_ports EXPCON_IO20]
ldc_set_location -site {G11} [get_ports EXPCON_IO21]
ldc_set_location -site {E11} [get_ports EXPCON_IO22]
ldc_set_location -site {D11} [get_ports EXPCON_IO23]
ldc_set_location -site {F11} [get_ports EXPCON_IO24]
ldc_set_location -site {D12} [get_ports EXPCON_IO25]
ldc_set_location -site {F12} [get_ports EXPCON_IO26]
ldc_set_location -site {D13} [get_ports EXPCON_IO27]
ldc_set_location -site {C14} [get_ports EXPCON_IO28]
ldc_set_location -site {E12} [get_ports EXPCON_IO29]
ldc_set_location -site {D14} [get_ports EXPCON_IO30]
ldc_set_location -site {C15} [get_ports EXPCON_IO31]

ldc_set_location -site {C17} [get_ports EXPCON_IO32]
ldc_set_location -site {D15} [get_ports EXPCON_IO33]
ldc_set_location -site {C18} [get_ports EXPCON_IO34]
ldc_set_location -site {D16} [get_ports EXPCON_IO35]
ldc_set_location -site {C19} [get_ports EXPCON_IO36]
ldc_set_location -site {D17} [get_ports EXPCON_IO37]
ldc_set_location -site {D18} [get_ports EXPCON_IO38]
ldc_set_location -site {C20} [get_ports EXPCON_IO39]
ldc_set_location -site {E16} [get_ports EXPCON_IO40]
ldc_set_location -site {E13} [get_ports EXPCON_IO41]
ldc_set_location -site {F13} [get_ports EXPCON_IO42]
ldc_set_location -site {F15} [get_ports EXPCON_IO43]
```

```
ldc_set_location -site {G15} [get_ports EXPCON_IO44]
ldc_set_location -site {G12} [get_ports EXPCON_IO45]
ldc_set_location -site {D22} [get_ports EXPCON_OSC]
ldc_set_location -site {A10} [get_ports EXPCON_CLKIN]
ldc_set_location -site {A21} [get_ports EXPCON_CLKOUT]
ldc_set_location -site {C13} [get_ports HPE_RESOUT#]
ldc_set_location -site {G9} [get_ports HPE_CARDSEL#]
```

References

- MachXO4 web page
- MachXO4 Family Data Sheet (FPGA-DS-02125)
- MachXO4 Programming and Configuration User Guide (FPGA-TN-02393)
- MachXO4 Soft Error Detection (SED) and Correction (SEC) User Guide (FPGA-TN-02406)
- Programming Cables User Guide (FPGA-UG-02042)
- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.1, April 2026

Section	Change Summary
All	Updated device name to *LFMXO4-110HC*.

Introduction	• Updated the MachXO4 device description to *FPGA.*
	• Updated device name to *LFMXO4-110HC.*
	• Removed reference to *Raspberry Pi Demo Guide.*
	• Updated the Features section.
	  • Removed ASC-related capability descriptions.
	  • Removed *voltage*, *current* and *temperature* monitoring feature.

Applying Power to the Board	Updated device name of note 1 in Table 2.2. MachXO4 Power Rail Options to *LFMXO4LF-110HC.*
JTAG / I2C Programming	Updated the Lattice Radiant software requirement version to *2025.2 or later*.
MachXO4 Device Clock Sources	Removed *Platform Manager* reference.
Headers and Test Connections	Updated MachXO4 ball location in Table 5.10. Raspberry Pi JP3 Header Pin Connections.
LEDs and Switches	• Added a Seven-Segment Display section. • Updated LED pin locations in Table 7.3. LED Signals. • Updated Figure 7.3. Push Button SW5 Circuit Design and Figure 7.4. Board LEDs. • Updated the LVDS Output Pins section. • Updated test points in Table 7.5. LVDS Test Points.
Software Requirements	• Updated the Lattice Radiant software version to *2025.2 or later*. • Updated the Lattice Radiant Programmer version to *2025.2 or later*.
Appendix C – User Defined Constraint File	• Renamed previous Appendix D – User Defined Preference File Listing to *User Defined Constraint File* and moved it to Appendix C. • Reworked section content.
Appendix C – Predefined Preference File Listing	Removed this section.

Revision 1.0, December 2025

Section	Change Summary
All	Initial release.

www.latticesemi.com