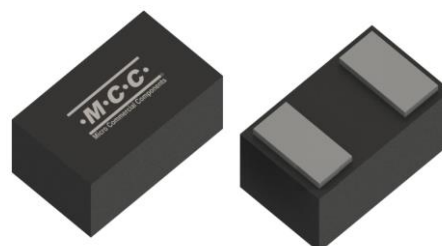


## 1-Line Bi-directional Ultra Low Capacitance ESD

### Features

- Transient protection:
  - IEC 61000-4-2 (ESD)  $\pm 15\text{kV}$  (Air),  $\pm 12\text{kV}$  (Contact)
  - IEC 61000-4-5 (Lightning) 4A (8/20 $\mu\text{s}$ )
- Bi-directional ESD protection of single line
- Reverse working voltage,  $V_{\text{RWM}}$ : 1.5V
- Low capacitance: 0.2pF
- Low clamping voltage: 3.25V
- Low reverse leakage current: 100nA max at  $V_{\text{R}} = 1.5\text{V}$
- Solid-state silicon-avalanche



CSP1006-2



### Applications

- Thunderbolt interface
- USB3.1 and USB3.0 interfaces
- USB Type-C interface
- DisplayPort interface
- Hand held portable applications
- Consumer electronics

### Mechanical Data

- Package: CSP1006-2
- Moisture Sensitivity Level 1, per J-STD-020
- Halogen Free. "Green" Device <sup>(Note1)</sup>
- Epoxy Meets UL 94 V-0 Flammability Rating
- Lead Free Finish/RoHS Compliant ("P" Suffix Designates RoHS Compliant. See Ordering Information)

### Body Marking and Pin Layout

Marking Code	Simplified Outline	Internal Structure
	 Transparent top view	

### Ordering Information

Product Name	Packing info
CSPSBULC1V5LB-TP	10K pcs/reel

For packaging details, visit our website at <https://www.mccsemi.com/Package/List>

## 1-Line Bi-directional Ultra Low Capacitance ESD

### Maximum Ratings (T<sub>A</sub>=25°C unless otherwise specified)

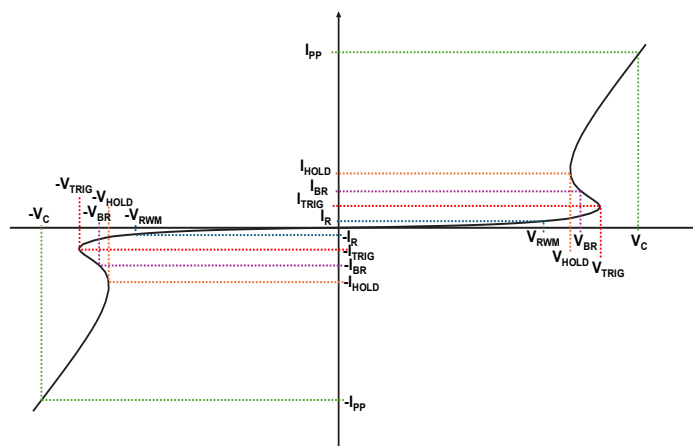
Parameter		Symbol	Rating	Unit
IEC61000-4-2(ESD)	Air	V <sub>ESD</sub>	±15	kV
	Contact	V <sub>ESD</sub>	±12	kV
Peak Pulse Current (8/20μs) (Note 2)		I <sub>PP</sub>	4	A
Peak Pulse Power (8/20μs) (Note 2)		P <sub>PK</sub>	13	W
Operating Temperature Range		T <sub>J</sub>	-55 to +125	°C
Storage Temperature Range		T <sub>STG</sub>	-55 to +150	°C

Note:

- Halogen free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and 1000ppm antimony compounds.
- Non-repetitive current pulse 8/20μs exponential decay waveform according to IEC61000-4-5.

### Parameter Definition

Symbol	Parameter
V <sub>RWM</sub>	Peak Reverse Working Voltage
I <sub>R</sub>	Reverse Leakage Current @ V <sub>RWM</sub>
V <sub>BR</sub>	Breakdown Voltage @ I <sub>T</sub>
I <sub>T</sub>	Test Current
I <sub>PP</sub>	Maximum Reverse Peak Pulse Current
V <sub>C</sub>	Clamping Voltage @ I <sub>PP</sub>
V <sub>TRIG</sub>	Reverse Trigger Voltage
I <sub>TRIG</sub>	Reverse Trigger Current
V <sub>HOLD</sub>	Reverse Holding Voltage
I <sub>HOLD</sub>	Reverse Holding Current
C <sub>J</sub>	Junction Capacitance
P <sub>PK</sub>	Peak Pulse Power



### Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V <sub>RWM</sub>				1.5	V
Reverse Breakdown Voltage	V <sub>BR</sub>	I <sub>T</sub> = 1mA	4.5	6.5	8	V
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 1.5V			0.1	μA
Clamping Voltage (Note3)	V <sub>C</sub>	I <sub>PP</sub> = 1A, t <sub>p</sub> = 8/20μs		1.75	2.2	V
		I <sub>PP</sub> = 4A, t <sub>p</sub> = 8/20μs		2.9	3.25	
Clamping Voltage (Note4)	V <sub>C</sub>	I <sub>PP</sub> = 4A(TLP)		2.5		V
		I <sub>PP</sub> = 16A(TLP)		4.9		
ESD Trigger Voltage	V <sub>TRIG</sub>	t <sub>p</sub> = 100ns, T <sub>A</sub> = 25°C		6.5		V
Reverse Holding Voltage	V <sub>HOLD</sub>			1.3		V
Junction Capacitance	C <sub>J</sub>	V <sub>R</sub> = 0V, f = 1MHz		0.2	0.25	pF
Dynamic Resistance (Note4)	R <sub>DYN</sub>	TLP, t <sub>p</sub> = 100ns		0.19		Ω

Note:

- Non-repetitive current pulse 8/20μs exponential decay waveform according to IEC61000-4-5.
- TLP parameter: Z<sub>0</sub> = 50Ω, t<sub>p</sub> = 100ns, t<sub>r</sub> = 2ns, averaging window from 60ns to 80ns. R<sub>DYN</sub> is calculated from 4A to 16A.

# 1-Line Bi-directional Ultra Low Capacitance ESD

## Curve Characteristics

Fig. 1 - 8 X 20 $\mu$ s Pulse Waveform

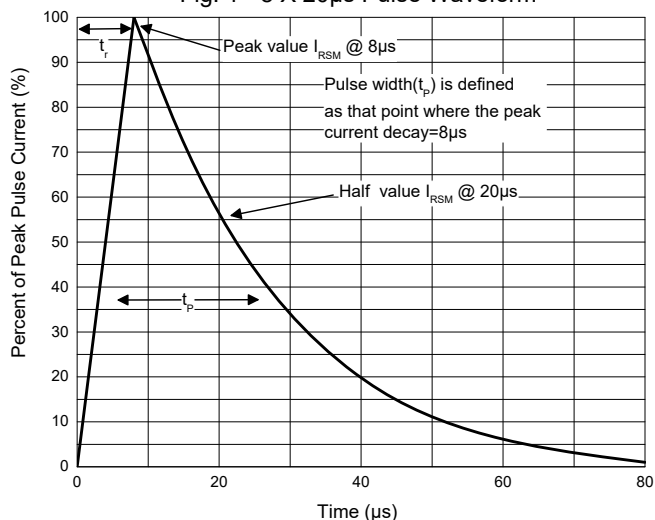


Fig. 2 - Pulse Derating Curve

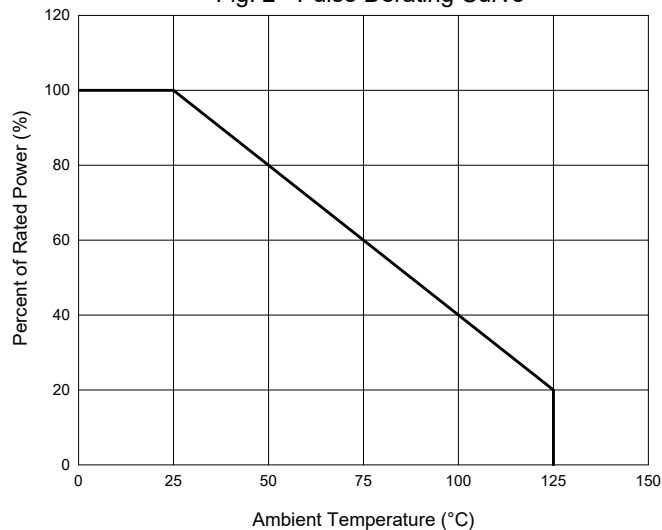


Fig. 3 - Capacitance Characteristics

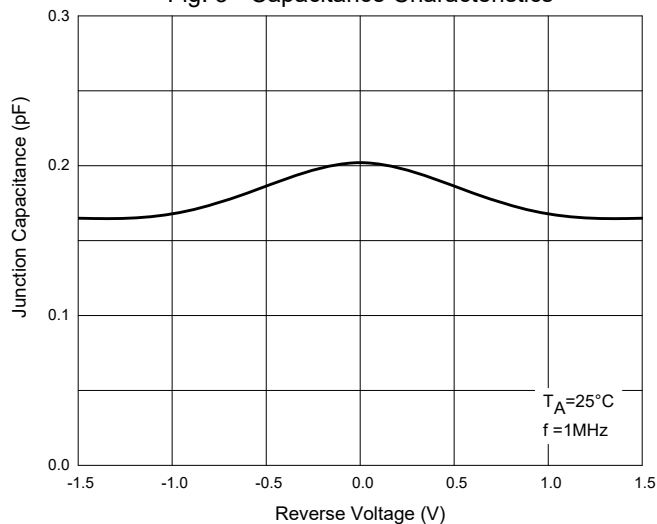


Fig. 4 - Clamping Voltage Characteristics

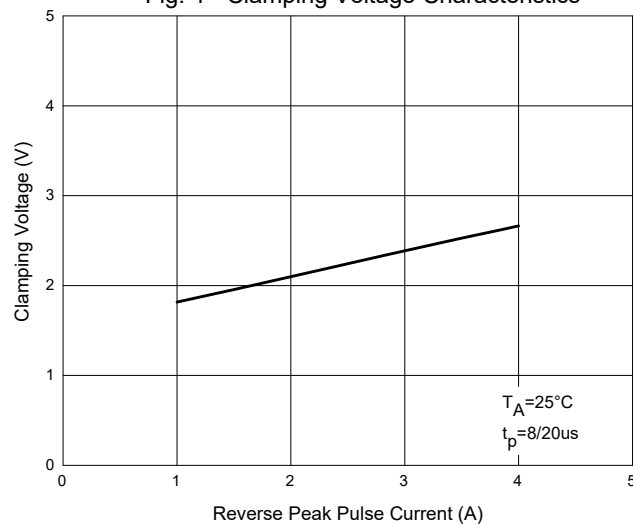


Fig. 5 - TLP Curve

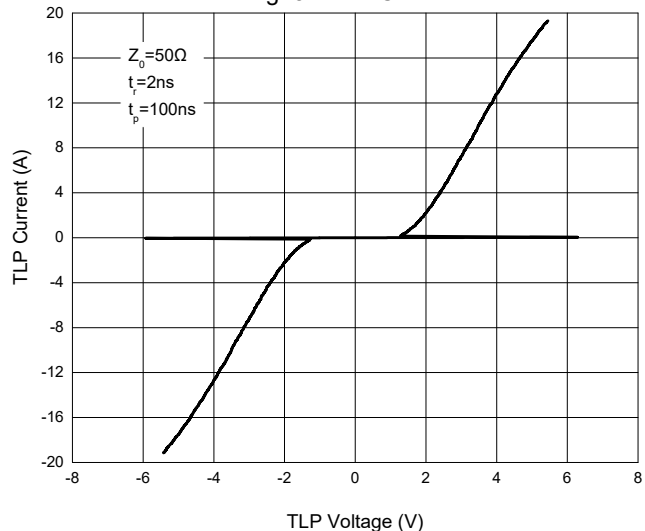
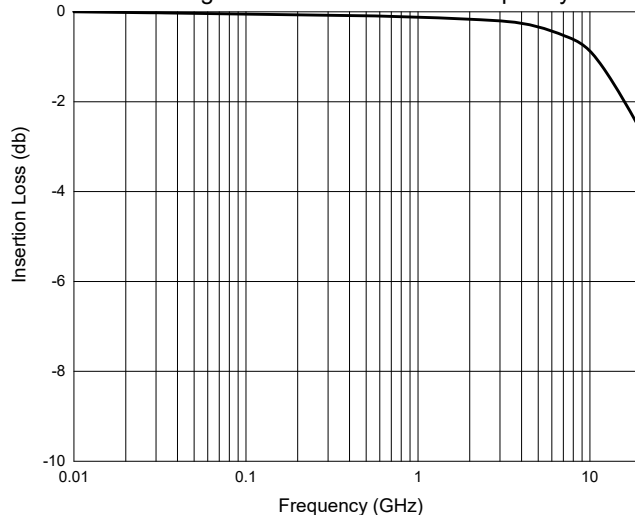


Fig. 6 - Insertion Loss VS. Frequency



## 1-Line Bi-directional Ultra Low Capacitance ESD

Fig. 7 - Return Loss VS.Frequency

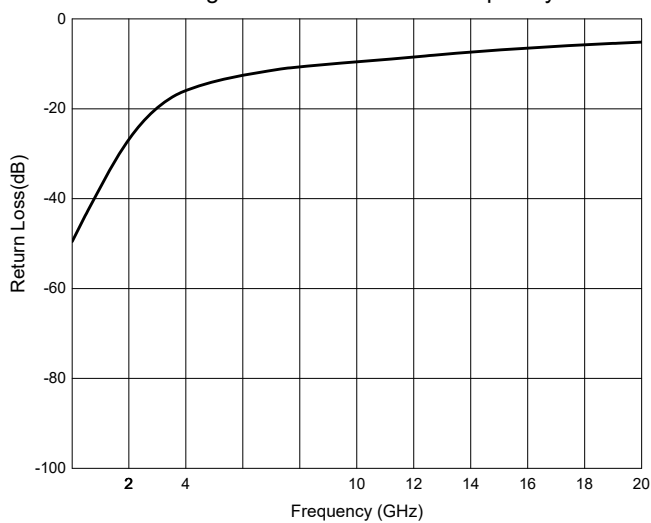
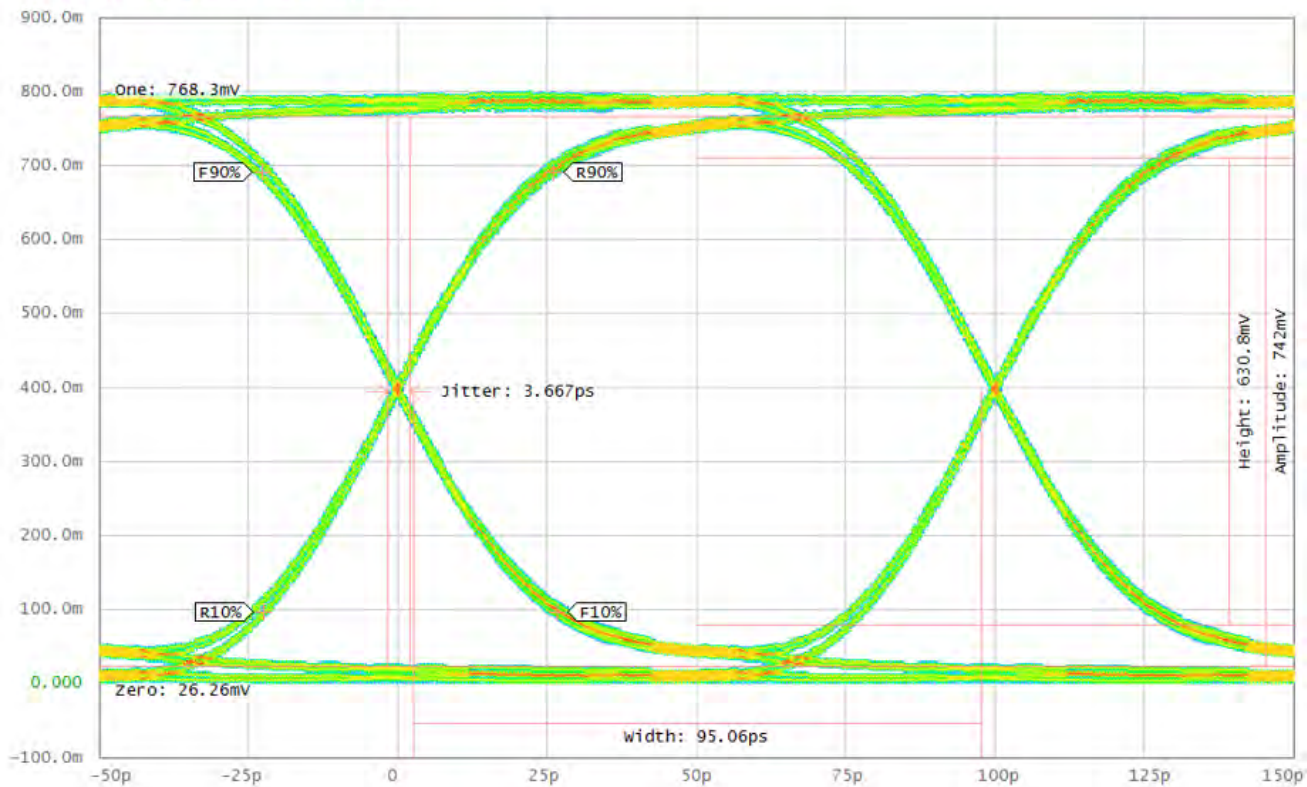
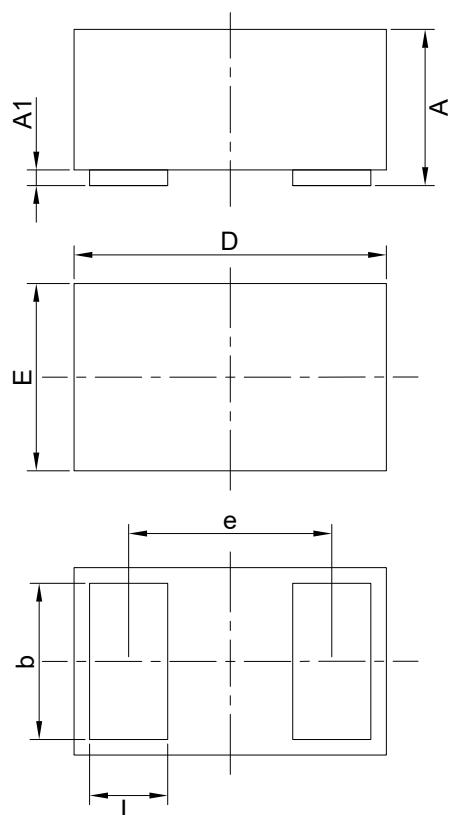


Fig. 8 - Eye Diagram (10 Gbps)

Tr3 Tdd21, High = 800mV Low = 0V, 10Gbps

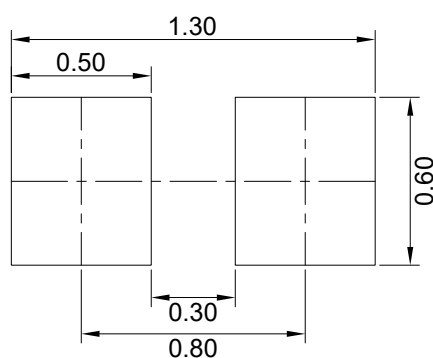


## Package Outline



DIM	INCH		MM		NOTE
	MIN	MAX	MIN	MAX	
A	0.016	0.022	0.40	0.55	
A1	0.000	0.002	0.00	0.05	
b	0.018	0.022	0.45	0.55	
D	0.037	0.041	0.95	1.05	
E	0.022	0.026	0.55	0.65	
e	0.026		0.65		TYP
L	0.008	0.012	0.20	0.30	

## Suggested Pad Layout (Unit:mm)



### Notes:

1. The suggested land pattern dimensions have been provided for reference only.
2. For further information, please refer to document IPC-7351A.

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