

# PFF3000-12-069RD

## 3000 W DC-DC Front-End Power Supply

PFF3000-12-069RD is a 3 kW DC/DC front-end converter that provides a main output 12.5 VDC from -40 to -72 VDC bus voltages to power Intermediate Bus Architectures (IBA) in high-performance and high-reliability servers, routers, and network switches.

Features include very high efficiency, high reliability, low output voltage noise, and excellent dynamic response to load / input changes.



### Key Features & Benefits

- Best-in-class, platinum equivalent efficiency
- Input voltage range: -40 to -72 VDC
- Up to 3 kW output power - 244 A output current
- Hot-plug capable
- Parallel operation with active analog current sharing
- 2 Status LEDs: DC input OK and warning / fault signaling
- High density design: 30.5 W/in<sup>3</sup>
- Form factor: 555 x 69 x 42 mm (21.85 x 2.72 x 1.65 in)
- Full digital controls for improved performance
- RoHS Compliant
- Reverse polarity, over temperature, output overvoltage, and overcurrent protections
- I2C communication interface for control, programming, and monitoring with Power Management Bus protocol



### Applications

- High Performance Servers
- Routers
- Switches

## 1. ORDERING INFORMATION

| PFF            | 3000        | -    | 12        | -    | 069   | R                        | D     | Option Code           |
|----------------|-------------|------|-----------|------|-------|--------------------------|-------|-----------------------|
| Product Family | Power Level | Dash | V1 Output | Dash | Width | Airflow                  | Input | Blank: Standard model |
| PFF Front-Ends | 3000 W      |      | 12.5 V    |      | 69 mm | R: Reversed <sup>1</sup> | D: DC |                       |

<sup>1</sup> Front to Rear

## 2. OVERVIEW

PFF3000-12-069RD power supply is a fully digital controlled, highly efficient front-end converter. It incorporates state-of-the-art technology and uses an interleaved forward converter topology with active clamp and synchronous rectification to reduce component stresses, thus providing increased system reliability and very high efficiency.

With a wide DC input voltage range and minimal linear output power derating with ambient temperature, PFF3000-12-069RD maximizes power availability in demanding server, switch, and router applications. The frontend is fan cooled and ideally suited for server integration with a matching airflow path.

Active OR-ing devices on the main output ensure no reverse load current and render the supply ideally suited for operation in redundant power systems. The standby output (12V/2A) provides power to external power distribution and management controllers. Its protection with an active OR-ing device provides for maximum reliability.

Status information is provided with two front-panel LEDs. In addition, the power supply can be controlled via I2C bus. This allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures. Cooling is managed by a fan controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I2C bus.

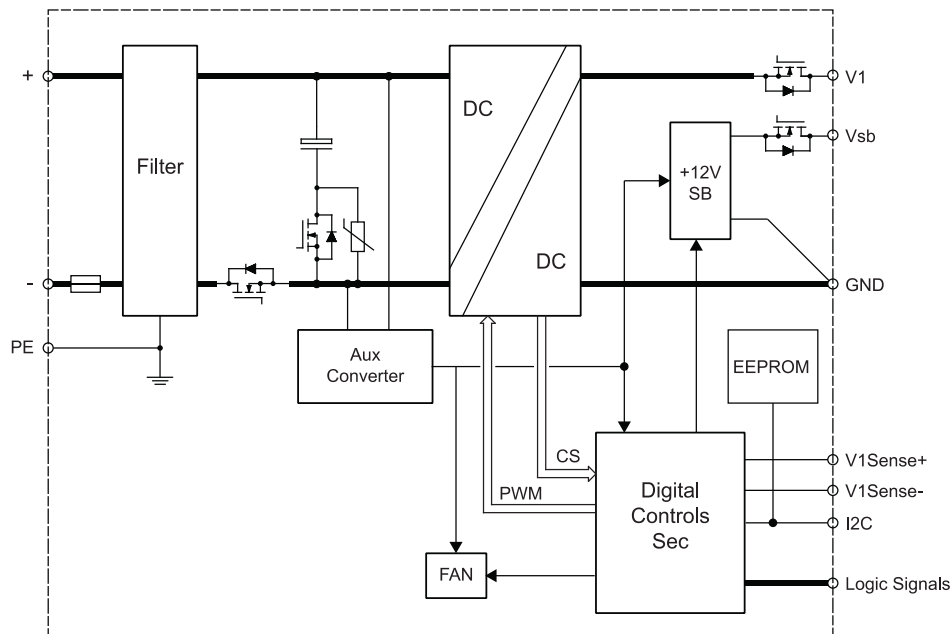


Figure 1. PFF3000-12-069RD Block Diagram

### 3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

| PARAMETER     | CONDITIONS / DESCRIPTION | MIN        | MAX | UNITS           |
|---------------|--------------------------|------------|-----|-----------------|
| $V_{i\ maxc}$ | Maximum Input            | Continuous | -75 | V <sub>DC</sub> |

### 4. INPUT

General Condition:  $T_A = 0 \dots 45\ ^\circ\text{C}$  unless otherwise noted.

| PARAMETER        | DESCRIPTION / CONDITION             | MIN                                                                      | NOM   | MAX   | UNIT            |
|------------------|-------------------------------------|--------------------------------------------------------------------------|-------|-------|-----------------|
| $V_{i\ start}$   | Minimum operating input voltage     | Communication available, DSP running                                     |       | 35    | V <sub>DC</sub> |
| $V_{i\ nom}$     | Nominal input voltage               |                                                                          | 53    |       | V <sub>DC</sub> |
| $V_i$            | Input voltage                       | Normal operation (from $V_{i\ min}$ to $V_{i\ max}$ )                    | -40   | -72   | V <sub>DC</sub> |
| $I_i$            | Input current                       | $V_i > V_{i\ min}$                                                       |       | 85    | A               |
| $I_{i\ pk}$      | Inrush current limitation           | From $V_{i\ min}$ to $V_{i\ max}$ , $T_A = 25^\circ\text{C}$             |       | 100   | A               |
| $V_{i\ on\_uv}$  | Turn-on input voltage low           | Ramping up                                                               | -42.5 | -43.5 | V <sub>DC</sub> |
| $V_{i\ off\_uv}$ | Turn-off input voltage low          | Ramping down                                                             | -38.0 | -39.5 | V <sub>DC</sub> |
| $V_{i\ on\_ov}$  | Turn-on input voltage high          | Ramping down                                                             | -68.5 | -69.5 | V <sub>DC</sub> |
| $V_{i\ off\_ov}$ | Turn-off input voltage high         | Ramping up                                                               | -72.0 | -75.0 | V <sub>DC</sub> |
| H                | Efficiency (fan power not included) | $V_{i\ nom}, 0.2 \cdot I_{i\ nom}, V_{i\ nom}, T_A = 25\ ^\circ\text{C}$ | 90.0  | 93.8  | %               |
|                  |                                     | $V_{i\ nom}, 0.5 \cdot I_{i\ nom}, V_{i\ nom}, T_A = 25\ ^\circ\text{C}$ | 94.0  | 95    | %               |
|                  |                                     | $V_{i\ nom}, I_{i\ nom}, V_{i\ nom}, T_A = 25\ ^\circ\text{C}$           | 91.0  | 93    | %               |

#### 4.1 INPUT FUSE

Fast-acting 100 A input fuse in series on minus DC rail inside the PSU protects against severe defects. The fuse is not accessible from the outside and is not therefore a serviceable part.

#### 4.2 INRUSH CURRENT & REVERSE POLARITY PROTECTION

Internal bulk capacitors will be charged through NTC resistors connected from bulk cap minus pin to the DC rail minus, thus limiting the inrush current. After the inrush phase, NTC resistors are then shorted with MOSFETs connected in parallel. Inrush control is managed by the digital controller (DSP).

Parallel connected MOSFETs in series to the DC minus rail input act as a reverse polarity blocking element (Fig. 1). In case of a short at the input voltage or input reverse polarity, these MOSFETs will open and prevent the bulk caps to be discharged via the input. Reverse polarity control is managed by a fast-acting analog circuit.

**NOTE:** In order to keep max inrush current below  $I_{i\ max}$ , it is not recommended to repeat plug-in/-out operations within 20 s.

### 4.3 INPUT UNDER-VOLTAGE

If input voltage  $V_i$  is below the input under-voltage lockout threshold  $V_{i\min}$ , main output will be inhibited. Once the input voltage returns within the normal operating voltage range, main output voltage will be enabled again and converter returns into normal operation.

### 4.4 EFFICIENCY

High efficiency is achieved by using state-of-the-art silicon power devices, thus minimizing conduction and switching losses by an optimized design and layout. Synchronous rectifiers on the output stage reduce losses in the high current output path. Fan speed is digitally controlled in order to keep all components below critical operating temperature.

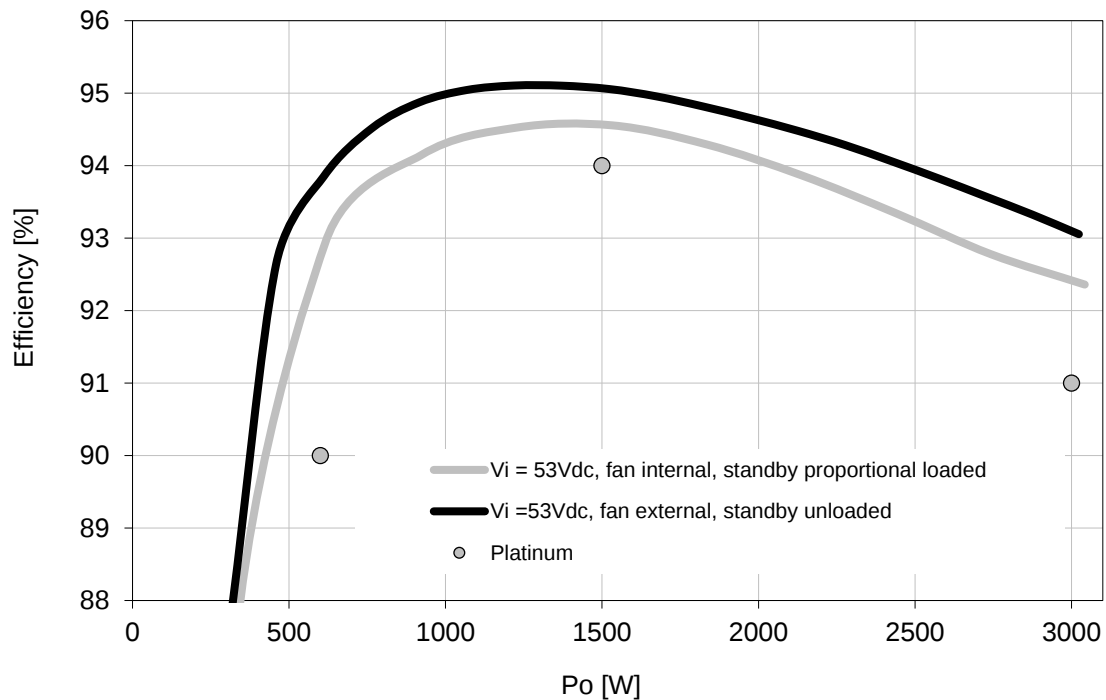


Figure 2. Efficiency vs. Load Current

## 5. OUTPUT

General Condition:  $T_A = 0...45\text{ °C}$  unless otherwise noted.

| PARAMETER                                 | DESCRIPTION / CONDITION                        | MIN                                                                                                                                                                                                                     | NOM                              | MAX   | UNIT                  |
|-------------------------------------------|------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|-------|-----------------------|
| <b>Main Output <math>V_1</math></b>       |                                                |                                                                                                                                                                                                                         |                                  |       |                       |
| $V_{1\text{ nom}}$                        | Nominal main output voltage                    | $0.5 \cdot I_{1\text{ nom}}, T_A = 25\text{ °C}$                                                                                                                                                                        | 12.5                             |       | $V_{DC}$              |
| $V_{1\text{ set}}$                        | Main output voltage set-point accuracy         | $0.5 \cdot I_{1\text{ nom}}, T_A = 25\text{ °C}$                                                                                                                                                                        | -0.5                             | +0.5  | % $V_{1\text{ nom}}$  |
| $dV_{1\text{ tot}}$                       | Total regulation                               | $V_{1\text{ min}}$ to $V_{1\text{ max}}$ , 0 to 100% $I_{1\text{ nom}}$ , $T_{A\text{ min}}$ to $T_{A\text{ max}}$                                                                                                      | -1.0                             | +1.0  | % $V_{1\text{ nom}}$  |
| $P_{1\text{ nom}}$                        | Nominal main output power                      | $V_1 = V_{1\text{ nom}} \pm 1.0\% V_{1\text{ nom}}$                                                                                                                                                                     | 3000                             |       | W                     |
| $I_{1\text{ nom}}$                        | Nominal main output current                    | $V_1 = V_{1\text{ nom}} \pm 1.0\% V_{1\text{ nom}}$                                                                                                                                                                     | 244                              |       | A                     |
| $I_{V1\text{ lim}}$                       | Current limitation on $V_1$                    |                                                                                                                                                                                                                         | See table Protection             |       |                       |
| $I_{V1\text{ ol}}$                        | Short time over load current                   | $V_1 = 12.3\text{ VDC}$ ,<br>$T_{A\text{ min}}$ to $T_{A\text{ max}}$ , maximum duration 20 ms<br>(See Section 5.2 and 6)                                                                                               |                                  | 280   | A                     |
| $I_{V1\text{ ol lim}}$                    | Current limit during short time overload $I_1$ |                                                                                                                                                                                                                         | See table Protection             |       |                       |
| $V_{1\text{ pp}}$                         | Main output ripple voltage                     | $V_{1\text{ nom}}, I_{1\text{ nom}}, 20\text{ MHz BW}$                                                                                                                                                                  |                                  | 160   | mV <sub>pp</sub>      |
| $dV_{1\text{ Load}}$                      | Load regulation                                | $V_{1\text{ nom}}, 0 - 100\% I_{1\text{ nom}}$                                                                                                                                                                          | 170                              |       | mV                    |
| $dV_{1\text{ droop}}$                     | Droop                                          | $0 - 100\% I_{1\text{ nom}}$                                                                                                                                                                                            | 0.7                              |       | mV/A                  |
| $dV_{1\text{ Line}}$                      | Line regulation                                | $V_1 = V_{1\text{ min}}...V_{1\text{ max}}$                                                                                                                                                                             | 0                                |       | mV                    |
| $dI_{\text{share}}$                       | Current sharing accuracy                       | Deviation $I_{1\text{ tot}} / N$ , $I_1 > 30\% I_{1\text{ nom}}$                                                                                                                                                        | -5                               | +5    | %                     |
| $dV_{1\text{ dyn}}$                       | Dynamic load regulation                        | $I_1 = 10\%...50\% I_{1\text{ nom}}$ ,<br>$I_{1\text{ tot}} = I_1 + \Delta I_1$ , $\Delta I_1 = 50\% I_{1\text{ nom}}$ ,<br>$dI_o / dt = 1\text{ A}/\mu\text{s}$ ,<br>recovery within 1% of $V_{1\text{ nom}}$          | -0.6                             | +0.6  | V                     |
| $T_{1\text{ rec}}$                        | Recovery time                                  |                                                                                                                                                                                                                         |                                  | 1     | ms                    |
| $t_{V1\text{ Pwr\_On}}$                   | Start-up time from DC input                    | $V_1 = 10.8 V_{DC}$                                                                                                                                                                                                     | See table on/ off signal timings |       |                       |
| $t_{V1\text{ rise}}$                      | Rise time (monotonic)                          | $V_1 = 10\%...90\% V_{1\text{ nom}}, 50\% I_{1\text{ nom}}$                                                                                                                                                             | 4.5                              |       | ms                    |
| $t_{V1\text{ holdup}}$                    | Hold-up time                                   | $0.5 \cdot I_1, V_1 = V_{1\text{ nom}}$                                                                                                                                                                                 | 2                                |       | ms                    |
| $C_{\text{load}}$                         | Capacitive loading                             | $T_A = 25\text{ °C}$                                                                                                                                                                                                    |                                  | 10000 | $\mu\text{F}$         |
| <b>Standby Output <math>V_{SB}</math></b> |                                                |                                                                                                                                                                                                                         |                                  |       |                       |
| $V_{SB\text{ nom}}$                       | Nominal standby output voltage                 | $0.5 \cdot I_{SB\text{ nom}}, T_A = 25\text{ °C}$                                                                                                                                                                       | 12.00                            |       | $V_{DC}$              |
| $V_{SB\text{ set}}$                       | Standby output set-point accuracy              | $0.5 \cdot I_{SB\text{ nom}}, T_A = 25\text{ °C}$                                                                                                                                                                       | -1.0                             | +1.0  | % $V_{SB\text{ nom}}$ |
| $dV_{SB\text{ tot}}$                      | Total regulation                               | $V_{1\text{ min}}$ to $V_{1\text{ max}}$ , 0 to 100% $I_{SB\text{ nom}}$ , $T_{A\text{ min}}$ to $T_{A\text{ max}}$                                                                                                     | -1.0                             | +1.0  | % $V_{SB\text{ nom}}$ |
| $P_{SB\text{ nom}}$                       | Nominal standby output power                   | $V_{SB} = V_{SB\text{ nom}} \pm 0.5\% V_{SB\text{ nom}}$                                                                                                                                                                | 24                               |       | W                     |
| $I_{SB\text{ nom}}$                       | Nominal standby output current                 | $V_{SB} = V_{SB\text{ nom}} \pm 0.5\% V_{SB\text{ nom}}$                                                                                                                                                                | 2                                |       | A                     |
| $V_{SB\text{ pp}}$                        | Standby output ripple voltage                  | $V_{SB\text{ nom}}, I_{SB\text{ nom}}, 20\text{ MHz BW}$                                                                                                                                                                |                                  | 120   | mV <sub>pp</sub>      |
| $I_{VSB\text{ lim}}$                      | Current limit                                  |                                                                                                                                                                                                                         | See table Protection             |       |                       |
| $t_{VSB\text{ lim}}$                      | Over load current limit time on $V_{SB}$       | Time to hit hiccup when in over current                                                                                                                                                                                 | See table Protection             |       |                       |
| $dV_{SB}$                                 | Load regulation                                | $0 - 100\% I_{SB\text{ nom}}$                                                                                                                                                                                           | 220                              |       | mV                    |
|                                           | Droop                                          | $0 - 100\% I_{SB\text{ nom}}$                                                                                                                                                                                           | 110                              |       | mV/A                  |
| $dV_{SB\text{ dyn}}$                      | Dynamic load regulation                        | $I_{SB} = 5\%...50\% I_{SB\text{ nom}}$ ,<br>$I_{SB\text{ tot}} = I_1 + \Delta I_1$ , $\Delta I_{SB} = 50\% I_{SB\text{ nom}}$ ,<br>$dI_o / dt = 1\text{ A}/\mu\text{s}$ ,<br>recovery within 1% of $V_{SB\text{ nom}}$ | -0.6                             | +0.6  | V                     |
| $T_{SB\text{ rec}}$                       | Recovery time                                  |                                                                                                                                                                                                                         |                                  | 5     | ms                    |
| $t_{VSB\text{ Pwr\_On}}$                  | Start-up time from DC input                    | $V_{SB} = 90\% V_{SB\text{ nom}}$                                                                                                                                                                                       | See table on/ off signal timings |       |                       |
| $t_{VSB\text{ rise}}$                     | Rise time (monotonic)                          | $V_{SB} = 10\%...90\% V_{SB\text{ nom}}$                                                                                                                                                                                | 0.1                              |       | ms                    |
| $t_{VSB\text{ holdup}}$                   | Hold-up time                                   | $I_{SB} = 0...2\text{ A}, V_1 > 48\text{ V}$                                                                                                                                                                            | 5                                | 260   | ms                    |
| $C_{\text{load}}$                         | Capacitive loading                             | $T_A = 25\text{ °C}$                                                                                                                                                                                                    | 1000                             |       | $\mu\text{F}$         |

## 5.1 OUTPUT VOLTAGE RIPPLE

The internal output capacitance at the power supply output (behind OR-ing element) is minimized to prevent disturbances during hot plug. In order to provide low output ripple voltage in the application, external capacitors should be added close to the power supply output. The setup of *Figure 3* has been used to evaluate suitable capacitor types. The capacitor combinations of Table 1 and Table 2 should be used to reduce the output ripple voltage.

The ripple voltage is measured with 20 MHz BWL, close to the external capacitors.

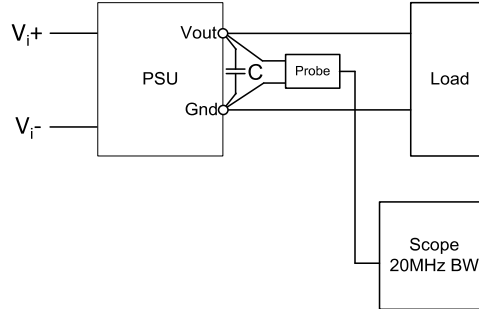


Figure 3. Output Ripple Test Setup

**NOTE:** Care must be taken when using ceramic capacitors with a total capacitance of 1  $\mu$ F to 50  $\mu$ F on output V1, due to their high quality factor the output ripple voltage may be increased in certain frequency ranges due to resonance effects.

| External Capacitor V1                                                                                    | dV1max | Unit |
|----------------------------------------------------------------------------------------------------------|--------|------|
| 2Pcs 47 $\mu$ F/16V/X5R/1210                                                                             | 160    | mVpp |
| 1Pcs 1000 $\mu$ F/16V/Low ESR Aluminum/ $\varnothing$ 10x20                                              | 160    | mVpp |
| 1Pcs 270 $\mu$ F/16V/Conductive Polymer/ $\varnothing$ 8x12                                              | 160    | mVpp |
| 2Pcs 47 $\mu$ F/16V/X5R/1210 plus 1Pcs 270 $\mu$ F Conductive Polymer OR 1Pcs 1000 $\mu$ F Low ESR AlCap | 90     | mVpp |

Table 1. Suitable Capacitors for V1

| External capacitor VSB                                      | dVSBmax | Unit |
|-------------------------------------------------------------|---------|------|
| 1Pcs 270 $\mu$ F/16V/Conductive Polymer/ $\varnothing$ 8x12 | 120     | mVpp |

Table 2. Suitable Capacitors for VSB

The output ripple voltage on VSB is influenced by the main output V1. Evaluating VSB output ripple must be done when maximum load is applied to V1.

## 5.2 OUTPUT ISOLATION

Main and standby outputs and all signals are galvanic isolated from the chassis and protective earth connection, although the applied voltage  $V_i$  has not to exceed  $75 V_{pk}$  in order to prevent catastrophic damage to the PSU.

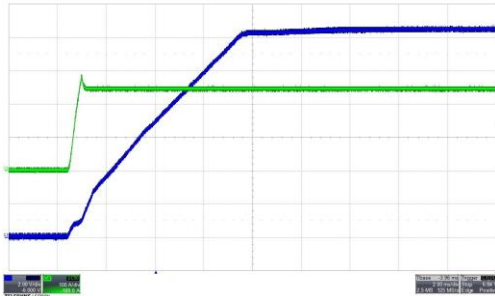


Figure 4. Turn-on at  $V_i = V_{i-nom}$ ,  $I_i = I_{i-nom}$  (2 ms/div)  
CH3 (blue):  $V_i$  (2 V/div), CH4 (green):  $I_i$  (100 A/div)

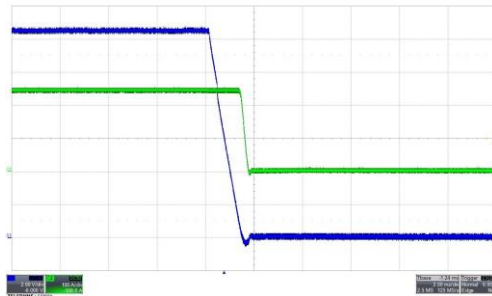


Figure 5. Turn-off at  $V_i = V_{i-nom}$ ,  $I_i = I_{i-nom}$  (2 ms/div)  
CH3 (blue):  $V_i$  (2 V/div), CH4 (green):  $I_i$  (100 A/div)

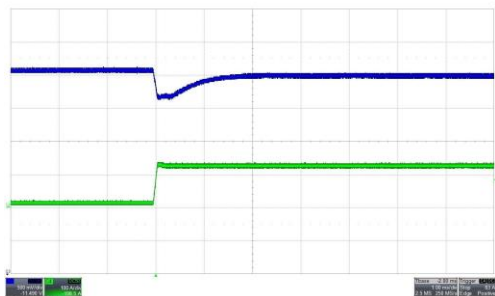


Figure 6. Load transient on  $V_i$ , 12 A to 122 A (1 ms/div)  
CH3 (blue):  $V_i$  (0.5 V/div), CH4 (green):  $I_i$  (100 A/div)

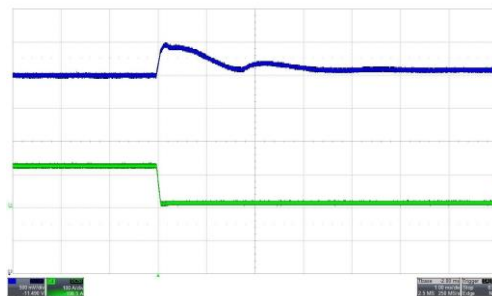


Figure 7. Load transient on  $V_i$ , 122 A to 12 A (1 ms/div)  
CH3 (blue):  $V_i$  (0.5 V/div), CH4 (green):  $I_i$  (100 A/div)

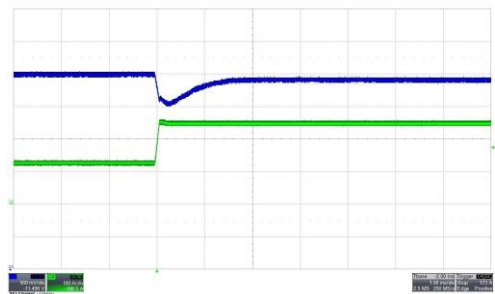


Figure 8. Load transient on  $V_i$ , 122 A to 244 A (1 ms/div)  
CH3 (blue):  $V_i$  (0.5 V/div), CH4 (green):  $I_i$  (100 A/div)

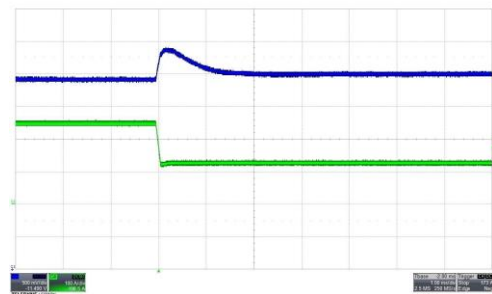


Figure 9. Load transient on  $V_i$ , 244 A to 122 A (1 ms/div)  
CH3 (blue):  $V_i$  (0.5 V/div), CH3 (green):  $I_i$  (100 A/div)

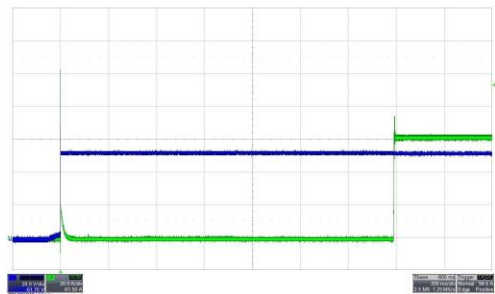


Figure 10. Inrush current,  $V_i = V_{i-nom}$ ,  $I_i = I_{i-nom}$  (200 ms/div)  
CH3 (blue):  $V_i$  (20 V/div), CH4 (green):  $I_i$  (20 A/div)

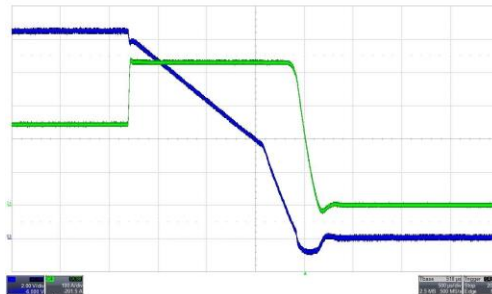


Figure 11. Short circuit on main output (500  $\mu$ s/div)  
CH3 (blue):  $V_i$  (2 V/div), CH4 (green):  $I_i$  (100 A/div)

## 6. PROTECTION

| PARAMETER              | DESCRIPTION / CONDITION                                 | MIN                                                                   | NOM  | MAX  | UNIT             |
|------------------------|---------------------------------------------------------|-----------------------------------------------------------------------|------|------|------------------|
| F                      | Input fuse                                              | Not user-accessible, quick-acting                                     |      |      | A                |
| V <sub>1</sub> OV      | Overvoltage threshold on V <sub>1</sub>                 | 13.6                                                                  | 14.2 | 14.8 | V <sub>DC</sub>  |
| t <sub>OV V1</sub>     | Overvoltage latch-off time on V <sub>1</sub>            |                                                                       |      | 1    | ms               |
| V <sub>SB</sub> OV     | Overvoltage threshold on V <sub>SB</sub>                | 13.3                                                                  | 13.9 | 14.5 | V <sub>DC</sub>  |
| t <sub>OV VSB</sub>    | Overvoltage latch-off time on V <sub>SB</sub>           |                                                                       |      | 1    | ms               |
| I <sub>V1</sub> lim    | Current limitation on V <sub>1</sub>                    | $T_a < 45^{\circ}\text{C}$<br>$T_a = 60^{\circ}\text{C}$ <sup>1</sup> |      |      | A                |
| t <sub>V1</sub> lim    | Current limit blanking time on V <sub>1</sub>           | Time to latch off when in over current                                |      |      | ms               |
| I <sub>V1 ol</sub> lim | Current limit during short time overload I <sub>1</sub> | 292                                                                   |      | 308  | A                |
| I <sub>V1</sub> SC     | Max Short Circuit Current I <sub>1</sub>                | I <sub>1</sub> < 3 V                                                  |      |      | 350 <sup>2</sup> |
| t <sub>V1</sub> SC     | Short circuit latch off time                            | Measured from V <sub>1</sub> < 8.0 V                                  |      |      | 1                |
| I <sub>VSB</sub> lim   | Current limitation on V <sub>SB</sub>                   | 2.5                                                                   |      | 3.5  | A                |
| t <sub>VSB</sub> lim   | Current limit blanking time on V <sub>SB</sub>          | Time to enter hiccup when in overcurrent                              |      |      | 1                |
| T <sub>SD</sub>        | Over temperature on critical points                     | Inlet ambient temperature                                             |      |      | 60               |
|                        |                                                         | Secondary Sync. MOSFETs temperature                                   |      |      | 115              |
|                        |                                                         | Secondary OR-ing MOSFETs temperature                                  |      |      | 125              |

<sup>1</sup> See *Figure 26* for linear power derating > 45°C

<sup>2</sup> Limit set don't include effects of main output capacitive discharge.

### 6.1 AUTOMATIC RETRY

Any fault condition on main output V<sub>1</sub> will shut down the main output and attempt to recover from the fault 5 times before latching off. The time between each restart attempt is 10 s. The fault latch and fault counter can be reset by disconnecting the input voltage or by toggling the PSON\_L input. If the unit operates for more than 10 min with no failure, then the failure counter will be reset automatically. A failure on the standby output V<sub>SB</sub> will shut down both outputs, whereas a failure on main output V<sub>1</sub> will only shut down this output, while V<sub>SB</sub> will continue to operate and communicate.

### 6.2 OVERVOLTAGE PROTECTION

The PSU provides a fixed threshold overvoltage (OV) protection, implemented with a hardware comparator. Once an overvoltage (OV) condition has been triggered, the supply will shut down and latch the fault condition.

### 6.3 UNDERVOLTAGE DETECTION

As both main and standby outputs are monitored, LEDs and the PWOK\_L pin will warn if V<sub>1</sub> or V<sub>SB</sub> exceed ± 7% of its nominal voltage. Output undervoltage protection is provided on both outputs. When either V<sub>1</sub> or V<sub>SB</sub> falls below 93% of its nominal voltage, the output is inhibited.

## 6.4 OUTPUT OVER-CURRENT PROTECTION

### MAIN OUTPUT

Two different over current protection features are implemented on the main output.

The 1<sup>st</sup> protection - a static over current protection will shut down the output, if the output current does exceed  $I_{V1 \text{ lim}}$  for more than 20 ms. If the output current is increased slowly this protection will shut down the supply. The main output current limitation level  $I_{V1 \text{ lim}}$  will decrease if the ambient (inlet) temperature increases beyond 45 °C (see *Figure 26*).

The 2<sup>nd</sup> protection - a substantially rectangular output characteristic controlled by a software feedback loop. This protects the power supply and system during the 20 ms blanking time of the static over current protection. If the output current is rising fast and reaches  $I_{V1 \text{ ol lim}}$ , the supply will immediately reduce its output voltage to prevent the output current from exceeding  $I_{V1 \text{ ol lim}}$ . When the output current is reduced below  $I_{V1 \text{ ol lim}}$ , the output voltage will return to its nominal value.

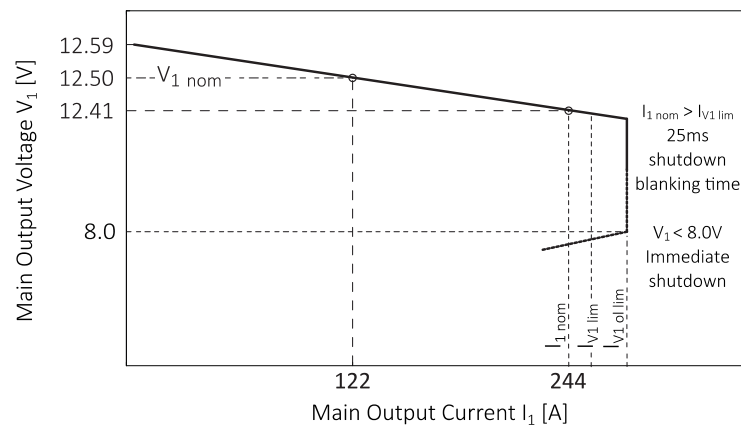


Figure 12. Current limitation on main output

### STANDBY OUTPUT

On the standby output a hiccup type over current protection is implemented. This protection will shut down the standby output immediately when standby current reaches or exceeds  $I_{\text{SB lim}}$ . After an off-time of 1s the output automatically tries to restart. If the overload condition is removed the output voltage will reach again its nominal value  $V_{\text{SB}} = V_{\text{SB nom}} \pm 1\%$ .

At continuous overload condition the output will repeatedly trying to restart with 1s intervals.

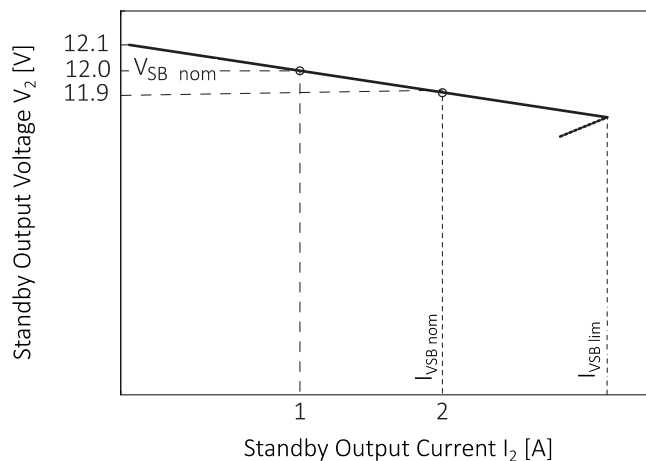


Figure 13. Current limitation on standby output

## 7. MONITORING

| PARAMETER     | DESCRIPTION / CONDITION | MIN                                                | NOM          | MAX          | UNIT   |
|---------------|-------------------------|----------------------------------------------------|--------------|--------------|--------|
| $V_{I\ mon}$  | Input voltage           | $V_{I\ min} \leq V_I \leq V_{I\ max}$              | -2.5         | +2.5         | %      |
| $I_{I\ mon}$  | Input current           | $I_I > 20\ A$<br>$8\ A < I_I \leq 20\ A$           | -5.0<br>-1   | +5.0<br>+1   | %<br>A |
| $P_{I\ mon}$  | Input power             | $P_I > 700\ W$<br>$330\ W < P_I \leq 700\ W$       | -5.0<br>-35  | +5.0<br>+35  | %<br>W |
| $V_{1\ mon}$  | Main output voltage     |                                                    | -2           | +2           | %      |
| $I_{1\ mon}$  | Main output current     | $I_1 > 134\ A$<br>$24\ A < I_1 \leq 75\ A$         | -2.0<br>-1.5 | +2.0<br>+1.5 | %<br>A |
| $P_{o1\ mon}$ | Main output power       | $P_{o1} > 400\ W$<br>$300\ W < P_{o1} \leq 400\ W$ | -5<br>-20    | +5<br>+20    | %<br>W |
| $V_{SB\ mon}$ | Standby voltage         |                                                    | -2           | +2           | %      |
| $I_{SB\ mon}$ | Standby current         |                                                    | -0.2         | 0.2          | A      |
| $P_{SB\ mon}$ | Standby output power    |                                                    | -2.4         | 2.4          | W      |

## 8. SIGNALING AND CONTROL

### 8.1 ELECTRICAL CHARACTERISTICS

| PARAMETER                          | DESCRIPTION / CONDITION                                                                 | MIN                      | NOM  | MAX  | UNIT |
|------------------------------------|-----------------------------------------------------------------------------------------|--------------------------|------|------|------|
| PSKILL / PSKILL_IN / PSON_L inputs |                                                                                         |                          |      |      |      |
| V <sub>IL</sub>                    | Input low level voltage                                                                 | -0.2                     |      | +0.8 | V    |
| V <sub>IH</sub>                    | Input high level voltage                                                                | 2.0                      |      | 3.6  | V    |
| I <sub>IL, H</sub>                 | Maximum input sink or source current                                                    | 0                        |      | 1    | mA   |
| R <sub>pu PSKILL(IN)</sub>         | Internal pull-up resistor on PSKILL                                                     |                          | 10   |      | kΩ   |
| R <sub>puPSON_L</sub>              | Internal pull-up resistor on PSON_L                                                     |                          | 10   |      | kΩ   |
| PWOK_L output                      |                                                                                         |                          |      |      |      |
| V <sub>OL</sub>                    | Output level voltage                                                                    | I <sub>sink</sub> < 4 mA | -0.2 | 0.4  | V    |
| V <sub>pu PWOK_L</sub>             | External pull-up voltage                                                                |                          |      | 12   | V    |
| R <sub>pu PWOK_L</sub>             | Recommended external pull-up resistor on PWOK_L at V <sub>pu PWOK_L</sub> = 3.3 V       |                          | 10   |      | kΩ   |
| Low level output                   | All outputs are turned on and within regulation                                         |                          |      |      |      |
| High level output                  | In standby mode or V <sub>1</sub> / V <sub>SB</sub> have triggered a fault condition    |                          |      |      |      |
| INOK_L output                      |                                                                                         |                          |      |      |      |
| V <sub>OL</sub>                    | Output low level voltage                                                                | I <sub>sink</sub> < 4 mA | -0.2 | 0.4  | V    |
| V <sub>puINOK_L</sub>              | External pull-up voltage                                                                |                          |      | 12   | V    |
| R <sub>pu INOK_L</sub>             | Recommended external pull-up resistor on INOK_L at V <sub>pu INOK_L</sub> = 3.3 V       |                          | 10   |      | kΩ   |
| Low level output                   | Input voltage is within range for PSU to operate                                        |                          |      |      |      |
| High level output                  | Input voltage is not within range for PSU to operate                                    |                          |      |      |      |
| SMB_ALERT_L output                 |                                                                                         |                          |      |      |      |
| V <sub>OL</sub>                    | Output low level voltage                                                                | I <sub>sink</sub> < 4 mA | -0.2 | 0.4  | V    |
| V <sub>pu SMALT_L</sub>            | External pull-up voltage                                                                |                          |      | 12   | V    |
| R <sub>pu SMALT_L</sub>            | Recommended external pull-up resistor on SMB_ALERT_L at V <sub>pu SMALT_L</sub> = 3.3 V |                          | 10   |      | kΩ   |
| Low level output                   | PSU is in warning or failure condition                                                  |                          |      |      |      |
| High level output                  | PSU is ok                                                                               |                          |      |      |      |

## 8.2 INTERFACING WITH SIGNALS

A 15 V Zener diode is added on all signal pins versus signal ground SGND to protect internal circuits from negative and high positive voltage. Signal pins of several supplies running in parallel can be interconnected directly. A supply having no input power will not affect the signals of other PSUs running in parallel.

The current share bus pin (ISHR\_BUS) must be interconnected without any additional components; as protection element, a 15 V Zener diode is connected to the signal reference SGND. The share bus is disconnected (analog switch) from internal circuits when the power supply is switched off.

## 8.3 LED STATUS - FRONT LEDs

The PSU has two front LEDs showing its status: DC Input LED is green colored and indicates DC power ON / OFF, DC Output LED is bi-colored green and yellow and shows DC output OK or a warning/fault status as listed in Table 1.

| OPERATING CONDITION                                 | LED SIGNALING               |
|-----------------------------------------------------|-----------------------------|
| <b>IN: DC Input LED</b>                             |                             |
| DC line within range                                | Solid Green                 |
| DC line UV / OV condition                           | OFF                         |
| Bootload                                            | Blinking green: OFF (1:1)   |
| <b>OUT: DC Output LED</b>                           |                             |
| Normal Operation                                    | Solid Green                 |
| PSKILL_IN_L - Left open                             | Blinking Yellow (1:1)       |
| PSON_L - High, PSKILL_L - High                      |                             |
| Power Management Bus Command OPERATION              |                             |
| DC line UV / OV condition                           |                             |
| V1 or VSB out of regulation                         | Solid Yellow                |
| Over temperature shutdown                           |                             |
| Output over voltage shutdown ( $V_1$ or $V_{SB}$ )  |                             |
| Output under voltage shutdown ( $V_1$ or $V_{SB}$ ) |                             |
| Output over current shutdown ( $V_1$ or $V_{SB}$ )  | Blinking Yellow/Green (2:1) |
| Both FANs blocked                                   |                             |
| Over temperature warning                            |                             |
| Minor fan regulation error ( $> 5\%$ , $< 15\%$ )   |                             |
| Or one of the FANs blocked                          | Blinking Yellow/Green (1:1) |
| Bootload                                            |                             |

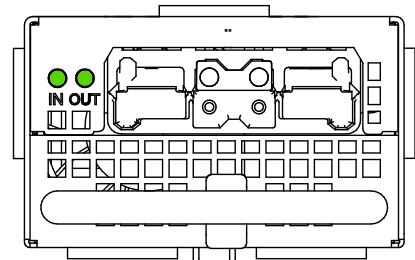


Table 3. LED Status

## 8.4 PRESENT\_L

PRESENT\_L is a trailing pin within the connector and will contact only once all other connector contacts. This active-low pin is used to indicate to a power distribution unit controller that a supply is plugged in. Maximum sink current on PRESENT\_L pin should not exceed 10 mA.

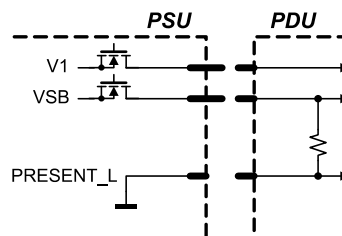


Figure 14. PRESENT\_L signal pin

## 8.5 PSKILL\_L / PSKILL\_IN\_L INPUT

PSKILL\_L input is an active-low trailing pin in the output connector and is used to disconnect the main output as soon as the power supply is being pulled out. This pin should be connected to SGND in the power distribution unit. Standby output will remain on, regardless of the PSKILL\_L input state.

PSKILL\_IN\_L input is an active-low signal pin in the input connector and is used to disconnect the main output as soon as the input connector is plugged out. This pin should be connected to SGND on the input connector mating part. Standby output will remain on, regardless of the PSKILL\_L input state.

## 8.6 DC TURN-ON / DROP-OUTS / INOK\_L

The INOK\_L signal indicates whether the DC input voltage is within the operating range and the power supply can turn on. The power supply will automatically turn-on when connected to the DC line within the operating voltage range under the condition that the PSON\_L signal is pulled low. INOK\_L is an active low open collector output that requires an external pull-up voltage to maximum 12.0 V.

## 8.7 PSON\_L INPUT

PSON\_L is an internally pulled-up (3.3 V) input signal to enable / disable the main output  $V_1$ . This active-low pin is also used to clear any latched fault condition. Timing parameters are listed in Table 2.

## 8.8 PWOK\_L SIGNAL

PWOK\_L is an open collector output that requires an external pull-up voltage to maximum 12 V, indicating whether both  $V_1$  and  $V_{SB}$  outputs are within regulation. This pin is active-low; timing parameters are listed in Table 2.

## 8.9 SIGNAL TIMING

| OPERATING CONDITION       |                                                              | MIN | MAX  | UNIT |
|---------------------------|--------------------------------------------------------------|-----|------|------|
| $t_{V1\_rise}$            | See table Output Parameter                                   |     |      |      |
| $t_{VSB\_rise}$           | See table Output Parameter                                   |     |      |      |
| $t_{INOK\_On}$            | INOK_L delay at dropout                                      | 0   | 700  | ms   |
| $t_{INOK\_On\_Pwr\_On}$   | INOK_L delay at coldstart                                    | 500 | 1800 | ms   |
| $t_{INOK\_to\_VSB\_rise}$ | INOK_L to $V_{SB}$ delay                                     | 1   | 5    | ms   |
| $t_{VSB\_Pwr\_On}$        | $V_{in}$ to $V_{SB}$ delay                                   | 520 | 1805 | ms   |
| $t_{V1\_Pwr\_On}$         | $V_{in}$ to $V_1$ delay                                      | 700 | 3000 | ms   |
| $t_{PWOK\_On}$            | $V_1$ in regulation to PWOK_L                                | 280 | 320  | ms   |
| $t_{V1\_fall}$            | monotonic                                                    |     |      |      |
| $t_{VSB\_fall}$           | monotonic                                                    |     |      |      |
| $t_{INOK\_Off}$           | INOK_L delay                                                 | 0   | 1.8  | ms   |
| $t_{INOK\_warn}$          | INOK_L to $V_1$ out of regulation ( $0.5 I_1$ ), $V_1 > 48V$ | 1.0 |      | ms   |
| $t_{V1\_holdup}$          | See table Output Parameter                                   |     |      |      |
| $t_{VSB\_holdup}$         | See table Output Parameter                                   |     |      |      |
| $t_{PWOK\_Off}$           | $V_1$ out of regulation to PWOK_L                            | 0   | 5    | ms   |
| $t_{PSON\_On}$            | PSON_L to $V_1$ in regulation                                | 150 | 170  | ms   |
| $t_{PSON\_Off}$           | PSON_L to $V_1$ out of regulation                            | 0   | 5    | ms   |
| $t_{PSKILL\_IN\_On}$      | PSKILL(IN)_L to $V_1$ in regulation                          | 150 | 170  | ms   |
| $t_{PSKILL\_IN\_Off}$     | PSKILL(IN)_L to $V_1$ out of regulation                      | 0   | 5    | ms   |

Table 4. On-/Off- Signal Timings

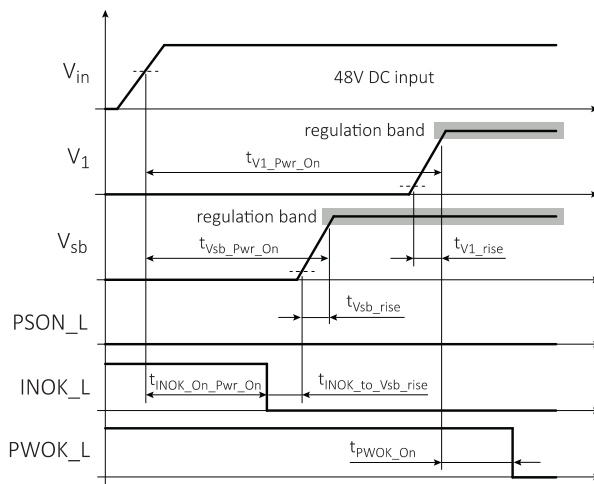


Figure 15. Power on Delay, Rise Time and Signaling

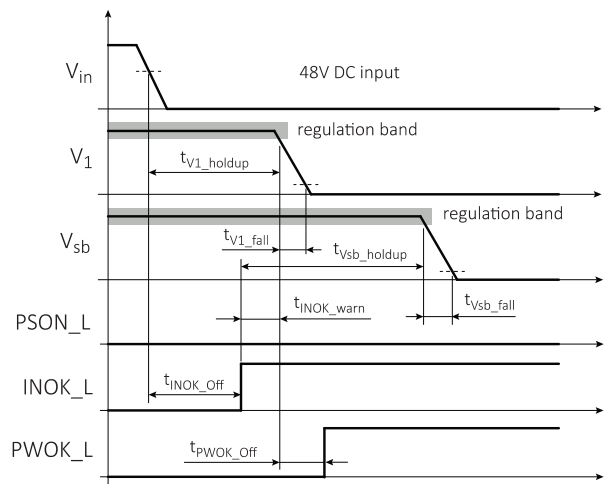


Figure 16. Power Removed Holdup, Fall Time and Signaling

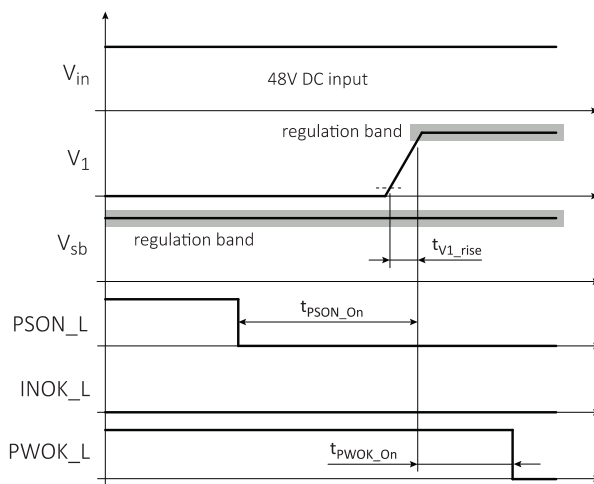


Figure 17. Turn On Delay, Rise Time and Signaling

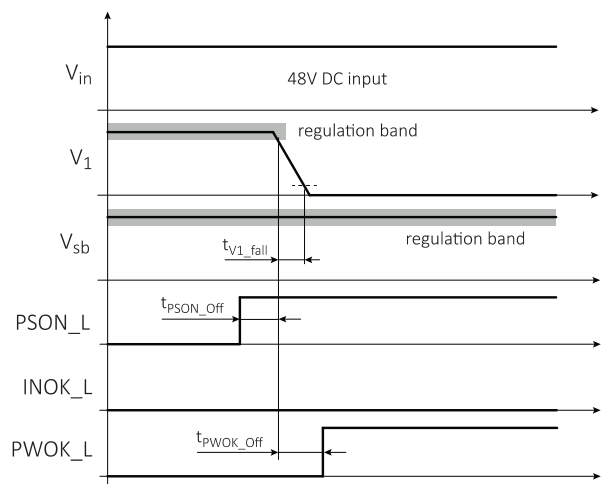


Figure 18. Turn Off, Fall Time and Signaling

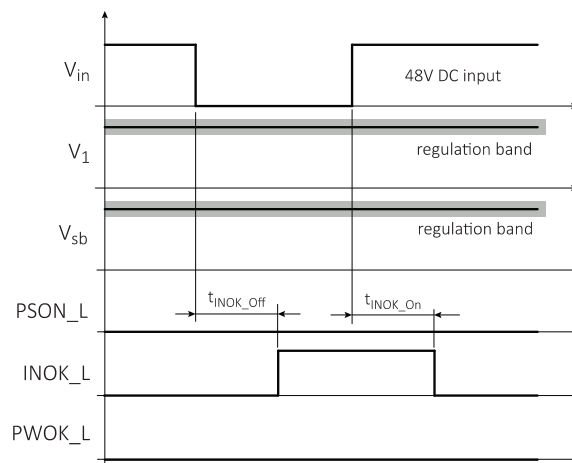


Figure 19. Dropout and Signaling

## 8.10 CURRENT SHARE

The PSU has an active current share scheme implemented for main output  $V_1$ . ISH\_BUS current share pins of all units in parallel need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHR\_BUS pin from the share bus: this will prevent dragging the output down (or up) in such cases.

Master / Slave current share function implemented by the controller uses an analog bus: the power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The output voltage increase is limited to +250 mV. Standby output uses an analog passive current-share method (droop-output voltage characteristic).

Maximum available main and stand-by power in (non)-redundant topology is listed in Table 5.

| No. of paralleled PSUs | Max available power on main output without redundancy | Max available power on main output with n+1 redundancy | Max available power on standby output |
|------------------------|-------------------------------------------------------|--------------------------------------------------------|---------------------------------------|
| 1                      | 3000 W                                                | -                                                      | 24 W                                  |
| 2                      | 5850 W                                                | 3000 W                                                 | 24 W                                  |
| 3                      | 8700 W                                                | 5850 W                                                 | 24 W                                  |
| 4                      | 11550 W                                               | 8700 W                                                 | 24 W                                  |
| 5                      | 14400 W                                               | 11550 W                                                | 24 W                                  |
| 6                      | 17250 W                                               | 14400 W                                                | 24 W                                  |

Table 5. Available power when multiple PSUs are operating

## 8.11 SENSE INPUTS

Main output sense lines have been implemented in order to compensate voltage drops on the load wires: a maximum voltage drop of 200 mV on the positive rail and 100 mV on the PGND rail is allowed. If sense inputs are not connected (open), main output voltage will rise by 250 mV; therefore, if sense inputs are not used, they should be connected to the power output and SGND, close to the power supply connector. The sense inputs are protected against short circuit and reverse polarity. If the sense lines are shorted (or reverse polarized) at start-up condition, then  $V_1$  will be regulated by 500 mV higher than the reference voltage for 100 ms and later the PSU will shut down reporting a sense fault error. If the sense lines are shorted (or reverse polarized) during operation, then the unit will shut down immediately.

## 8.12 I2C / POWER MANAGEMENT BUS COMMUNICATION

The PSU is a communication slave device only: it never initiates messages on the I2C / SMBus. It recognizes any time Start / Stop bus conditions and the interface driver in the supply is referred to the SGND. Communication bus voltage and timing are defined by:

- 100 k $\Omega$  internal pull-up resistors
- SDA / SCL IOs must be pull-up externally to  $3.3 \pm 0.3$  V
- Pull-up resistor should be 2 k $\Omega$  to 5 k $\Omega$  to ensure SMBUS compliant signal rise times
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of > 25 ms with recovery time within 10 ms

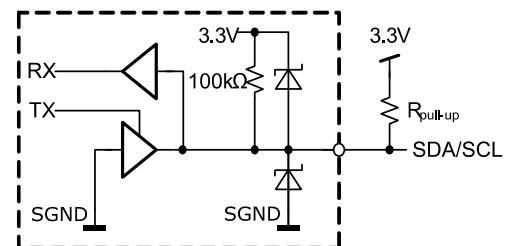


Figure 20. Physical layer of communication interface

SMB\_ALERT\_L signal indicates that the power supply is experiencing a problem that the system agent should investigate: this is a logical OR of the shutdown and warning events. Communication to the DSP will be possible as long as the input voltage is provided. If no input voltage is present, communication to the unit is possible as long as it is connected to a live  $V_{SB}$  output (e.g. provided by a redundant unit); if only  $V_1$  is provided, communication is not possible.

| PARAMETER          | CONDITION                                                |                                                            | MIN                                             | MAX                                   | UNIT |
|--------------------|----------------------------------------------------------|------------------------------------------------------------|-------------------------------------------------|---------------------------------------|------|
| V <sub>iL</sub>    | Input low voltage                                        |                                                            | -0.2                                            | 0.4                                   | V    |
| V <sub>iH</sub>    | Input high voltage                                       |                                                            | 2.1                                             | 3.6                                   | V    |
| V <sub>hys</sub>   | Input hysteresis                                         |                                                            | 0.15                                            |                                       | V    |
| V <sub>oL</sub>    | Output low voltage                                       | 4 mA sink current                                          | 0                                               | 0.4                                   | V    |
| t <sub>r</sub>     | Rise time for SDA and SCL                                |                                                            | 20 + R <sub>b</sub> C <sub>b</sub> <sup>1</sup> | 300                                   | ns   |
| t <sub>of</sub>    | Output fall time V <sub>iHmin</sub> → V <sub>iLmax</sub> | 10 pF < C <sub>b</sub> <sup>1</sup> < 400 pF               | 20 + R <sub>b</sub> C <sub>b</sub> <sup>1</sup> | 250                                   | ns   |
| I <sub>i</sub>     | Input current SCL / SDA                                  | 0.1 V <sub>DD</sub> < V <sub>i</sub> < 0.9 V <sub>DD</sub> | -10                                             | 10                                    | μA   |
| C <sub>i</sub>     | Capacitance for each SCL / SDA                           |                                                            |                                                 | 10                                    | pF   |
| f <sub>SCL</sub>   | SCL clock frequency                                      |                                                            | 0                                               | 100                                   | kHz  |
| R <sub>pu</sub>    | External pull-up resistor                                |                                                            |                                                 | 1000 ns / C <sub>b</sub> <sup>1</sup> | Ω    |
| t <sub>HDSTA</sub> | Hold time (repeated) START                               | f <sub>SCL</sub> ≤ 100 kHz                                 | 4.0                                             |                                       | μs   |
| t <sub>LOW</sub>   | Low period of the SCL clock                              | f <sub>SCL</sub> ≤ 100 kHz                                 | 4.7                                             |                                       | μs   |
| t <sub>HIGH</sub>  | High period of the SCL clock                             | f <sub>SCL</sub> ≤ 100 kHz                                 | 4.0                                             |                                       | μs   |
| t <sub>SUSTA</sub> | Setup time for a repeated START                          | f <sub>SCL</sub> ≤ 100 kHz                                 | 4.7                                             |                                       | μs   |
| t <sub>HDDAT</sub> | Data hold time                                           | f <sub>SCL</sub> ≤ 100 kHz                                 | 0                                               | 3.45                                  | μs   |
| t <sub>SUDAT</sub> | Data setup time                                          | f <sub>SCL</sub> ≤ 100 kHz                                 | 250                                             |                                       | μs   |
| t <sub>SUSTO</sub> | Setup time for STOP condition                            | f <sub>SCL</sub> ≤ 100 kHz                                 | 4.0                                             |                                       | μs   |
| t <sub>BUF</sub>   | Bus free time between STOP and START                     | f <sub>SCL</sub> ≤ 100 kHz                                 | 4.7                                             |                                       | μs   |
| EEPROM_WP          |                                                          |                                                            |                                                 |                                       |      |
| V <sub>iL</sub>    | Input low voltage                                        |                                                            | -0.2                                            | 0.4                                   | V    |
| V <sub>iH</sub>    | Input high voltage                                       |                                                            | 2.1                                             | 3.6                                   | V    |
| I <sub>i</sub>     | Input sink or source current                             |                                                            | -1                                              | 1                                     | mA   |
| R <sub>pu</sub>    | Internal pull-up resistor to 3.3V                        |                                                            |                                                 | 10k                                   | Ω    |

<sup>1</sup>  $C_b$  = Bus line capacitance in pF, typically in the range of 10 pF...400 pF,  $R_b$  = 100  $\Omega$

Table 6. I2C / SMBus Specification

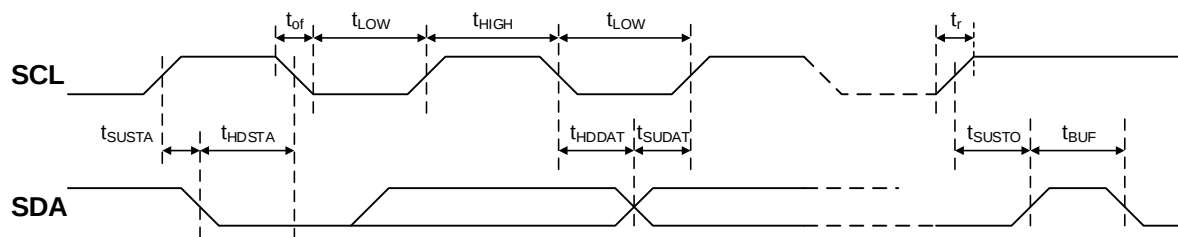


Figure 21. I2C / SMBus Timing

### 8.13 ADDRESS

The unit supports the Power Management Bus communication protocol with a fixed address at 0x20. The EEPROM is at fixed address = 0xA0.

### 8.14 CONTROLLER ACCESS

The controller and the EEPROM in the power supply share the same I2C bus physical layer (see Figure 23). In order to write to the EEPROM, the write protection needs to be disabled by setting EEPROM\_WP input correctly. EEPROM\_WP=HIGH: write disabled; EEPROM\_WP=LOW: write enabled.

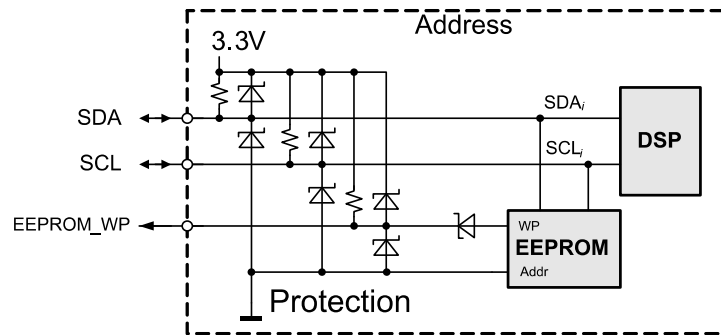


Figure 22. I2C Bus to Controller and EEPROM

### 8.15 EEPROM PROTOCOL

The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

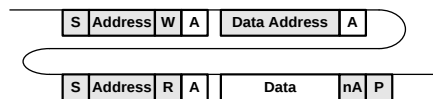
#### WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.



#### READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



## 8.16 POWER MANAGEMENT BUS PROTOCOL

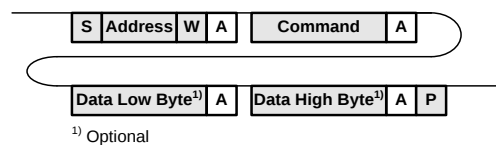
The Power Management Bus is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at: [www.powerSIG.org](http://www.powerSIG.org).

Power Management Bus command codes are not register addresses. They describe a specific command to be executed. PFF3000-12-069RD supply supports the following basic command structures:

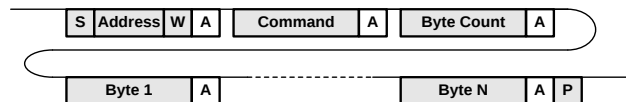
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

### WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).

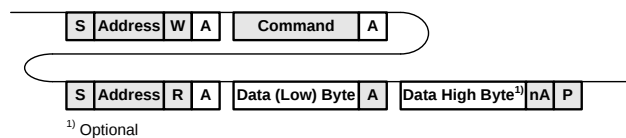


In addition, Block write commands are supported with a total maximum length of 255 bytes. See PFF3000-12-069RA Power Management Bus Communication Manual BCA.00070 for further information.

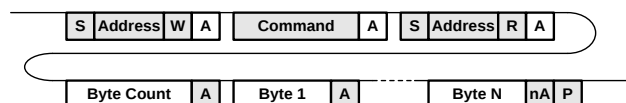


### READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



In addition, Block read commands are supported with a total maximum length of 255 bytes. See PFF3000-12-069RD Power Management Bus Communication Manual BCA.00216 for further information.



## 8.17 GRAPHICAL USER INTERFACE

Bel Power Solutions provides its I2C Utility: a Windows® XP / Vista / Win7 compatible graphical user interface (GUI), allowing PFF3000-12-069RD programming and monitoring. This utility can be downloaded at [belfuse.com/power-solutions](http://belfuse.com/power-solutions) and supports both the PSI and Power Management Bus protocols. The GUI allows automatic finding of connected units to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.

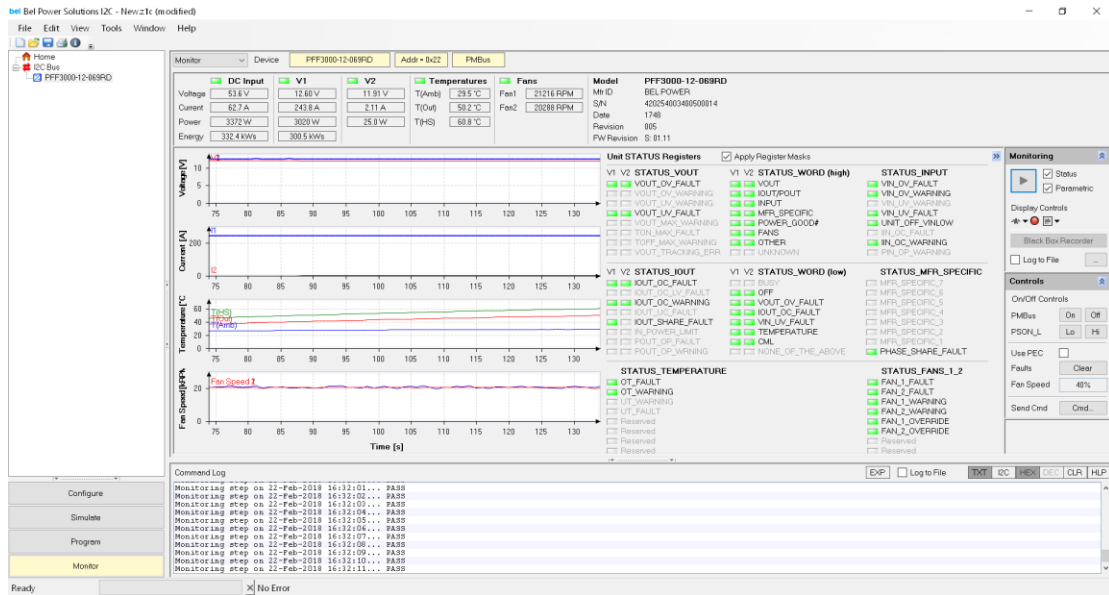


Figure 23. Monitoring dialog of the I2C utility (example)

## 9. TEMPERATURE AND FAN CONTROL

In order to achieve best cooling results, sufficient airflow through the supply must be ensured; airflow shall not be blocked or obstructed by placing large objects close to the output connector at the rear of the supply. PFF3000-12-069RD is provided with a front-to-rear airflow, thus meaning the air enters through the power supply handle side (front) and leaves at the rear side. PFF3000-12-069RD has been designed for horizontal operation. The internal fan is controlled by a microprocessor: fan rpm is then adjusted to provide optimal cooling air and is a function of output power, inlet and internal MOSFETs temperature.

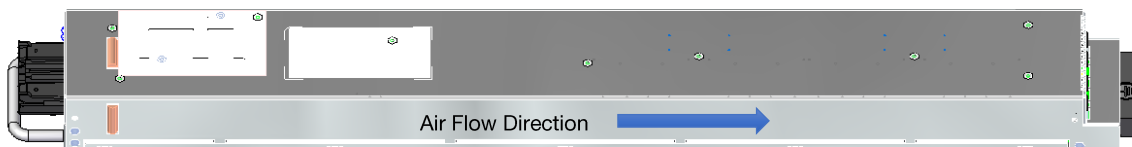


Figure 24. Airflow direction

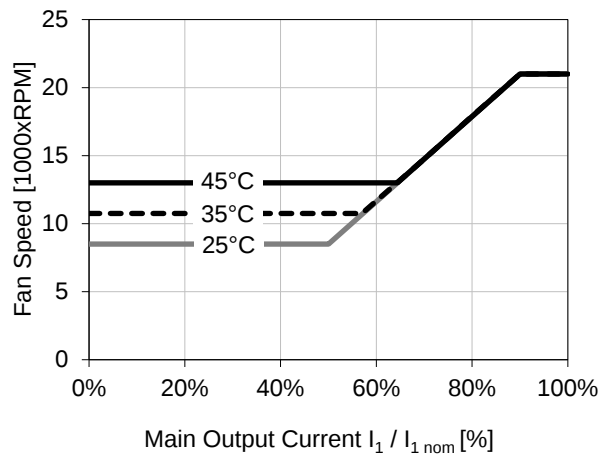


Figure 25. Fan speed vs. main output load

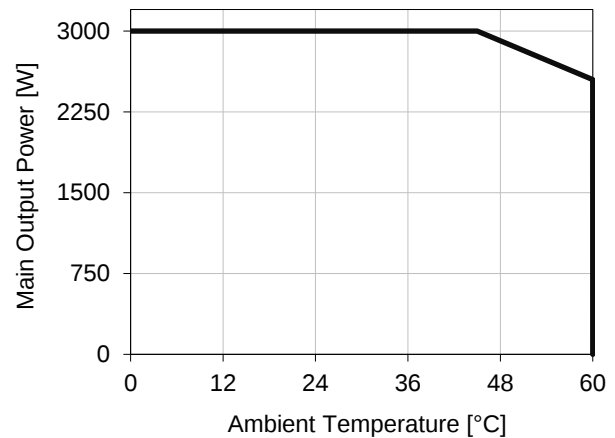


Figure 26. Thermal power derating

## 10. ELECTROMAGNETIC COMPATIBILITY

### 10.1 IMMUNITY

**NOTE:** Most of the immunity requirements are derived from EN 55024:1998/A2:2003.

| PARAMETER                      | DESCRIPTION / CONDITION                                                                                    | CRITERION |
|--------------------------------|------------------------------------------------------------------------------------------------------------|-----------|
| ESD Contact Discharge          | IEC / EN 61000-4-2, $\pm 8$ kV, 25 + 25 discharges per test point (metallic case, LEDs, connector body)    | A         |
| ESD Air Discharge              | IEC / EN 61000-4-2, $\pm 15$ kV, 25 + 25 discharges per test point (non-metallic user accessible surfaces) | A         |
| Radiated Electromagnetic Field | IEC / EN 61000-4-3, 10 V/m, 1 kHz / 80% Amplitude Modulation, 1 $\mu$ s Pulse Modulation, 10 kHz...2GHz    | A         |
| Burst                          | IEC / EN 61000-4-4, level 3, DC port $\pm 1$ kV, 1 minute                                                  | A         |
| Surge                          | IEC / EN 61000-4-5<br>Line to earth: level 2, $\pm 1$ kV<br>Line to line: level 3, $\pm 1$ kV              | A         |
| RF Conducted Immunity          | IEC / EN 61000-4-6, level 3, 10 V <sub>rms</sub> , CW, 0.1... 80 MHz                                       | A         |

### 10.2 EMISSION

| PARAMETER          | DESCRIPTION / CONDITION                                                  | CRITERION        |
|--------------------|--------------------------------------------------------------------------|------------------|
| Conducted Emission | EN55022 / CISPR 22: 0.15... 30 MHz, QP and AVG                           | Class A          |
| Radiated Emission  | EN55022 / CISPR 22: 30 MHz... 1 GHz, QP                                  | Class A          |
| Acoustical Noise   | Sound power statistical declaration (ISO 9296, ISO 7779, IS9295)<br>load | @ 50 %<br>60 dBA |

## 11. SAFETY / APPROVALS

Maximum electric strength testing is performed in factory according to IEC / EN 60950 and UL 60950. Input - to - output electric strength tests should not be repeated in the field. Bel Power Solutions will not honour any warranty claims resulting from electric strength field tests.

| PARAMETER                | DESCRIPTION / CONDITION                                                                                                                                               | CRITERION                                            |
|--------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------|
| Agency Approvals         | Approved to the latest edition of the following standards:<br>• IEC60950-1 2nd edition (CB)<br>• EN60950-1 2nd Edition (Nemko)<br>• UL/CSA0950-1 2nd Edition (cCSAus) | Approved by independent body<br>(see CE declaration) |
| Isolation Strength       | Input (DCIN+ / DCIN-) to case (PE)<br>Input (DCIN+ / DCIN-) to output<br>Output to case (PE)                                                                          | Basic<br>Basic<br>Functional                         |
| Creepage / Clearance     | Primary (DCIN+ / DCIN-) to protective earth (PE)<br>Primary to secondary                                                                                              | According to safety standard                         |
| Electrical Strength Test | Input to case<br>Input to output<br>Output and signals to case                                                                                                        | According to safety standard                         |

## 12. ENVIRONMENTAL

| PARAMETER         | DESCRIPTION / CONDITION    | MIN                                                                                                 | NOM           | MAX   | UNIT                |
|-------------------|----------------------------|-----------------------------------------------------------------------------------------------------|---------------|-------|---------------------|
| T <sub>A</sub>    | Ambient temperature        | V <sub>I min</sub> to V <sub>I max</sub> , I <sub>I nom</sub> , I <sub>SB nom</sub> at 4000 m       |               | +40 * | °C                  |
|                   |                            | V <sub>I min</sub> to V <sub>I max</sub> , I <sub>I nom</sub> , I <sub>SB nom</sub> at 1800 m       |               | +45   | °C                  |
| T <sub>Aext</sub> | Extended temperature range | Derated output                                                                                      |               | +45   | +55 °C              |
| T <sub>S</sub>    | Storage temperature        | Non - operational                                                                                   |               | -40   | +70 °C              |
|                   | Altitude                   | Operational, above sea level                                                                        |               | -     | 4000 m              |
|                   | Relative humidity          | Operational: T <sub>A</sub> = 40 °C                                                                 |               | 7     | 85 %                |
|                   |                            | Non-Operational                                                                                     |               | 5     | 93 %                |
| N <sub>a</sub>    | Audible noise              | V <sub>I nom</sub> , 50 % I <sub>O nom</sub> ,<br>T <sub>A</sub> = 25 °C at by-stander position     |               | 60    | dBA                 |
|                   | Cooling                    | System back pressure                                                                                |               | 0.5   | in H <sub>2</sub> O |
| Shock             | IEC60068-2-27              | Operational: 11ms, half-sine<br>Non-Operational: 11ms, half-sine                                    | 7<br>30       |       | g pk                |
| Vibration         | IEC60068-2-27              | Operational: Swept-sine, 5-500-5 Hz<br>Non-Operational: Swept-sine, 5-500-5 Hz<br>Random, 10-500 Hz | 1<br>4<br>3.5 |       | gpk                 |
| Fall test         | IEC60068-2-32              | Edge drop, Corner drop, topple                                                                      |               | 1     | m                   |

**NOTE:** \* System airflow will assist the PSU airflow

## 13. MECHANICAL

| PARAMETER  | DESCRIPTION / CONDITION | MIN | NOM  | MAX | UNIT |
|------------|-------------------------|-----|------|-----|------|
| Dimensions | Width                   |     | 69   |     | mm   |
|            | Height                  |     | 42   |     | mm   |
|            | Depth                   |     | 555  |     | mm   |
| m          | Weight                  |     | 2.66 |     | kg   |

[illegible]

Technical drawing of a long, thin mechanical component. The drawing shows a side view of the component with various features and dimensions. The overall length is dimensioned as 613.71. The width of the component is dimensioned as 20.2. The thickness of the component is dimensioned as  $\pm 0.5$ . The drawing also shows a detail of the end of the component, which includes a circular feature and a rectangular feature. The drawing is labeled with the number 1 in the top right corner.

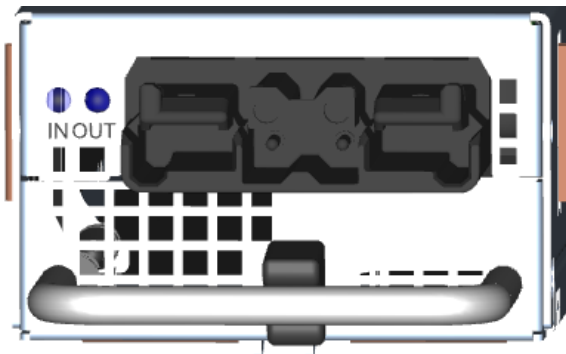


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## 14. CONNECTORS

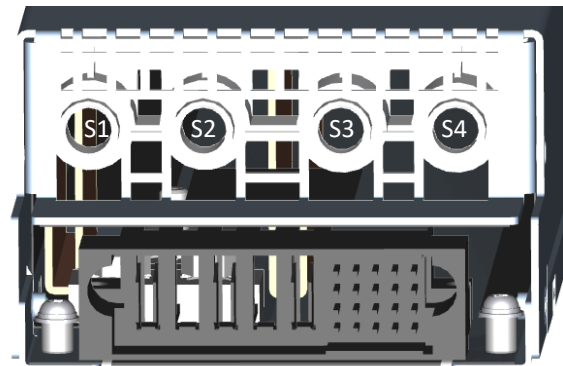
### Input



|     |      |      |     |
|-----|------|------|-----|
| IN1 | Aux1 | Aux2 | IN2 |
|     | Aux3 | Aux4 |     |

Connector: Anderson Power SBS75XPRBLK-BK  
 Counterpart:  
 Housing: Anderson Power SBS75XBLK  
 Power pins IN1/2 (AWG6): Anderson Power 1339G2  
 Sockets Aux1/2 (AWG24-20): Anderson Power PM16S2024S32

### Output



| S1 |    | S2 |    | S3 |    | S4 |    |    |    |
|----|----|----|----|----|----|----|----|----|----|
| P1 | P2 | P3 | P4 | P5 | D1 | D2 | D3 | D4 | D5 |
|    |    |    |    |    | C1 | C2 | C3 | C4 | C5 |
|    |    |    |    |    | B1 | B2 | B3 | B4 | B5 |
|    |    |    |    |    | A1 | A2 | A3 | A4 | A5 |

Connector: Amphenol/FCI 51939-768LF  
 Counterpart: Amphenol/FCI 51915-401LF  
 A1 and A2 are trailing pins (short pins)  
 For main output pins (S1-S4), see section 14

### 14.1 INPUT CONNECTOR PINOUT

| PIN                  | NAME        | DESCRIPTION                       |
|----------------------|-------------|-----------------------------------|
| <i>Input Power</i>   |             |                                   |
| IN1                  | DCIN-       | Input voltage negative            |
| IN2                  | DCIN+       | Input voltage positive            |
| <i>Input Signals</i> |             |                                   |
| Aux1                 | reserved    |                                   |
| Aux2                 | reserved    |                                   |
| Aux3                 | PSKILL_IN_L | Input connector power supply kill |
| Aux4                 | SGND        | Signal ground                     |

Table 7. Input Connector Pinout

## 14.2 OUTPUT CONNECTOR PINOUT

| Output         |                                                                                   |                                      |            |
|----------------|-----------------------------------------------------------------------------------|--------------------------------------|------------|
| S1, S2         | PGND                                                                              | +12 VDC main output ground           |            |
| S3, S4         | V1                                                                                | +12 VDC main output                  |            |
| PE             |                                                                                   |                                      |            |
| P1             |  | Protective Earth                     |            |
| P2             | empty                                                                             | -                                    |            |
| P3             |  | Protective Earth                     |            |
| P4             | empty                                                                             | -                                    |            |
| P5             |  | Protective Earth                     |            |
| Output Signals |                                                                                   |                                      |            |
| A1             | PSKILL_L                                                                          | Power supply kill (trailing pin):    | active low |
| B1             | PWOK_L                                                                            | Power OK signal output:              | active low |
| C1             | INOK_L                                                                            | Input OK signal:                     | active low |
| D1             | PSON_L                                                                            | Power supply on input:               | active low |
| A2             | PRESENT_L                                                                         | Power supply present (trailing pin): | active low |
| B2             | SGND                                                                              | Signal ground * (return)             |            |
| C2             | SGND                                                                              | Signal ground * (return)             |            |
| D2             | SGND                                                                              | Signal ground * (return)             |            |
| A3             | SCL                                                                               | I2C clock signal line                |            |
| B3             | SDA                                                                               | I2C data signal line                 |            |
| C3             | SMB_ALERT_L                                                                       | SMB alert signal output:             | active low |
| D3             | ISHR_BUS                                                                          | V1 current share bus                 |            |
| A4             | EEPROM_WP                                                                         | EEPROM Write protect                 |            |
| B4             | RSVD                                                                              | Reserved                             |            |
| C4             | V1_SNS_R                                                                          | Main output negative sense           |            |
| D4             | V1_SNS                                                                            | Main output positive sense           |            |
| A5             | VSB                                                                               | Standby positive output              |            |
| B5             | VSB                                                                               | Standby positive output              |            |
| C5             | VSB_R                                                                             | Standby ground *                     |            |
| D5             | VSB_R                                                                             | Standby ground *                     |            |

**NOTE:** \* These pins should be connected to SGND on the system.  
See section 7 for pull-up resistor settings of signal pins - All signal pins are referred to SGND.

Table 8. Output Connector Pinout



## 16. ACCESSORIES

| ITEM                                                                              | DESCRIPTION                                                                                                                          | ORDERING PN | SOURCE                                                                       |
|-----------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|-------------|------------------------------------------------------------------------------|
|  | <b>I²C Utility</b><br>Windows Vista/7/8 compatible<br>GUI to program, control and<br>monitor PFE Front-Ends (and<br>other I²C units) | N/A         | <a href="http://belfuse.com/power-solutions">belfuse.com/power-solutions</a> |

## 17. REFERENCES

| DOCUMENT NUMBER | DESCRIPTION                                                |
|-----------------|------------------------------------------------------------|
| BCA.00447       | PFF3000-12-069RD Installation Instruction                  |
| BCA.00216       | PFF3000-12-069RD Power Management Bus Communication Manual |
| BCD.00887       | Power Shelf SPSPPF3-01G datasheet                          |
| BCD.00820       | NAC2006-01 datasheet                                       |

## 18. REVISION HISTORY

| REV | DESCRIPTION                                                                                                                                                  | PSU PRODUCT<br>VERSION | DATE      | AUTHOR |
|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|-----------|--------|
| 008 | First release version                                                                                                                                        |                        | Jan-2018  | RK/MS  |
| 011 | Product photo updated; Output and Protection table update; Added EEPROM and Power Management Bus Protocol chapters; General unification with PFE3000 product |                        | Mar-2018  | RK/MS  |
| AA  | Update readback and protection table, release to AA                                                                                                          |                        | June-2018 |        |
| AB  | Update input voltage from positive to negative values, Correct (swap) Pi and Po readback tolerances                                                          |                        | Aug-2018  | RK     |
| AC  | Remove preliminary watermark                                                                                                                                 |                        |           |        |

**For more information on these products consult: [tech.support@psbel.com](mailto:tech.support@psbel.com)**

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