

# TEC3200-54-074xA

## AC-DC CRPS Front-End Power Supply

TEC3200-54-074xA is a 3200 W Common Redundant Power Supply (CRPS) power supply that converts standard AC mains power or High Voltage DC bus voltages (HVDC) into a main output of 54 VDC for powering systems using distributed power architectures.

The power supply is hot-swappable and supports N+1 redundant architecture. The high-power density helps to improve the overall system efficiency and enhance system reliability. The full digital control facilitates remote set-up, monitoring and control.

TEC3200-54-074xA offers multiple protections including overvoltage, overtemperature, overcurrent, overpower & short circuit protection.

This power supply meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).



### Features & Benefits

- Input Voltage Range 90 – 264 VAC / 180 – 300 VDC
- Nominal Output Voltage 54 VDC
- Standby Output 12 V<sub>SB</sub> (3 A)
- Output Power up to 3200 W
- Dimensions: 185 x 73.5 x 40 mm (7.28 x 2.89 x 1.57 in)
- High Power Density
- UL/CSA 62368-1, EN/IEC 62368-1 Safety Approved
- Supports N+1 Redundancy, SMART\_ON Redundancy, Internal ORing
- Black Box Recorder, Bootloader
- Clockwise and Counter-Clockwise Fan Rotation
- Supports Power Management Bus Communication Protocol

### Applications

- Networking Switches
- Servers & Routers
- Telecommunications

## 1 ORDERING INFORMATION

TEC	3200	-	54	-	074	x	A
Product Family	Power Level	Dash	V1 Output	Dash	Width	Airflow	Input
TEC Front-Ends	3200 W		54 V		73.5 mm	N: Normal R: Reverse	A: AC

## 2 INPUT

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Input Voltage Ranges*	Low Voltage AC Range (1300 W); AC Current 16 A (Low line)	90	100~127	132	V <sub>RMS</sub>
	Low Voltage Start-up		84 ± 4		VAC
	Low Voltage Power Off		75 ± 5		VAC
	High Voltage AC Range (3000 W); AC Current 16 A (High line 1)	180	200~219	220	V <sub>RMS</sub>
	High Voltage Start-up		175 ± 4		VAC
	High Voltage Power Off		164 ± 5		VAC
	High Voltage AC Range (3200 W); AC Current 16 A (High line 2)	220	220~240	264	V <sub>RMS</sub>
	HVDC (3000 W); DC current 16 A	180	200	219	VDC
	Start-up		171 ± 4		VDC
	Power Off		160 ± 5		VDC
	HVDC (3200 W); DC Current 16 A	220	240	320	VDC
AC Inrush Current	@ 240 VAC / 240 VDC, 3200 W, 1 – 1200 ms cold start			35	APK
Input Frequency		47	50/60	63	Hz
Power Factor	230 VAC / 50 & 60 Hz	0.90			
	230 VAC / 50 & 60 Hz	0.96			
	230 VAC / 50 & 60 Hz	0.98			
	230 VAC / 50 & 60 Hz	0.99			
iTHD (Total Harmonic Distortion)	230 VAC / 50 & 60 Hz, 10% load			15	
	230 VAC / 50 & 60 Hz, 20 % load			10	%
	230 VAC / 50 & 60 Hz, 50% load			5	
	230 VAC / 50 & 60 Hz, 100% load			5	
Efficiency	230 VAC / 60 Hz, 10% load	90			%
	230 VAC / 60 Hz, 20% load	94			%
	230 VAC / 60 Hz, 50% load	96			%
	230 VAC / 60 Hz, 100% load	94			%
Hold-up Time	@ 3200W	8			ms
	@ 2600W	10			ms
12V <sub>SB</sub> Hold-up Time	@ 100% load	70			ms
AC Line Sag	0 to 1/2 AC cycle (nom AC voltage ranges, 50/60 Hz)		95		%
	No loss of function or performance. (0%-70%load)				
	> 1 AC cycle (nom AC voltage ranges, 50/60 Hz)	30			%
AC Line Surge	Loss of function acceptable, self-recoverable				
	Continuous (nom AC voltage ranges, 50/60 Hz)		10		%
	No loss of function or performance				
	0 to 1/2 AC cycle (mid-point of nom VAC ranges, 50/60 Hz)		30		%
AC Line Isolation	No loss of function or performance				
	Primary to secondary; reinforced insulation (IEC 60950)	3000 4242			VAC VDC

### Notes:

1. The Brown IN/OUT Hysteresis min is 5 VAC
2. Maximum input current at low input voltage range is measured at 100 VAC, at max load
3. Maximum input current at high input voltage range is measured at 200 VAC, at max load
4. Dc input current maximum while input voltage is 200 VDC.at max load
5. AC Brown-in/out loading is 80% load; (low line & high line)



### 3 OUTPUT

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Output Voltage	Output voltage adjusted to 54 VDC $\pm$ 0.1 VDC @ 50% load at 230 VAC input		+54		VDC
Voltage Regulation Limits	$\pm$ 5 %	+51.3	+54	+56.7	VDC
Output Power	Continuous			3200	W
Output Current	@ 1300 W @ 3000 W @ 3200 W			24 55.5 59.2	A
Overshoot			7		%
Transient Load *	$\Delta$ Step Load Size, 60% of Load Max, Load Slew Rate 2.5 A/ $\mu$ s			100	$\mu$ F
Capacitive Loading		100		13000	$\mu$ F
Output Ripple & Noise	10 Hz – 20 MHz BW (10 $\mu$ F tantalum capacitor in parallel with a 0.1 $\mu$ F ceramic capacitor placed at the point of measurement)			540	mVpp
<b>+12 V<sub>SB</sub> OUTPUT</b>					
+12 V <sub>SB</sub> Output Voltage			+12.2		V <sub>SB</sub>
Voltage Regulation	$\pm$ 5 %	+11.59	+12.2	+12.81	V
+12 V <sub>SB</sub> Output Current				3	A
Overshoot			7		%
Transient Load *	$\Delta$ Step Load Size = 1 A; Load Slew Rate 2.5 A/ $\mu$ s			100	$\mu$ F
Capacitive Loading		100		3100	$\mu$ F
Output Ripple & Noise	10 Hz to 20 MHz BW (10 $\mu$ F tantalum capacitor in parallel with a 0.1 $\mu$ F ceramic capacitor placed at the point of measurement)			120	mVpp

\* The min. load for the test condition on +54 V rail is 1 A, the min. load for the test condition on +12V rail is 0.1A.

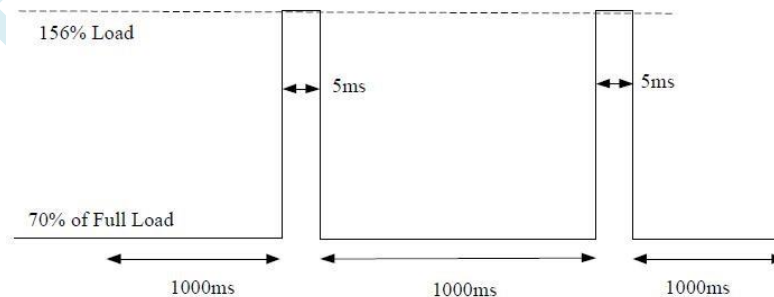
#### 3.1 PEAK LOAD

EDPP-pattern1~4 support different input phases.

##### 3.1.1 EDPP PATTERN 1

Pmax Peak support is based on Pmax Protection specified that included and added system 54 V capacitors. The peak loading current measured between PSU and system buffer capacitance. The current slope is 2.5 A/ $\mu$ s during the Peak power period, and the applied Peak loading starts from the PSU 70% of rated current.

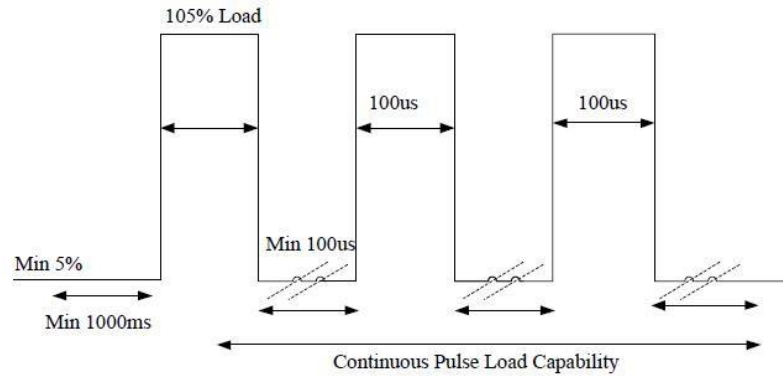
PSU TYPE	PMAX PEAK LOAD <sup>1</sup>	PEAK CURRENT	SYSTEM CAPACITANCE	PEAK LOAD DURATION	VOLTAGE UNDERSHOOT
CRPS	70% to 156%	41.1 A to 92.5 A	1000 $\mu$ F	5 ms	-7%



### 3.1.2 EDPP PATTERN 2

Slew Rate: 5 A/us, Repeat Pattern with OFF Time: 0.1ms/0.5ms/1.0ms/2.5ms/7.5ms/10ms.

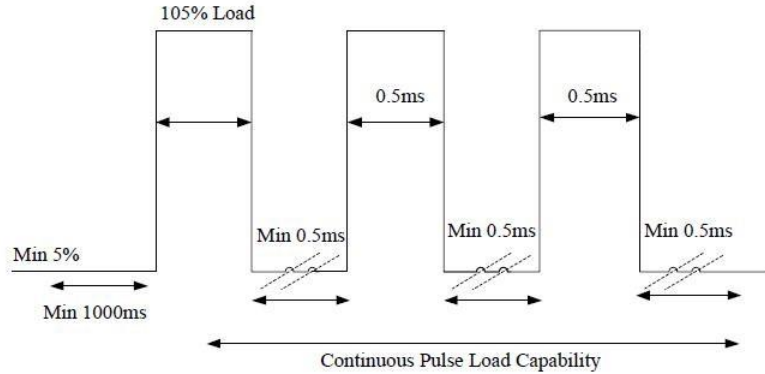
PSU TYPE	P <sub>MAX</sub> PEAK LOAD <sup>1</sup>	PEAK CURRENT	SYSTEM CAPACITANCE	PEAK LOAD DURATION	VOLTAGE UNDERSHOOT
CRPS	5% to 105%	2.96 A to 62.16 A	1000 uF	100 us	-7%



### 3.1.3 EDPP PATTERN 3

Slew Rate: 5A/us, Repeat Pattern with OFF Time: 0.5ms/1.0ms/2.5ms/7.5ms/10ms.

PSU TYPE	P <sub>MAX</sub> PEAK LOAD <sup>1</sup>	PEAK CURRENT	SYSTEM CAPACITANCE	PEAK LOAD DURATION	VOLTAGE UNDERSHOOT
CRPS	5% to 105%	2.96 A to 62.16 A	1000 uF	500 us	-7%

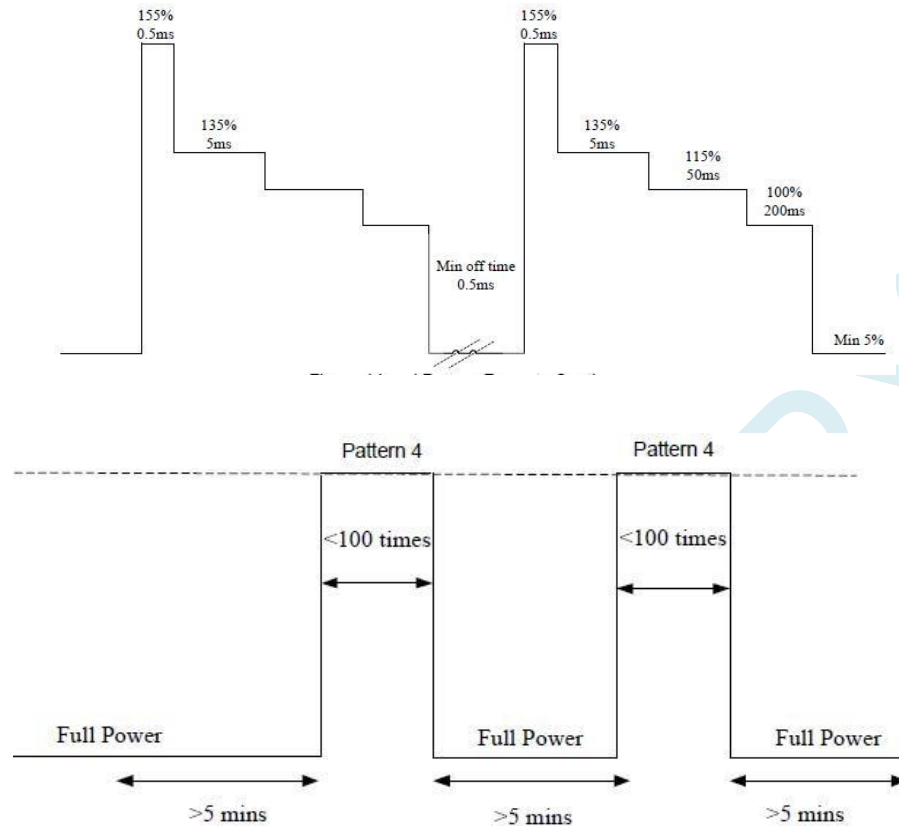


### 3.1.4 EDPP PATTERN 4

Slew Rate: 1A/us, Repeat Pattern with OFF Time: 0.5ms/1.0ms/2.5ms/7.5ms/10ms.

Load Pattern Repeats Continuous, Continuous time need to less than 100 times (this is considered the average power will over 2.6kW at Pattern 4 condition), and need to power down to full power 5 minutes at least, then repeat the Pattern 4.

PSU TYPE	P <sub>MAX</sub> PEAK LOAD <sup>1</sup>	PEAK CURRENT	SYSTEM CAPACITANCE	PEAK LOAD DURATION	VOLTAGE UNDERSHOOT
CRPS	5% to 155%	2.9 A to 91.7 A	1000 uF	0.5 ms	-7%
	155% to 135%	91.7 A to 79.9 A		5 ms	
	135% to 115%	79.9 A to 68.8 A		50 ms	
	115% to 100%	68.8 A to 59.2 A		200 ms	



### 3.2 POWER & CURRENT RATINGS

Output	Input voltage (VAC)	Input voltage (VDC)	Output Power (W)	Max. Current Rating (A)	20 s Peak Current (A)	5 ms Peak Current (A)
54 V main	90 – 132	-	1300	24	Rated + 2	156% Rated
54 V main	180 – 219	180 – 219	3000	55.5	Rated + 4	156% Rated
54 V main	220 – 264	220 – 320	3200	59.2	Rated + 4	156% Rated
12 V <sub>SB</sub>			0	3.0	3.3	-

\* Length of time the 20 sec peak power can be supported is based on thermal sensor and assertion of the SMBAlert# signal. Minimum peak power duration shall be 20 sec without asserting the SMBAlert# signal at maximum operating temperature.

### 3.3 FORCED LOAD SHARING

The +54V output has active load sharing. The output shares within 10% at full load. The failure of a power supply should not affect the load sharing or output voltages of the other supplies still operating. The supplies must be able to load share in parallel and operate in a hot-swap / redundant 1+1 configurations.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
VSHARE; I <sub>OUT</sub> =Max	Voltage of load share bus at specified maximum output current	7.6	8.0	8.4	V
VSHARE; I <sub>OUT</sub> =75%Max	Voltage of load share bus at specified 75% maximum output current	5.7	6.0	6.3	V
VSHARE; I <sub>OUT</sub> =50%Max	Voltage of load share bus at specified 50% maximum output current	3.6	4.0	4.4	V
VSHARE; I <sub>OUT</sub> =25%Max	Voltage of load share bus at specified 25% maximum output current	1.8	2.0	2.2	V
ΔVSHARE / ΔI <sub>OUT</sub> ; I <sub>OUT</sub> > 1A	Slope of load share bus voltage with changing load		8.0 / I <sub>MAX</sub>		V/A



### 3.4 TIMING REQUIREMENTS

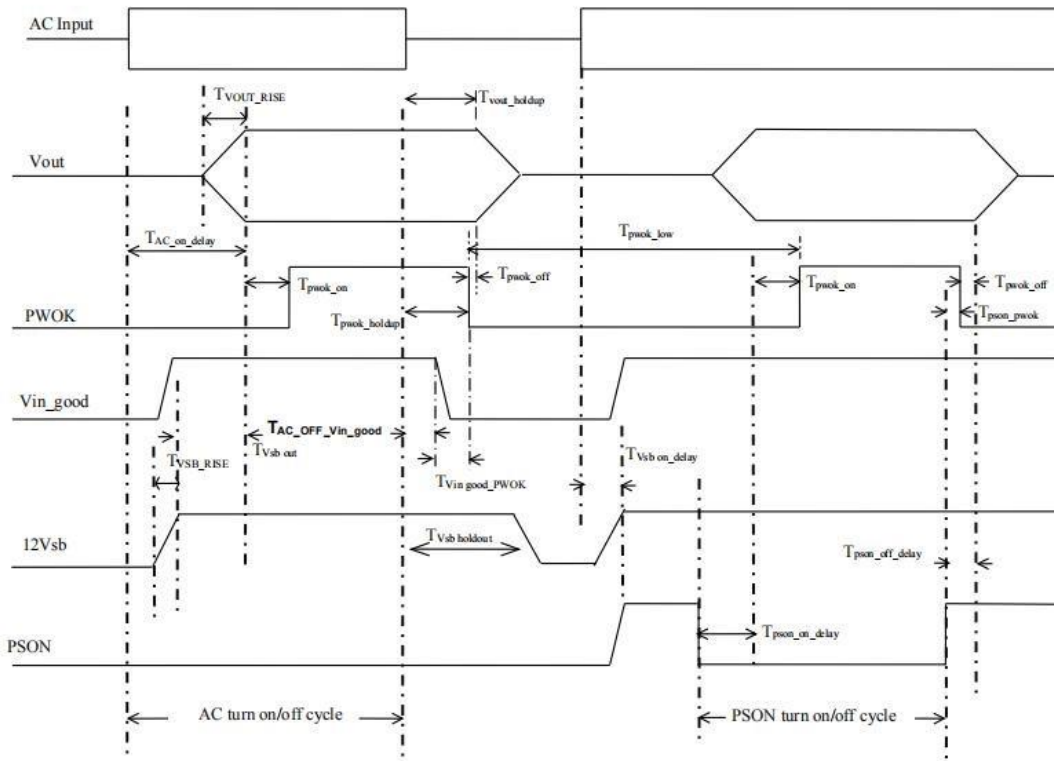


Figure 1. Signal Timing Sequence

#### Timing Values for Signal Timing Sequence:

ITEM	DESCRIPTION	MIN	MAX	UNITS
T <sub>AC_OFF_Vin_good</sub>	The time interval between AC Drop to zero to Vin_good signal gets asserted		4	ms
T <sub>Vin_good_PWOK</sub>	Vin_good shall be get asserted 1ms prior to PWOK during ac loss event.	1	--	ms
T <sub>VSB_RISE</sub>	Standby voltage rise time for VSB	5	50	ms
T <sub>VSB_ON_DELAY</sub>	Delay from AC being applied to 12VSB being within regulation.		2000	ms
T <sub>VOUT_RISE</sub>	Output voltage rises time for 54V <sub>OUT</sub>	5	150	ms
T <sub>AC_ON_DELAY</sub>	Delay from AC being applied to 54V <sub>OUT</sub> output voltage being within regulation.		3000	ms
T <sub>VOUT_HOLDUP</sub>	Time 54V <sub>OUT</sub> output voltage stays within regulation after loss of AC with specified load on section 2.	9	--	ms
T <sub>PWOK_HOLDUP</sub>	Delay from loss of AC to de-assertion of PWOK with specified load on section 2.	8	--	ms
T <sub>PSON_OFF_DELAY</sub>	Delay from PSON# de-asserted to power supply turning off.		5	ms
T <sub>PSON_ON_DELAY</sub>	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
T <sub>PSON_PWOK</sub>	Delay from PSON# deactivate to PWOK being de- asserted.		5	ms
T <sub>PWOK_ON</sub>	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	ms
T <sub>PWOK_OFF</sub>	Delay from PWOK de-asserted to output voltages dropping out of regulation limits.	1	--	ms
T <sub>PWOK_LOW</sub>	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON# signal.	100	--	ms
T <sub>VSB_VOUT</sub>	Delay from V <sub>SB</sub> being in regulation to V <sub>OUT</sub> output voltage being in regulation at AC turn on.	50	1000	ms
T <sub>VSB_HOLDUP</sub>	Time the V <sub>SB</sub> standby voltage stays within regulation after loss of AC.	70	--	ms

## 4 PROTECTION

Protection circuits inside the power supply cause only the power supply's main outputs to shutdown. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15 sec and a PSON# cycle HIGH for 1 sec are able to reset the power supply.

### 4.1 OVER CURRENT PROTECTION (OCP)

The power supply has a current limit to prevent the outputs from exceeding the values shown in the table below. If the current limits have been exceeded, the power supply shuts down and latch off. The power supply will not be damaged from repeated power cycling in this condition. 12Vsb will be auto-recovered after removing OCP limit.

INPUT VOLTAGE	SPEC	DESCRIPTION	MIN	MAX	MIN	MAX
220 – 264 VAC Or 220 – 320 VDC (High Line 2)	Fast OCP	Fast over current protection (shutdown, latch)	70A	72A	100msec	150msec
	Slow OCP	Slow over current protection (shutdown and latch after MIN/MAX timing)	65A	79A	20sec	21sec
	Fast OCW	Fast over current warning (SMBAlert#)	67A	69A	60msec	100msec
	Slow OCW	Slow over current warning (SMBAlert#)	62A	64A	18sec	19sec
180 – 219 VAC Or 180 – 219 VDC (High Line 1)	Fast OCP	Fast over current protection (shutdown, latch)	64A	66A	100msec	150msec
	Slow OCP	Slow over current protection (shutdown and latch after MIN/MAX timing)	61A	63A	20sec	21sec
	Fast OCW	Fast over current warning (SMBAlert#)	58A	60A	60msec	100msec
	Slow OCW	Slow over current warning (SMBAlert#)	58A	62A	18sec	19sec
90 – 132 VAC (Low Line)	Fast OCP	Fast over current protection (shutdown, latch)	32A	33A	100msec	150msec
	Slow OCP	Slow over current protection (shutdown and latch after MIN/MAX timing)	28A	31A	20sec	21sec
	Fast OCW	Fast over current warning (SMBAlert#)	30A	31A	60msec	100msec
	Slow OCW	Slow over current warning (SMBAlert#)	26A	27A	18sec	19sec
High/Low line	12Vsb OCP	12Vsb over current protection (shutdown, hiccup mode)	3.5A	5.0A	1msec	100msec

### 4.2 OVER VOLTAGE PROTECTION (OVP)

The power supply over voltage protection is locally sensed. The power supply shuts down and then retry third time before latch off after an over voltage condition occurs. This latch will be cleared by toggling the PSON# signal or by an AC power interruption. The values are measured at the output of the power supply's connectors. The voltage will never exceed the maximum levels when measured at the power connectors of the power supply connector during any single point of fail. The voltage will never trip any lower than the minimum levels when measured at the power connector. 12VSB will be auto-recovered after removing OVP limit.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Over Voltage Protection (OVP)	+54 V Output - Latch off	58.5	59.5	62	V
	+12 V <sub>SB</sub> Output - Hiccup mode	13.3	14.5	15.6	V

### 4.3 OVER TEMPERATURE PROTECTION (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shut down. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the 12VSB remains always on. The OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip level shall have a minimum of 3 °C of ambient temperature hysteresis.

SENSOR	OTP °C	OTW °C	OTR °C
AMB.	67	63	57
SR	100	97	82
PFC	125	120	105



#### 4.4 SHORT CIRCUIT PROTECTION (SCP)

A short circuit is considered to be resistance of 100 mΩ or less, applied to any output during start-up or while running will not cause any damage to the power supply (connectors, components, PCB traces, etc.). The power supply shuts down and latches off for short on main outputs but recovers upon PS\_ON toggled or AC re-applied. When the Standby output VSB is shorted the output may go into “hiccup mode”, and all outputs shuts down upon a short circuit of the VSB. When the short is removed on VSB, the power supply shall recover automatically.

#### 4.5 CLOSED LOOP SYSTEM THROTTLING (CLST)

The power supply will always assert the SMBAlert# signal whenever temperature-monitored component in the power supply reaches a warning threshold. Upon reduction of the load within 2ms after the SMBAlert# signal is asserted if the load is reduced to less than the power supply rating; the power supply will continue to operate and not shutdown.

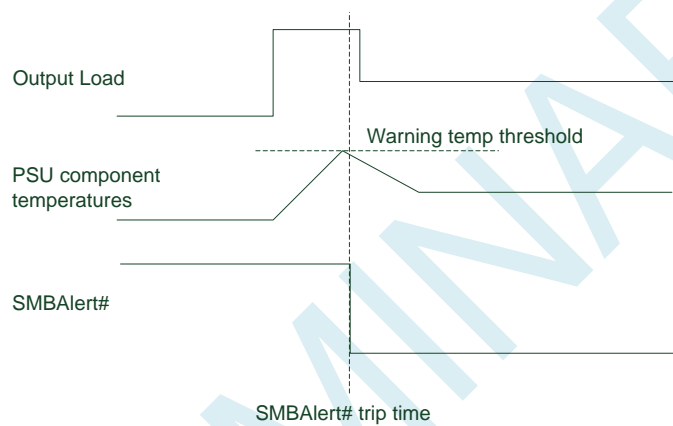


Figure 2. CLST Timing Requirements

#### 4.6 SMART RIDE-THROUGH (SmaRT)

The power supply will assert the SMBAlert# signal < 4 ms after AC input voltage is lost to 0 VAC.



## 5 CONTROL

The following sections define the input and output signals from the power supply. Signals that can be defined as low true use the following convention: Signal# = low true

### 5.1 DEVICE ADDRESS LOCATION (A0; A1)

This signal is defined by end user system for Power Management Bus communication, to allocate address of power supply unit in particular slot location. This signal has a 10 kohm internal resistor to internal 3.3 V located in power supply

SIGNAL TYPE	PULL-UP TO INTERNAL 3.3 V LOCATED IN POWER SUPPLY	
Adress_A0/A1 = high	Address 1	
Adress_A0/A1 = low	Address 0	
	MIN	MAX
Logical Level Low	0 V	0.4 V
Logical Level High	2.0 V	3.46 V

### 5.2 I2C BUS (SCL; SDA)

Each module shall provide SCL/SDA bus for EEPROM read/write of system. It's pull up from +3.3 V<sub>DD</sub> device by a 10 kohm resistor. SCL/SDA pin should be link together and closer. The SCL/SDA bus total capacitance must lower 100 pF from system and PDB. The max I2C bus speed is 400 kHz and the mcu of PSU is slave device in I2C bus. The time interval of I2C command is 1 ms.

### 5.3 SMBALERT#

This is an active low signal and indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. The signal shall activate in the case of critical component temperature reached a warning threshold, general failure, over-current, over-voltage, under-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits.

SIGNAL TYPE	OPEN COLLECTOR / DRAIN OUTPUT FROM POWER SUPPLY. PULL-UP TO 3.3 V <sub>SB</sub> LOCATED IN SYSTEM.	
Alert# = High	OK	
Alert# = Low	Power Alert to system	
	MIN	MAX
Logic level low voltage, I <sub>sink</sub> = 4 mA	0 V	0.4 V
Logic level high voltage, I <sub>source</sub> = 50 $\mu$ A	2.0 V	3.46 V
Sink current, Alert# = low		4 mA
Source current, Alert# = high		50 $\mu$ A
Alert# fall time		10 $\mu$ s



## 5.4 PSON#

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the +54V power rail. When this signal is not pulled low by the system, or left open, the outputs (except the +12VSB) turn off.

The power supply shall provide an internal pull-up resistor to high. The power supply shall also provide de-bounce circuitry on PSON# to prevent it from oscillating On/Off at startup when activated by mechanical switch.

Provisions for de-bouncing will be included in the PSON# circuitry to prevent the power supply from oscillating on/off at startup.

SIGNAL TYPE			ACCEPTS AN OPEN COLLECTOR/DRAIN INPUT FROM THE SYSTEM. PULL-UP TO INTERNAL VCC LOCATED IN POWER SUPPLY
PSON# = Low			PSU ON
PSON# = Open or High			PSU OFF
	MIN		MAX
Logic level low (PSU ON)	0 V		1 V
Logic level high (PSU OFF)	2.0 V		3.46 V
Source current, $V_{PSON\#} = \text{low}$			4 mA
Power up delay: $T_{PSON\#\_ON\_DELAY}$	5 ms		400 ms
Power off delay: $T_{PSON\#\_PWOK}$			5 ms

## 5.5 PWOK

This signal should be asserted high by the power supply to indicate that all outputs are within the regulation thresholds. Conversely, this signal should be de-asserted to a low state when any of the DC outputs voltage falls below its under voltage threshold, or when mains power has been removed for a time sufficiently long so that power supply operation can't be guaranteed.

This signal must be driven low at least 1ms before any of the outputs go out of regulation. Also, that will be defined and selected for inclusion from any variation of the following three items:

- A.) AC Power Loss
- B.) Fan Failure
- C.) Over Temperature

This signal will have an internal pull-up resistor to internal 3.3 V sources.

SIGNAL TYPE			OPEN COLLECTOR/DRAIN OUTPUT FROM POWER SUPPLY. PULL-UP TO VSB LOCATED IN THE POWER SUPPLY.
PWOK or P_Good = High			DC Outputs O.K.
PWOK or P_Good = Low			DC Outputs N.G.
	MIN		MAX
Logical Level Low, $I_{SINK} = 400 \mu A$	0 V		0.4 V
Logical Level High, $I_{SOURCE} = 200 \mu A$	2.4 V		3.46 V
Sink current, PWOK = low			400 $\mu A$
Source current, PWOK = high			2 mA
PWOK delay: $T_{PWOK\_ON}$	100 ms		500 ms
Power down delay: $T_{PWOK\_OFF}$	1 ms		
PWOK or P_Good Rise & Fall Time			100 $\mu s$

## 5.6 COLD REDUNDANCY BUS

This is a common specification defining Cold Redundancy requirements uses in redundant power supplies. It covers both power supply and system requirements supporting redundant configurations of 1+1, 2+2, and 3+1. Cold Redundancy uses the PMBus manufacturer specific command area to define SMBus commands for the system to communicate with the power supplies for enabling, configuration, and monitoring.



5.7 PRESENT#

This signal is an active low type signal and is connected to the power supply’s output ground internally. The mating pin of this signal in system side should have a pull-up resistor which limit the max. current 4mA to go through from this signal pin to the power supply. A Low state on this signal indicates the PSU is physically presents.

5.8 Vin\_good

This signal is an output to indicate AC power is existence and is within operation range. It should act from high to low level within 4 ms only for Vin drops out to zero and input voltage brown-out events. The 4 mS timing is defined as Vin = 0 to Vin\_good signal low level.

SIGNAL TYPE	PULL-UP 1KΩ TO INTERNAL 3.3 V LOCATED IN POWER SUPPLY	
Vin_good = High	Input voltage is in operating range	
Vin_good = low	Input voltage is out of operating range	
	MIN	MAX
Logical Level Low, ISINK = 4 mA	0 V	0.4 V
Logical Level High, ISOURCE = 50 μA	2.4 V	3.46 V
Sink current, Vin_good = low		4 mA
Source current, Vin_good = high		50 μA
Vin_good Rise & Fall Time		400 μs

Table 1. Vin\_good Signal Characteristics

5.9 REMOTE SENSE-

The power supply has return remote sense to regulate out ground drops in the system for the main output voltage. The return remote sense is able to regulate out a maximum of 300mV of drop on the ground output.

5.10 REMOTE SENSE+

The power supply uses +54V remote sense to regulate out +54V drops in the system for the main output voltage. The +54V remote sense is able to regulate out a maximum of 300mV of drop on the +54V output.



## 6 FRU REQUIREMENTS

### 6.1 FRU DATA

The FRU data format shall be compliant with the IPMI ver.1.0 (per rev.1.1 from Sept.25, 1999) specification. The following is the exact listing of the EEPROM content. During testing this listing shall be followed and verified.

### 6.2 FRU DEVICE PROTOCOL

The FRU device will implement the same protocols, including the Byte Read, Sequential Read, Byte Write, and Page Read protocols.

Four pins will be allocated for the FRU information on the Power Supply connector. One pin is the serial clock (SCL). The second pin is used for serial data (SDA). Two pins are for address lines to indicate to the power supply's EEPROM which position the power supply is located in the system. The SCL and SDA signals are pulled up by system, the address lines are also pulled up by system.

A1 LOGICAL VOLTAGE	A0 LOGICAL VOLTAGE	PSU ADDRESS	FRU ADDRESS
0	0	0xB0	0xA0
0	1	0xB2	0xA2
1	0	0xB4	0xA4
1	1	0xB6	0xA6

## 7 POWER MANAGEMENT BUS

Refer to the Power Management Bus application profile for systems for requirements.

Note. Power Management Bus signal should be pull up to 3.3 V only inside PSU.

### 7.1 POWER MANAGEMENT BUS COMMAND SET

The following table shows mandatory Power Management Bus commands to be supported by the PSU.

COMMAND CODE	COMMAND NAME	SMBUS TRANSACTION TYPE:		NUMBER OF DATA BYTES	COMMENT
		Writing Data	Reading Data		
00h	PAGE	Write Byte	Read Byte	1	
01h	OPERATION	Write Byte	Read Byte	1	0x80 ON; 0x00 OFF Default: 0x80
02h	ON_OFF_CONFIG	Write Byte	Read Byte	1	Default: 0x1D
03h	CLEAR_FAULTS	Send Byte	N/A	0	
05h	PAGE_PLUS_WRITE	Block Write	N/A	Variable	
06h	PAGE_PLUS_READ	N/A	Block Write – Block Read	Variable	
19h	CAPABILITY	N/A	Read Byte	1	0xB0
1Ah	QUERY	N/A	Block Write – Block Read	1	
1Bh	SMBALERT_MASK	Write Word	Block Write – Block Read	2	
20h	VOUT_MODE		Read Byte	1	0x17 (n=-9)
21h	VOUT_COMMAND	Write Word	Read Word	2	
30h	COEFFICIENTS	N/A	Block Write – Block Read	5	Use for Ein/Eout
31h	POUT_MAX	N/A	Read Word	2	
3Ah	FAN_CONFIG_1_2	Write Byte	Read Byte	1	Default is duty
3Bh	FAN_COMMAND_1	Write Word	Read Word	2	
4Ah	IOUT_OC_WARN_LIMIT		Read Word	2	
51h	OT_WARN_LIMIT		Read Word	2	
5Dh	IIN_OC_WARN_LIMIT		Read Word	2	



6Ah	POUT_OP_WARN_LIMIT		Read Word	2	
6Bh	PIN_OP_WARN_LIMIT		Read Word	2	
78h	STATUS_BYTE		Read Byte	1	
Bit 6	OFF				
Bit 5	VOUT_OV_FAULT				
Bit 4	IOUT_OC				
Bit 3	VIN_UV				
Bit 2	TEMPERATURE				
Bit 1	CML				
79h	STATUS_WORD		Read Word	2	
Bit 7(H)	VOUT				
Bit 6	IOUT/POUT				
Bit 5	INPUT				
Bit 3	POWER_GOOD#				
Bit 2	FANS				
Bit 6(L)	OFF				
Bit 5	VOUT_OV_FAULT				
Bit 4	IOUT_OC_FAULT				
Bit 3	VIN_UV_FAULT				
Bit 2	TEMPERATURE				
Bit 1	CML				
7Ah	STATUS_VOUT		Read Byte	1	
Bit 7	VOUT_OV_FAULT				
Bit 4	VOUT_UV_FAULT				
7Bh	STATUS_IOUT		Read Byte	1	
Bit 7	Iout OC fault				
Bit 5	Iout OC warning				
Bit 1	Pout OP fault				
Bit 0	Pout OP warning				
7Ch	STATUS_INPUT		Read Byte	1	
Bit 7	Vin OV fault				
Bit 6	Vin OV warning				
Bit 5	Vin UV warning				
Bit 4	Vin UV fault				
Bit 3	Unit off for insufficient input				
Bit 1	Iin over current warning				
Bit 0	Pin over power warning				
7Dh	STATUS_TEMPERATURE		Read Byte	1	
Bit 7	OT fault				
Bit 6	OT warning				
7Eh	STATUS_CML		Read Byte	1	
Bit 7	Invalid COMMAND				
Bit 6	Invalid DATA				
Bit 5	PEC Failed				
81h	STATUS_FANS_1_2		Read Byte	1	
Bit 7	Fan 1 fault				
Bit 5	Fan 1 warning				
86h	READ_EIN	N/A	Block Read	6	DIRECT Data Format
87h	READ_EOUT	N/A	Block Read	6	DIRECT Data Format
88h	READ_VIN	N/A	Read Word	2	Linear
89h	READ_IIN	N/A	Read Word	2	Linear
8Bh	READ_VOUT	N/A	Read Word	2	Linear16
8Ch	READ_IOUT	N/A	Read Word	2	Linear
8Dh	READ_TEMPERATURE_1	N/A	Read Word	2	Ambient
8Eh	READ_TEMPERATURE_2	N/A	Read Word	2	SR Hotspot
8Fh	READ_TEMPERATURE_3	N/A	Read Word	2	PFC Hotspot
90h	READ_FAN_SPEED_1	N/A	Read Word	2	In RPM
96h	READ_POUT	N/A	Read Word	2	Linear
97h	READ_PIN	N/A	Read Word	2	Linear



98h	PMBUS_REVISION	N/A	Read Byte	1	1.2
99h	MFR_ID	Block Write	Block Read	Variable (3)	"bel"
9Ah	MFR_MODEL	Block Write	Block Read	Variable (16)	"XXXXXXXXXXXXXXXX"
9Bh	MFR_REVISION	Block Write	Block Read	Variable (3)	"RXX"
9Ch	MFR_LOCATION	Block Write	Block Read	Variable (5)	"CHINA"
9Dh	MFR_DATE	Block Write	Block Read	Variable (6)	"YYMMDD"
9Eh	MFR_SERIAL	Block Write	Block Read	Variable (19)	Serial Number
9Fh	APP_PROFILE_SUPPORT	N/A	Block Read	Variable (2)	Power Management Bus 1.2
A0h	MFR_VIN_MIN	N/A	Read Word	2	90V
A1h	MFR_VIN_MAX	N/A	Read Word	2	264V
A2h	MFR_IIN_MAX	N/A	Read Word	2	
A3h	MFR_PIN_MAX	N/A	Read Word	2	
A4h	MFR_VOUT_MIN	N/A	Read Word	2	51.3V
A5h	MFR_VOUT_MAX	N/A	Read Word	2	56.7V
A6h	MFR_IOUT_MAX	N/A	Read Word	2	
A7h	MFR_POUT_MAX	N/A	Read Word	2	
A8h	MFR_TAMBIENT_MAX	N/A	Read Word	2	55°C
A9h	MFR_TAMBIENT_MIN	N/A	Read Word	2	-5°C
AAh	MFR_EFFICIENCY_LL	N/A	Block Read	14	At 20%/50%/100%
ABh	MFR_EFFICIENCY_HL	N/A	Block Read	14	At 20%/50%/100%
B0h	PMBUS_MFR_CALIBRATION_0xB0	Block Write	Block Read	Variable	
C0h	MFR_MAX_TEMP_1	N/A	Read Word	2	55°C
C1h	MFR_MAX_TEMP_2	N/A	Read Word	2	120°C
C2h	MFR_MAX_TEMP_3	N/A	Read Word	2	100°C
D0h	MFR_COLD_REDUNDANCY_CONFIG	Write Byte	Read Byte	1	
D4h	MFR_HW_COMPATIBILITY	N/A	Read Word	2	
D5h	MFR_FWUPLOAD_CAPABILITY	N/A	Read Byte	1	
D6h	MFR_FWUPLOAD_MODE	Write Byte	Read Byte	1	
D7h	MFR_FWUPLOAD	Block Write	N/A		
D8h	MFR_FWUPLOAD_STATUS	N/A	Read Word	2	
D9h	MFR_FW_REVISION	N/A	Block Read	3	
DCh	MFR_BLACK_BOX	N/A	Block Read	237	
DDh	MFR_REAL_TIME	Block Write	Block Read	4	
DEh	MFR_SYSTEM_BLACK_BOX	Block Write	Block Read	40	
DFh	MFR_BLACKBOX_CONFIG	Write Byte	Read Byte	1	
E0h	MFR_CLEAR_BLACKBOX	Send Byte	N/A	1	

Table 2. Supported Power Management Bus Command

**Note:** Write protocol must include PEC (Packet Error Checking).

7.2 STATUS COMMANDS

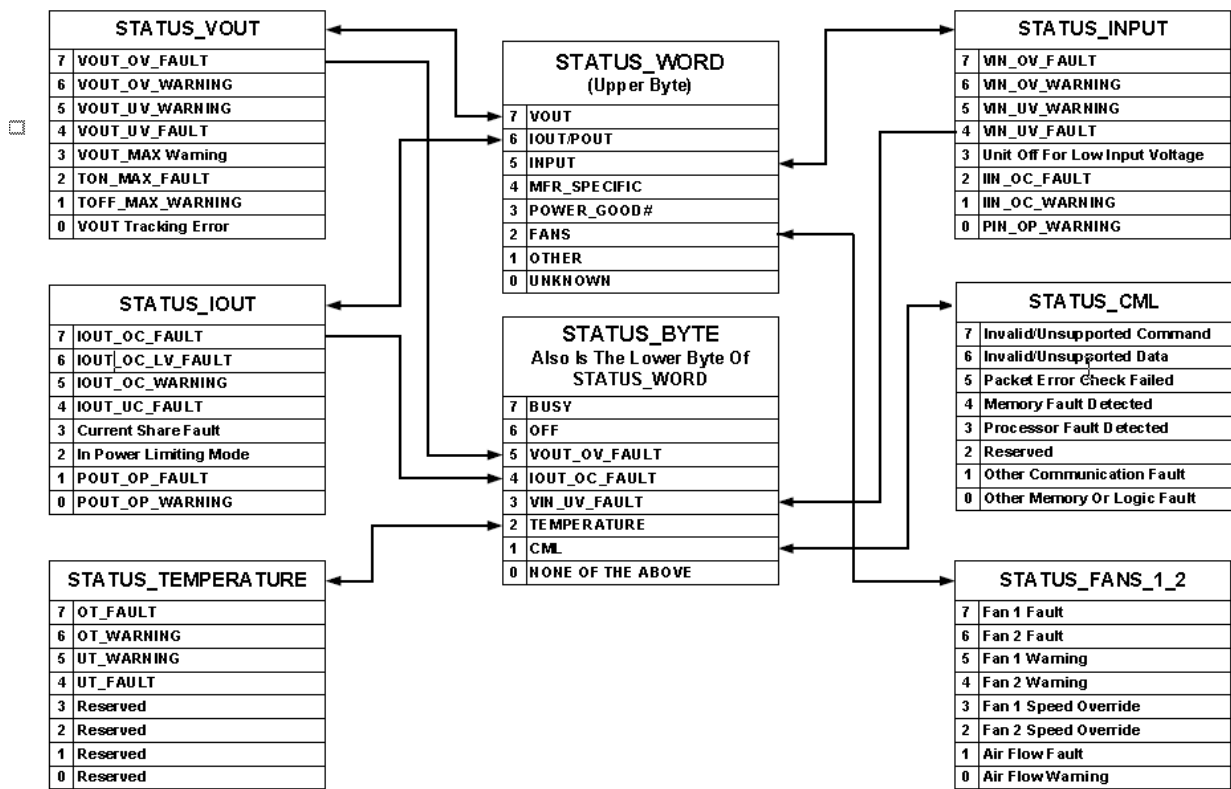


Figure 3. Summary of The Status Registers

The following Power Management Bus STATUS commands shall be supported. All STATUS commands stated in Figure 6 Supporting PAGE instances shall support the PAGE\_PLUS\_WRITE and PAGE\_PLUS\_READ commands since they are used by both the BMC and ME. The BMC and ME refer to the two instances of the commands accessed via the PAGE\_PLUS\_WRITE and PAGE\_PLUS\_READ commands. The status bits shall assert whenever the event driving the status bit is present. Once a bit is asserted it shall stay asserted until cleared

The STATUS commands that are supported with the PAGE\_PLUS\_READ and PAGE\_PLUS\_WRITE commands shall still support direct access of the base STATUS\_XXX commands using the read word, write word, read byte, and write byte protocols.

STATUS\_FAN\_1\_2 command is only accessed by the system BMC. It uses the standard read byte protocol to read status and write byte protocol to clear bits.

The STATUS events are also used to control the SMBAlert# signal. The new SMBALERT\_MASK command is used to define which status event control the SMBAAlert# signal. Default values for these mask bits are shown in the table below.



Power Management Bus command	Bit location	PSU state when bit is asserted ('1')	Instances No PAGE'ing2 PAGE 00h = BMC PAGE 01h = ME	SMBALERT_MASK defaults for each of the three instances (No PAGE, PAGE 00h, PAGE 01h) 0 = causes assertion of SMBAlert# 1 = does not cause assertion of SMBAlert#
STATUS_WORD			No PAGE'ing, 00h, 01h	
OFF	6 (lower)	OFF		NA
IOUT_OC_FAULT	4 (lower)	Refer to STATUS_IOUT		NA
VIN_UV_FAULT	3 (lower)	Refer to STATUS_INPUT		NA
TEMPERATURE	2 (lower)	Refer to STATUS_TEMPERATURE		NA
CML	1 (lower)	ON		NA
VOUT	7 (upper)	Refer to STATUS_VOUT		NA
IOUT/POUT	6 (upper)	Refer to STATUS_IOUT		NA
INPUT	5 (upper)	Refer to STATUS_INPUT		NA
FANS	2 (upper)	Refer to STATUS_FANS		NA
STATUS_VOUT			No PAGE'ing	
VOUT_OV_FAULT	7	OFF		1, 1, 1
VOUT_UV_FAULT	4	OFF		1, 1, 1
STATUS_IOUT			No PAGE'ing, 00h, 01h	
IOUT_OC_FAULT	7	OFF		1, 1, 1
IOUT_OC_WARNING	5	ON		1, 1, 0
POUT_OP_FAULT	1	OFF		1, 1, 1
POUT_OP_WARNING	0	ON		1, 1, 1
STATUS_INPUT			No PAGE'ing, 00h, 01h	
VIN_UV_WARNING	5	ON		1, 1, 1
VIN_UV_FAULT 1	4	OFF		1, 1, 0
Unit off for low input voltage	3	OFF		1, 1, 1
IIN_OC_WARNING	1	ON		1, 1, 1
PIN_OP_WARNING	0	ON		1, 1, 1
STATUS_TEMPERATURE			No PAGE'ing, 00h, 01h	
OT_FAULT	7	OFF		1, 1, 1
OT_WARNING	6	ON		1, 1, 0
STATUS_FANS_1_2			No PAGE'ing	
Fan 1 fault 3	7	OFF		1, 1, 1
Fan 1 warning 3	5	ON		1, 1, 1

Table 3. Power Management Bus STATUS Commands Summary

1. The Vin Fault bit in STATUS\_INPUT shall get asserted if the input power has dropped below the PSU's operating range for any duration of time; even if the PSU continues to operate normally through a momentary input dropout event.
2. 'No PAGE' is the standard STATUS\_ commands accessed directly without using the PAGE\_PLUS commands.



### 7.3 POWER MANAGEMENT BUS TEMPERATURE READ COMMANDS

The following temperature read commands as documented by the Power Management Bus specification Part II version 1.2 should be supported.

READ\_TEMPERATURE\_1(8Dh), should provide the PSU inlet temperature.

READ\_TEMPERATURE\_2(8Eh), should provide the temperature of the SR heat sink in the PSU.

READ\_TEMPERATURE\_3(8Fh), should provide the temperature of the PFC heat sink in the PSU.

### 7.4 PAGE (00h)

Setting a PAGE value of FFh is used to clear all status bits in all PAGEs with the CLEAR\_FAULT command.

### 7.5 OPERATION (01h)

The OPERATION command is used to configure the operational state of the converter, in conjunction with input from the CONTROL pin. The OPERATION command is used to turn the Power Management Bus device output on and off.

Bit [7] controls whether the Power Management Bus device output is on or off.

If Bit [7] is cleared (equals 0) then the output is off. If Bit [7] is set (equals 1), then the output is on.

### 7.6 ON\_OFF\_CONFIG (02h)

The ON\_OFF\_CONFIG command configures the combination of CONTROL pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied.

The default response for any Power Management Bus device is specified by the device manufacturer.

Example conditions:

If bit [4] is cleared, then the unit powers up and operates any time bias power is available regardless of the setting of bits [3:0].

If bit [4] is set, bit [3] is set, and bit [2] is cleared, then the unit is turned on and off only by commands received over the serial bus.

If bit [4] is set, bit [3] is cleared, and bit [2] is set, then the unit is turned on and off only by the CONTROL pin.

If bit [4] is set, bit [3] is set, and bit [2] is set, then the unit is turned on and off only when both the commands received over the serial bus AND the CONTROL pin are commanding the device to be on. If either a command from the serial bus OR the CONTROL pin commands the unit to be off, the unit turns off.

BIT NUMBER	PURPOSE	BIT VALUE	MEANING
[7:5]		000	Reserved For Future Use
4	Sets the default to either operate any time power is present or for the on/off to be controlled by	0	Unit powers up any time power is present regardless of state of the CONTROL pin
		1	Unit does not power up until commanded by the CONTROL pin and OPERATION command (as programmed in bits [3:0]).
3	Controls how the unit responds to commands received via the serial bus	0	Unit ignores the on/off portion of the OPERATION command from serial bus
		1	To start, the unit requires that that the on/off portion of the OPERATION command is instructing the unit to run. Depending on bit [2], the unit may also require the CONTROL pin to be asserted for the unit to start and energize the output.
2	Controls how the unit responds to the CONTROL pin	0	Unit ignores the CONTROL pin (on/off controlled only the OPERATION command)
		1	Unit requires the CONTROL pin to be asserted to start the unit. Depending on bit [3], the OPERATION command may also be required to instruct the device to start before the output is energized.
1	Polarity of the CONTROL pin	0	Active low (Pull pin low to start the unit)
		1	Active high (Pull high to start the unit)
0	CONTROL pin action when commanding the unit to turn off	0	Use the programmed turn off delay and fall time
		1	Turn off the output and stop transferring energy to the output as fast as possible. The device's product literature shall specify whether or not the device sinks current to decrease the output voltage fall time.

Table 4. ON\_OFF\_CONFIG Data Byte



## 7.7 CLEAR\_FAULTS COMMAND (03h)

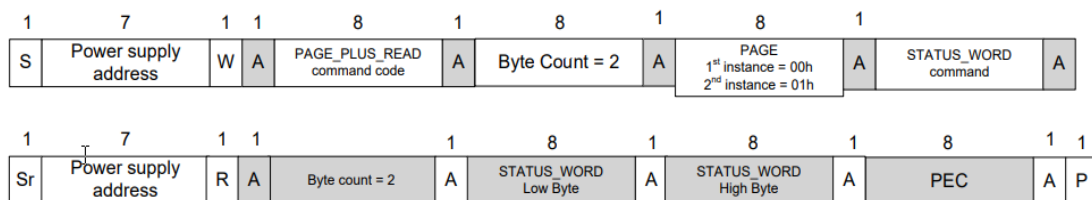
The CLEAR\_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device negates (clears, releases) its SMBALERT# signal output if the device is asserting the SMBALERT# signal.

## 7.8 PAGE\_PLUS\_WRITE / PAGE\_PLUS\_READ COMMANDS (05h/06h)

The new PAGE\_PLUS\_WRITE and PAGE\_PLUS\_READ commands are used with the STATUS\_WORD, STATUS\_INPUT, STATUS\_TEMPERATURE, STATUS\_IOUT, STATUS\_VOUT, and STATUS\_CML to create two instances of the same command. Each instance is set by the same events but cleared by their own master in the system. The instances at PAGE 00h are controlled by the system BMC and the instances at PAGE 01h are controlled by the system ME. Below are the protocols used to read and clear the STATUS\_ commands using the PAGE\_PLUS\_WRITE and PAGE\_PLUS\_READ commands.

Reading STATUS\_WORD

Block Write – Block Read Process Call with PEC



Reading STATUS\_TEMPERATURE, STATUS\_IOUT, STATUS\_INPUT, STATUS\_CML

Block Write – Block Read Process Call with PEC

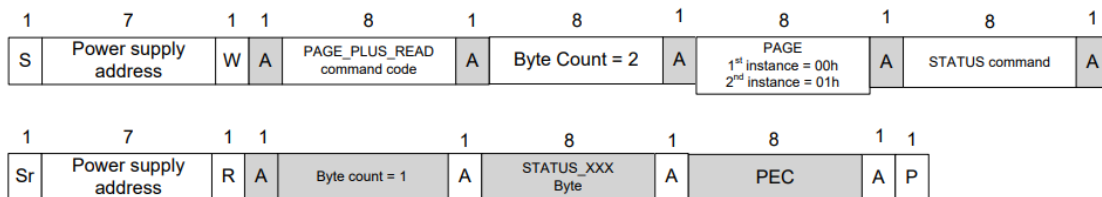
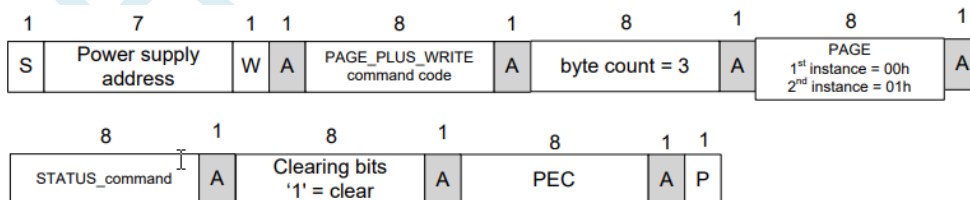


Figure 4. Reading STATUS commands with PAGE\_PLUS\_READ

Clearing STATUS commands (write '1' to clear a bit) STATUS\_TEMPERATURE, STATUS\_IOUT, STATUS\_INPUT, STATUS\_CML

Block Write with PEC



STATUS\_WORD cannot be cleared directly It is cleared based on lower level status commands

Figure 5. Clearing STATUS commands using PAGE\_PLUS\_WRITE

## 7.9 CAPABILITY (19h)

This command provides a way for a host system to determine some key capabilities of a Power Management Bus device. There is one data byte formatted as shown in table below. This command is read only.

BITS	DESCRIPTION	VALUE	MEANING
7	Packet Error Checking	0	Packet Error Checking not supported
		1	Packet Error Checking is supported
6:5	Maximum Bus Speed	00	Maximum supported bus speed is 100 kHz
		01	Maximum supported bus speed is 400 kHz
		10	Reserved
		11	Reserved
4	SMBALERT#	0	The device does not have a SMBALERT# pin and does not support the SMBus Alert Response protocol
		1	The device does have a SMBALERT# pin and does support the SMBus Alert Response protocol
3:0	Reserved	X	Reserved

Table 5. CAPABILITY COMMAND Data Byte Format

## 7.10 QUERY (1Ah)

The QUERY command is used to ask a Power Management Bus device if it supports a given command, and if so, what data formats it supports for that command. This command uses the Block Write-Block Read Process Call described in the SMBus specification.

BITS	VALUE	MEANING
7	1	Command is supported
	0	Command is not supported
6	1	Command is supported for write
	0	Command is not supported for write
5	1	Command is supported for read
	0	Command is not supported for read
4:2	000	Linear Data Format used
	001	16 bit signed number
	010	Reserved
	011	Direct Mode Format used
	100	8 bit unsigned number
	101	VID Mode Format used
	110	Manufacturer specific format used
	111	Command does not return numeric data. This is also used for commands that return blocks of data.
1:0	XX	Reserved for future use

Table 6. QUERY Command Returned Data Byte Format

If bit [7] is zero, then the rest of the bits are “don’t care”.



### 7.11 SMBALERT\_MASK (1Bh)

This allows the system to mask events from asserting the SMBAlert# signal and to read back this information from the PSU. SMBALERT\_MASK command can be used with any of the supported STATUS events. The events are masked from asserting SMBAlert# by writing a '1' to the associated STATUS bits. The SMBALERT\_MASK command is used in conjunction with the PAGE\_PLUS command and STATUS\_ commands. It is not supported for masking the Non-PAGE'd STATUS\_ commands. Below are the protocols.

#### Reading mask values using PAGE\_PLUS

##### Block Write – Block Read Process Call with PEC

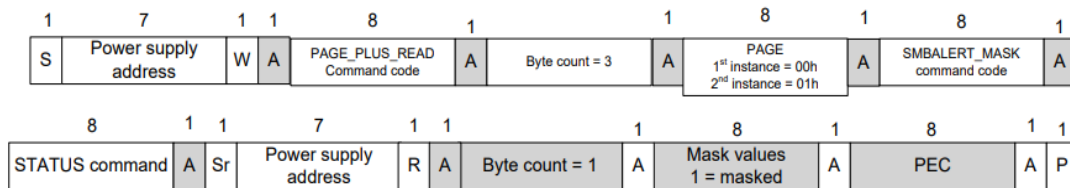
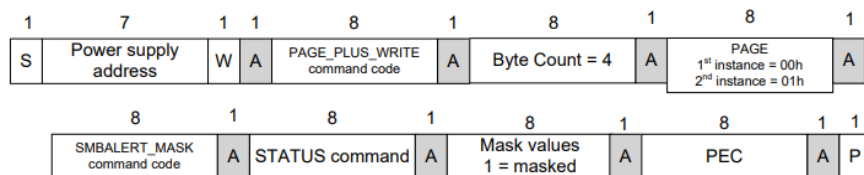


Figure 7. PAGE\_PLUS\_READ command.

#### Writing mask values using PAGE\_PLUS

##### Block Write with PEC



STATUS\_WORD is not used with SMBALERT\_MASK. Only the 'root' event bits are used to control the SMBAlert signal

Figure 8. PAGE\_PLUS\_WRITE command.

### 7.12 COEFFICIENT (30h)

The power supply shall support the Power Management Bus COEFFICIENT command. The system shall use this to read the values of m, b, and R used to determine READ\_EIN and READ\_EOUT accumulated power values.

COMMAND	COEFFICIENTS SUPPORT	M	B	R
READ_EIN	Yes	01h	00h	00h
READ_EOUT	Yes	01h	00h	00h

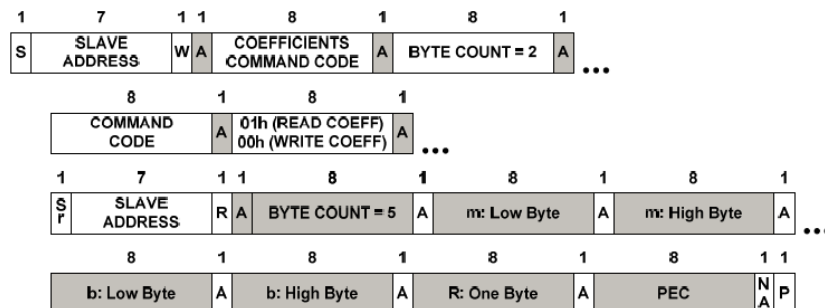


Figure 9. Retrieving Coefficients Using PEC

### 7.13 FAN\_CONFIG\_1\_2 (3Ah)

The FAN\_CONFIG\_1\_2 command is used to define the presence of a fan and the method it is controlled (by duty cycle or RPM).

The first of the configuration tells the Power Management Bus device whether or not a fan associated with position 1 (or 2) is installed. Any combination of fan installation is permitted.

The second part of the configuration tells the device whether the fan speed commands are in RPM or PWM duty cycle (in percent). These settings do not have to be the same for Fan 1 and Fan 2.

The third part of the configuration data tells the Power Management Bus device the number of tachometer pulses per revolution each fan provides. This information is needed for commanding and reporting fan speed in RPM. Two bits are provided for each fan. These settings do not have to be the same for Fan 1 and Fan 2. The binary values of these bits map to pulses per revolution as follows:

- 00b = 1 pulse per revolution,
- 01b = 2 pulses per revolution,
- 10b = 3 pulses per revolution,
- 11b = 4 pulses per revolution.

This command has one data byte formatted as follows:

BITS	VALUE	MEANING
7	1	Fan in position 1
6	0	Fan 1 commanded in Duty Cycle
	1	Fan 1 commanded in RPM
5:4	00b-11b	Fan 1 Tachometer Pulses Per Revolution
3	0	No fan in position 2
2	Not used	
1:0	Not used	

Table 7. FAN\_CONFIG\_1\_2 Command

### 7.14 FAN\_COMMAND\_1 (3Bh)

The system may increase the power supplies fan speed through using the FAN\_COMMAND\_1 command. This command can only increase the power supplies fan speed; it cannot decrease the PSU fan speed below what the PSU minimum speed of the thermal requirement.

The default control mode of fan is duty (0-100).

### 7.15 READ\_FAN\_SPEED\_1 (90h)

The system will read the fan speed by using the READ\_FAN\_SPEED\_1 command. This data shall return the fan speed in the Power Management Bus linear format.

### 7.16 POWER MANAGEMENT BUS\_REVISION (98h)

This is a correction to the table in the Power Management Bus part II specification regarding the POWER MANAGEMENT BUS\_REVISION command.

BITS [7:4]	PART I REVISION	BITS [3:0]	PART II REVISION
0000	1.0	0000	1.0
0001	1.1	0001	1.1
0010	1.2	0010	1.2
0011	1.3	0011	1.3

Table 8. POWER MANAGEMENT BUS\_REVISION Command



### 7.17 MFR-EFFICIENCY\_LL (AAh)

The MFR\_EFFICIENCY\_LL command sets or retrieves information about the efficiency of the device while operating at a low line condition. Not including the PEC byte, if used, and the byte count byte, there are fourteen data bytes as described below. The efficiency is specified at one input voltage and three data points consisting of output power and the efficiency at that output power. The three power ratings are typically referred as low, medium and high output power and are transmitted in that order. For example, the low, medium and high output power might correspond to 20%, 50% and 100% of the rated output power. The exact values of the output power is specified is left to the Power Management Bus device manufacturer. Each value (voltage, power or efficiency) is transmitted as two bytes in linear format.

BYTE NUMBER	BYTE ORDER	DESCRIPTION
0	Low Byte	The input voltage, in volts, at which the low line efficiency data is applicable. Note that byte 0 is the first data byte transmitted as part of the block transfer.
1	High Byte	
2	Low Byte	Power, in watts, at which the low power efficiency is specified
3	High Byte	
4	Low Byte	The efficiency, in percent, at the specified low power.
5	High Byte	
6	Low Byte	Power, in watts, at which the medium power efficiency is specified
7	High Byte	
8	Low Byte	The efficiency, in percent, at the specified medium power.
9	High Byte	
10	Low Byte	Power, in watts, at which the high power efficiency is specified
11	High Byte	
12	Low Byte	The efficiency, in percent, at the specified high power.
13	High Byte	

Table 9. MFR\_EFFICIENCY\_LL

### 7.18 MFR-EFFICIENCY\_HL (ABh)

The MFR\_EFFICIENCY\_HL command sets or retrieves information about the efficiency of the device while operating at a high line condition. Not including the PEC byte, if used, and the byte count byte, there are fourteen data bytes as described below. The efficiency is specified at one input voltage and three data points consisting of output power and the efficiency at that output power. The three power ratings are typically referred as low, medium and high output power and are transmitted in that order. For example, the low, medium and high output power might correspond to 20%, 50% and 100% of the rated output power. The exact values of the output power is specified is left to the Power Management Bus device manufacturer. Each value (voltage, power or efficiency) is transmitted as two bytes in linear format.

BYTE NUMBER	BYTE ORDER	DESCRIPTION
0	Low Byte	The input voltage, in volts, at which the high line efficiency data is applicable. Note that byte 0 is the first data byte transmitted as part of the block transfer.
1	High Byte	
2	Low Byte	Power, in watts, at which the low power efficiency is specified
3	High Byte	
4	Low Byte	The efficiency, in percent, at the specified low power.
5	High Byte	
6	Low Byte	Power in watts, at which the medium power efficiency is specified
7	High Byte	
8	Low Byte	The efficiency, in percent, at the specified medium power.
9	High Byte	
10	Low Byte	Power, in watts, at which the high power efficiency is specified
11	High Byte	
12	Low Byte	The efficiency, in percent, at the specified high power.
13	High Byte	

Table 10. MFR\_EFFICIENCY\_HL

### 7.19 READ\_EIN (86h)

The new READ\_EIN command is used to allow the system to apply its own input power filtering. This will allow the system to get faster input power data while preventing aliasing. The command returns an accumulated power value and an associated sample count of number of accumulated power values. This allows the system to calculate its own average power value each time the system polls the PSU.

	MIN	MAX	DESCRIPTION
Format	Power Management Bus Direct format m = 01h, R = 00h, b = 00h		Power Management Bus data format; refer to Power Management Bus specification for details.
Psample averaging period	4 AC cycles		Period instantaneous input power is averaged over to calculate Psample.
READ_EIN update period	80/66.7ms (50/60Hz)		Period at which the power accumulator and sample counter are updated
Range of System polling period	1 sec	100 ms	The PSU shall be polled over this range of rates while testing accuracy.

IMPORTANT:

The PSU READ\_EIN update period MUST always be less than the system polling period. To make sure the PSU is compatible with all possible system polling periods; the PSU must update the READ\_EIN power accumulator and sample counter at a period less than 100msec (required period is 4 AC cycles 80/67msec).

Table 11. READ\_EIN Requirements Summary

### 7.20 READ\_EOUT (87h)

The new READ\_EOUT command is used to allow the system to apply its own output power filtering. This will allow the system to get faster output power data while preventing aliasing. The command returns an accumulated power value and an associated sample count of number of accumulated power values. This allows the system to calculate its own average power value each time the system polls the PSU.

	MIN	MAX	DESCRIPTION
Format	Power Management Bus Direct format m = 01h, R = 00h, b = 00h		Power Management Bus data format; refer to Power Management Bus specification for details.
Psample averaging period	Nominal 50 ms		Period instantaneous input power is averaged over to calculate Psample.
Sampling period	Nominal 50 ms		Period at which the power accumulator and sample counter are updated
System polling rate	1 sample /s	10 samples /s	The PSU shall be polled over this range of rates while testing accuracy.

Table 12. READ\_EOUT Requirements Summary



## 7.21 READ\_EIN & READ\_EOUT FORMATS

The READ\_EIN and READ\_EOUT commands shall use the Power Management Bus direct format to report an accumulated power value and the sample count. The Power Management Bus coefficients m, R, and b shall be fixed values and the PSU shall report these values using the Power Management Bus COEFFICIENT command. The coefficient m shall be set to 01h, coefficient R shall be set to 00h, and coefficient b shall be set to 00h.

READ\_EIN and READ\_EOUT shall use the SMBus Block Read with PEC protocol in the below format.

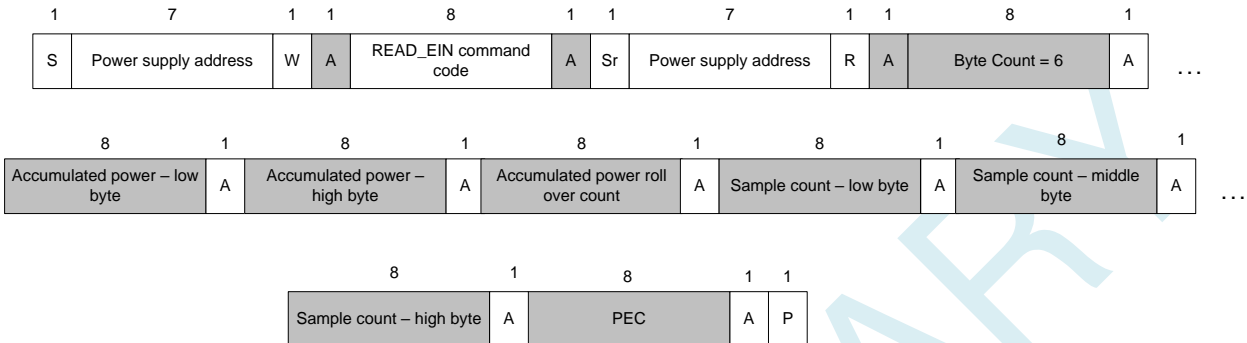


Figure 10. READ\_EIN Command

The accumulated power data shall be the sum of input power values averaged over 4 AC cycles (or over 50ms for READ\_EOUT). The value shall automatically roll-over when the 15 bit maximum value is reached ( $> 7FFFh$ ). The sample count should increment 1 for each accumulated power value. The system shall calculate average power by dividing the accumulated power value by the sample count. The system must sample READ\_EIN and READ\_EOUT faster than the roll-over period to get an accurate power calculation. Below is a block diagram depicting the accumulator function in the PSU.

### IMPORTANT NOTE:

When the PSU responds to the system requesting READ\_EIN or READ\_EOUT data; the data in the sample count must always alignment with the number of samples accumulated in the power accumulator. To achieve this power accumulator, power rollover counter, and sample counter shall be loaded into a READ\_EIN and READ\_EOUT register at the same time.

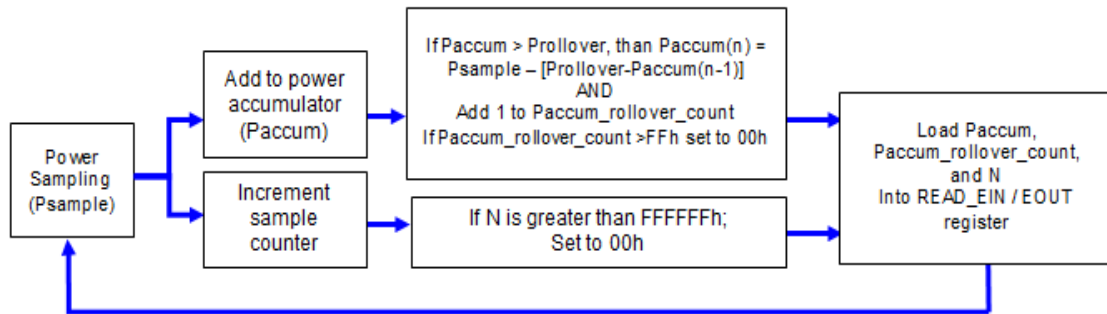


Figure 11. READ\_EIN PSU Functional Diagram

VALUE	DESCRIPTION
Psample:	The sampled power value in linear or direct format
Paccum:	2 bytes in Power Management Bus linear or direct format. The accumulated power values made up of Psample(0) + Psample(1) + ... + Psample(n)
N:	3 byte unsigned integer value. The number of accumulated power values summed in Paccum
Prollover:	The max value of Paccum before a rollover will occur
Paccum_rollover_count:	1 byte unsigned integer counting the number of times Paccum rolls over. Once this reaches FFh; it will automatically get reset to 00h



## 7.22 POWER SUPPLY ACCURACY

The following Power Management Bus commands shall be supported for the purpose of monitoring current, voltage, and power. All sensors shall continue providing real time data as long as the Power Management Bus device is powered. This means in standby mode the main output(s) of the PSU shall be zero amps and zero volts. Sensors shall meet requirements from 100 VAC to 127 VAC and from 200 VAC to 240 VAC; DC input: 220 VDC -260 VDC); maximum deviation for the ambient temperature is +/- 4°C.

	10% - <20% Load	>= 20% - 50% Load	> 50% - 100% Load
PIN / EIN	+/- 3%	+/- 3%	+/- 3%
VIN		+/- 3%	
IIN	+/-3%	+/-2%	+/-2%
FAN		+/- 500 rpm	
54VOUT		+/- 2%	
IOUT	+/-1A	+/-2%	+/-2%
POUT	+/- 3%	+/-2%	+/-2%
AMB Temperature		+/- 3°C	

Table 13. Power Management Bus Accuracy for AC-DC Models

### Notes:

1. The spec is based on input voltage 115Vac, 230Vac and 240Vdc measurement, the Max. output may be different between low and high line, the load definition where is taken Max. value.
2. In 240Vdc application, no matter the input polarity is positive or negative, the PSU could operate normally, but Accuracy shall be measured when positive polarity on Neutral. If customer may apply positive polarity on either one, please inform bel early.
3. For light load reporting requirement, in the normal redundant application, PSU shall report below value to system once the below condition is set, which is not included the PSU that in cold redundant mode and set as slave. When  $I_{in} < 0.2A$ , report 0.2A when  $P_{in} \leq 10W$ , report 10W when  $I_{out} < 1A$ , report 1A when  $P_{out} \leq 7W$ , report 7W. For system power calculation requirement, the reporting performance shall make sure the  $P_{in} > P_{out}$  situation.
4. The accuracy of AMB temperature is defined as the temperature around the temperature sensor inside of PSU, thereby this accuracy performance shall measure the closest point on the inlet chassis to internal temperature sensor.



### 7.23 LINEAR DATA FORMAT

The Linear Data Format is typically used for commanding and reporting the parameters such as (but not only) the following:

- Output Current,
- Input Voltage,
- Input Current,
- Operating Temperatures,
- Time (durations), and Energy Storage Capacitor Voltage.

The Linear Data Format is a two byte value with:

- An 11 bit, two's complement mantissa and,
- A 5 bit, two's complement exponent (scaling factor),

The format of the two data bytes is illustrated in Figure as show below.

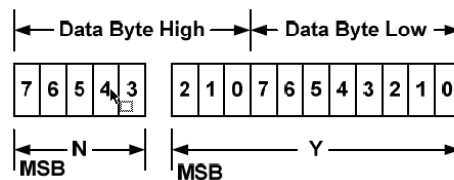


Figure 12. Linear Data Format Data Bytes

The relation between  $Y$ ,  $N$  and the "real world" value is:

$$X = Y \cdot 2^N$$

Where, as described above:

$X$  is the "real world" value;

$Y$  is an 11 bit, two's complement integer; and

$N$  is a 5 bit, two's complement integer.

Devices that use the linear format must accept and be able to process any value of  $N$ .

7.24 VOUT\_MODE (20h)

The data byte for the VOUT\_MODE command is one byte that consists of a three bit Mode and a five bit exponent. The three bit Mode shall be set to indicate the LINEAR mode for output voltage related commands. The five bit Exponent shall be set to indicate the value of the five bit two's complement exponent for the mantissa delivered as the data bytes for an output voltage related command.

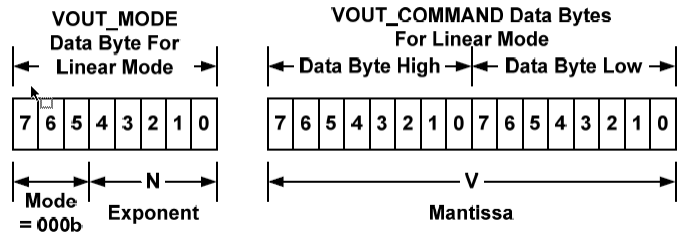


Figure 13. Linear Format Data Bytes

The voltage, in volts, is calculated from the equation  $\text{Voltage} = V \cdot 2^N$ , where:

- V is a 16 bit unsigned binary integer
- N is a 5 bit two's complement binary integer

Sending the VOUT\_MODE command with the address set for writing is not supported. If the system sends a VOUT\_MODE command for a write, the power supply shall reject the command, and set the Invalid/Unsupported Data bit in the STATUS\_CML register.

## 8 COLD REDUNDANCY

### 8.1 OVERVIEW

Below is a block diagram showing the Cold Redundancy architecture. When the power subsystem is in Cold Redundant mode; only the needed power supply to support the best power delivery efficiency are ON. Any additional power supplies; including the redundant power supply, is in Cold Standby state.

Each power supply has an additional signal that is dedicated to supporting Cold Redundancy; CR\_BUS. This signal is a common bus between all power supplies in the system. CR\_BUS is asserted (pulled low) when there is a fault in any power supply OR the power supplies output voltage falls below the  $V_{\text{fault}}$  threshold. Asserting the CR\_BUS signal causes all power supplies in Cold Standby state to power ON.

Enabling power supplies to maintain best efficiency is achieved by looking at the Load Share bus voltage and comparing it to a programmed voltage level via a PMBus command.

Whenever there is no Cold Redundant active power supply on the Cold Redundancy bus driving a HIGH level on the bus all power supplies are ON no matter their defined Cold Redundant roll (active or Cold Standby). This guarantees that incorrect programming of the Cold Redundancy states of the power supply will never cause the power subsystem to shut down or become over loaded. The default state of the power subsystem is all power supplies ON. There needs to be at least one power supply in Cold Redundant Active state or Standard Redundant state to allow the Cold Standby state power supplies to go into Cold Standby state.

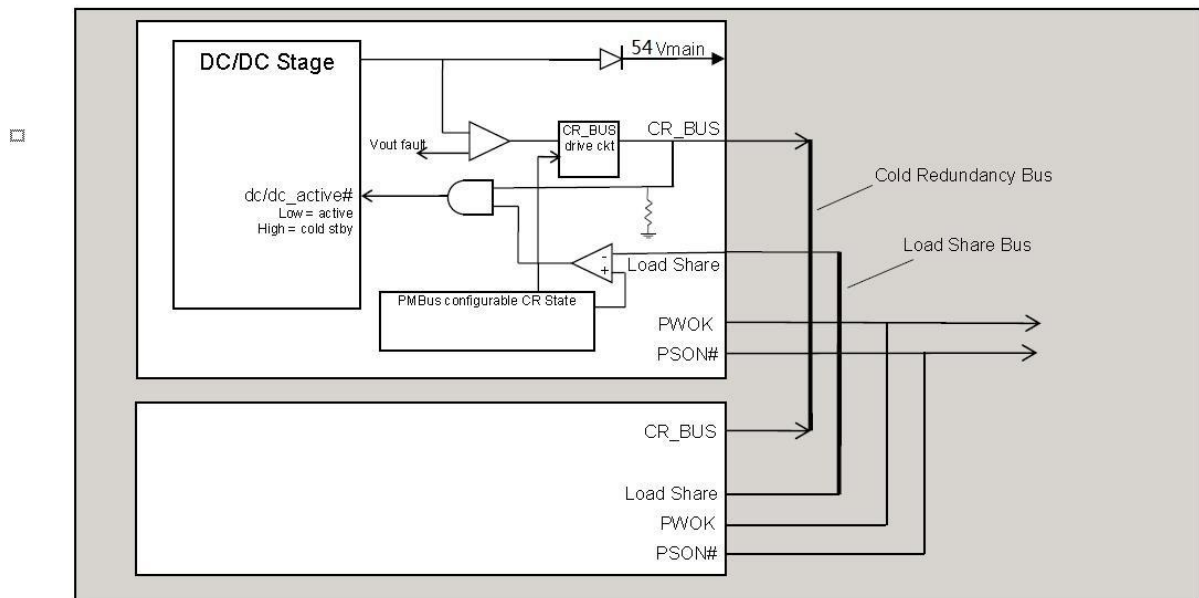


Figure 14. Cold Redundancy 1+1 Functional Block Diagram

SMART_ON_BUS	LOAD SHARE	DC/DC_ACTIVE#	SMART_ON STANDBY POWER SUPPLY STATE(S)
High	$< V_{\text{CR\_ON}}$	High	Cold Standby
Low	$< V_{\text{CR\_ON}}$	Low	Active
High	$> V_{\text{CR\_ON}}$	Low	Active
Low	$> V_{\text{CR\_ON}}$	Low	Active

Table 14. Logic Matrix for SMART\_ON Standby Power Supplies

## 8.2 POWERING ON COLD STANDBY SUPPLIES TO MAINTAIN BEST EFFICIENCY

Power supplies in Cold Standby state shall monitor the shared voltage level of the load share signal to sense when it needs to power on. Depending upon which position (1, 2, or 3) the system defines that power supply to be in the cold standby configuration; will slightly change the load share threshold that the power supply shall power on at.

	Enable Threshold for $V_{CR\_ON\_EN}$	Disable Threshold for $V_{CR\_ON\_DIS}$	CR_BUS De-asserted / Asserted States
Standard Redundancy	N/A; Ignore dc/dc_ active# signal; power supply is always ON		OK = Tri-state Fault = Low
Cold Redundant Active	NA; Ignore dc/dc_ active# signal; power supply is always ON		OK = High Fault = Low
Cold Standby 1 (02h)	3.2 V (40% of max)	$90\% \times (3.2V \times 1/2) = 1.44 V$	OK = Tri-state Fault = Low
Cold Standby 2 (03h)	5.0 V (62% of max)	$90\% \times (5.0V \times 2/3) = 3.01 V$	OK = Tri-state Fault = Low
Cold Standby 3 (04h)	6.7 V (84% of max)	$90\% \times (6.7V \times 3/4) = 4.52 V$	OK = Tri-state Fault = Low

Table 15. Example Load Share Threshold for Activating Supplies

Notes:

Maximum load share voltage = 8.0 V at 100% of rated output power

These are example load share bus threshold; for any power supply these shall be customized to maintain the best efficiency curve that specific model.

## 8.3 POWERING ON COLD STANDBY SUPPLIES DURING A FAULT OR OVER CURRENT CONDITION

When an active power supply asserts its CR\_BUS signal (pulling it low), all parallel power supplies in cold standby mode shall power on within 100µsec.

## 8.4 COLD REDUNDANCY SMBUS COMMANDS

The Power Management Bus manufacturer specific command MFR\_SPECIFIC\_00 is used to configure the operating state of the power supply related to SMART\_ON redundancy. We will call the command Cold\_Redundancy\_Config (D0h).

Below is the definition of the values used with the Read-Write Byte SMBus protocol with PEC.

VALUE	STATE	DESCRIPTION
00h	Standard Redundancy (default power on state)	Turns the power supply ON into standard redundant load sharing more. The power supply's CR_BUS signal shall be in Tri-state but still pull the bus low if a fault occurs to activate any power supplies still in Cold Standby state.
01h	Cold Redundant Active	Defines this power supply to be the one that is always ON in a cold redundancy configuration.
02h	Cold Standby 1*	Defines the power supply that is first to turn on in a cold redundant configuration as the load increases.
03h	Cold Standby 2*	Defines the power supply that is second to turn on in a cold redundant configuration as the load increases.
04h	Cold Standby 3*	Defines the power supply that is third to turn on in a cold redundant configuration as the load increases.
05h	Always Standby	Defines this power supply to be always in cold redundant configuration no matter what the load condition

\* When the CR\_BUS transitions from a high to a low state; each PSU programmed to be in Cold Standby state shall be put into Standard Redundancy mode (Cold\_redundancy\_Config = 00h). For the power supplies to enter Cold Redundancy mode the system must re-program the power supplies using the Cold\_Redundancy\_Config command.

Table 16. Cold\_Redundancy\_Config (D0h)

## 8.5 COLD REDUNDANT SIGNALS

There is an additional signal defined supporting Cold Redundancy. This is connected to a bus shared between the power supplies; the CR\_BUS.



## 9 BLACK BOX

### 9.1 BLACK BOX FUNCTION DESCRIPTION

This specification defines the requirements for power supplies with Power Management Bus capability to store Power Management Bus and other data into non-volatile memory inside the power supply. The data shall be saved to non-volatile memory upon a critical failure that caused the power supply to shutdown. The data can be accessed via the Power Management Bus interface by applying power to the 12Vstby pins. No AC power need to be applied to the power supply.

### 9.2 WHEN IS DATA SAVED TO THE BLACK BOX?

Data is saved to the Black Box for the following fault events:

- General fault
- Over voltage on output
- Over current on output
- Loss of AC input
- Input voltage fault
- Fan failure
- Over temperature

### 9.3 BLACK BOX EVENTS

There are two types of data saved in the black box:

- 1) System Tracking Data.
- 2) Power supply event data.

System tracking data is saved to the Black Box whenever the system powers ON or when a power supply is added to the system.

### 9.4 BLACK BOX PROCESS

- System writes system tracking data to the power supply RAM at power ON.
- System writes the real time clock data to the PSU RAM once every ~5 minutes.
- Power supply tracks number of PSON# and AC power cycles in EEPROM.
- Power supply tracks ON time in EEPROM
- Power supply loads warning and fault event counter data from EEPROM into RAM
- Upon a warning event; the PSU shall increment the associated counter in RAM.
- Upon and fault event the PSU shall increment the associated counter in RAM
- Upon a fault event that causes the PSU to shut down all event data in the PSU's RAM is saved to event data location N in the power supply's EEPROM. This data includes the real time clock, number of AC & PSON# power cycles, PSU ON time, warning event counters and fault event counters.

### 9.5 RELATED COMMAND OF BLACK BOX

The following command set will be used for Black Box function via the Host System. The commands and protocol used by the Host System and shall be implemented by the microcontroller are defined by this document.

COMMAND CODE	COMMAND NAME	SMBUS TRANSACTION TYPE	NUMBER OF DATA BYTES	REMARK
DCh	MFR_BLACK_BOX	Read only	237	Read the data of the Black box.
DDh	MFR_REAL_TIME	Read/Write	4	Read/Write the data of MFR real time.
DEh	MFR_SYSTEM_BLACK_BOX	Read/Write	40	Read/Write the data of MFR system black box.
DFh	MFR_BLACKBOX_CONFIG	Read/Write	1	Read/Write the data of MFR black box configure.
E0h	MFR_CLEAR_BLACKBOX	Write only	1	Send one byte to clear all data of black box.

## 1) Command Name: MFR\_BLACKBOX

Format: Read Block with PEC (237 bytes)

Code: DCh

ITEM		NUMBER OF BYTES	DESCRIPTION
System Tracking Data	System top assembly number	10	The system will write its Intel part number for the system top assembly to the power supply when it is powered ON. This is 9 ASCII characters.
	System serial number	10	The system shall write the system serial number to the power supply when it is powered ON. This includes the serial number and date code.
	Motherboard assembly number	10	The system will write the motherboard Intel part number for the assembly to the power supply when it is powered ON. This is 9 ASCII characters.
	Motherboard serial number	10	The system shall write the motherboard's serial number to the power supply when it is powered ON. This includes the serial number and date code.
	Present total PSU ON time	3	Total on time of the power supply with PSON# asserted in minutes. LSB = 1 minute.
	Present number of AC power cycles	2	Total number of times the power supply powered OFF then back ON due to loss of AC power. This is only counted when the power supply's PSON# signal is asserted. This counter shall stay at FFFFh once the max is reached.
	Present number of PSON# power cycles	2	Total number of times the power supply is powered OFF then back ON due to the PSON# signal de-asserting. This is only counted when AC power is present to the power supply. This counter shall stay at FFFFh once the max is reached.
Power supply event data (N)		38	Most recent occurrence of saved black box data
Time Stamp			The power supply shall track these time and power cycle counters in RAM. When a black box event occurs, the data is saved into the Black Box.
	Power supply total power on time	3	Total on time of the power supply in minutes. LSB = 1 minute.
	Real Time Clock Data from System (reserved for future use)	4	This time stamp does not need to be generated by the power supply. The system rights a real time clock value periodically to the power supply using the MFR_REAL_TIME command. Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970. This format is sufficient to maintain time stamping with 1-second resolution past the year 2100. This is based on a long-standing UNIX-based standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSI C.
	Number of AC power cycles	2	Number of times the power supply powered OFF then back ON due to loss of AC power at the time of the event. This is only counted when the power supply's PSON# signal is asserted.
	Number of PSON# power cycles	2	Number of times the power supply is powered OFF then back ON due to the PSON# signal de-asserting at the time of the event. This is only counted when AC power is present to the power supply.
Power Management Bus			The power supply shall save these Power Management Bus values into the Black Box when a black box event occurs. Fast events may be missed due to the filtering effects of the Power Management Bus sensors.
	STATUS_WORD	2	
	STATUS_IOUT	1	
	STATUS_INPUT	1	
	STATUS_TEMPERATURE	1	
	STATUS_FAN_1_2	1	
	READ_VIN	2	
	READ_IIN	2	
	READ_IOUT	2	
	READ_TEMPERATURE_1	2	



	READ_TEMPERATURE_2	2	
	READ_FAN_SPEED_1	2	
	READ_PIN	2	
	READ_VOUT	2	
Event Counters			The power supply shall track the total number for each of the following events. These values shall be saved to the black box when a black box event occurs. Once a value has reached 15, it shall stay at 15 and not reset.
	AC shutdown due to under voltage on input	Lower ½	The power supply shall save a count of these critical events to non-volatile memory each time they occur. The counters will increment each time the associated STATUS bit is asserted.
	Thermal shutdown	Upper ½	
	Over current or over power shutdown on output	Lower ½	
	General failure shutdown	Upper ½	
	Fan failure shutdown	Lower ½	
	Shutdown due to over voltage on output	Upper ½	The power supply shall save into RAM a count of these warning events. Events are count only at the initial assertion of the event/bit. If the event persists without clearing the bit the counter will not be incremented. When the power supply shuts down it shall save these warning event counters to non-volatile memory. The counters will increment each time the associated STATUS bit is asserted.
	Input voltage warning; no shutdown	Lower ½	
	Thermal warning; no shutdown	Upper ½	
	Output current power warning; no shutdown	Lower ½	
	Fan slow warning; no shutdown	Upper ½	
Power supply event data (N-1)		38	
Power supply event data (N-2)		38	
Power supply event data (N-3)		38	
Power supply event data (N-4)		38	

## 2) Name: MFR\_REAL\_TIME\_BLACK\_BOX

Format: Write/Read Block with PEC (4 bytes)

**Code: DDh**

The system shall use this command to periodically write the real time clock data to the power supply.

Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970. This format is sufficient to maintain time stamping with 1-second resolution past the year 2100. This is based on a long standing UNIX-based standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSIC.

## 3) Name: MFR\_SYSTEM\_BLACK\_BOX

Format: Write/Read Block with PEC (40 bytes). Low byte first.

**Code: DEh**

The system uses this command to write the following data to the PSU.

Item	Bytes	
System top assembly number	1-10	Low bytes
System serial number	11-20	
Motherboard assembly number	21-30	
Motherboard serial number	31-40	High bytes

1)



4) Name: MFR\_BLACKBOX\_CONFIG

Format: Read/Write Byte with PEC

Code: DFh

BIT	VALUE	DESCRIPTION
0	0 = disable black box function	Writing a 1 enables the power supply with black box function. Writing a 0 disables the power supply black box function. The state of MFR_BLACKBOX_CONFIG shall be saved in non-volatile memory so that it is not lost during power cycling. Intel shall receive the power supply with the black box function enabled; bit 0 = '1'.
	1 = enable black box function	
1-7		Reserved

5) Name: MFR\_CLEAR\_BLACKBOX

Format: Send Byte with PEC

Code: E0h

The MFR\_CLEAR\_BLACKBOX command is used to clear all black box records simultaneously.

This command is write only. There is no data byte for this command.

9.6 HARDWARE REQUIREMENTS

The SMBus interface shall be used to access the Black Box data. It may be accessed when the power supply is ON or in standby mode. It also may be accessed when no AC power is applied, and power is only applied at the standby output pins by an external source (12Vstby).



## 10 BOOTLOADER

### 10.1 FUNCTION DESCRIPTION

This specification defines the common architecture for in-system power supply firmware updates. It is required that the FW in the main microcontroller on the secondary side of the power supply must be able to be updated in the system using the In-System Firmware Update feature while in the ON state (i.e. with AC power present and PSON# asserted). It is desired that any other microcontroller in the power supply also be able to be updated with this same process (example: primary side microcontroller); however, this is not a requirement at this time.

### 10.2 FW IMAGE MAPPING

The power supply firmware image shall be made up of two parts; 1) Boot loader; 2) Main program. The system shall contain a backup of the power supply image in its BMC whenever updating the FW to the power supply.

#### 1) Boot Loader:

This is the part of the power supply firmware that is never updated by the system. The power supply shall always be able to recover and power ON into the boot loader mode no matter the state of the power supply's main program. This code shall support the In-System FW update code and basic power supply functions to power ON/OFF, fan cooling, and protections (UV, OV, OC).

#### 2) Main Program:

This is the fully functional power supply program space. There is no requirement to keep a backup image of this code in the power supply since a copy of the power support FW image shall always be kept in the system's BMC.

### 10.3 POWER SUPPLY OPERATING MODE DURING AND AFTER FIRMWARE UPDATE

#### 1) Firmware update mode in ON state with no power cycle needed:

Power supply may be able to support FW upload in the ON state. The new FW will take effect once it is taken out of FW upload load.

#### 2) Bad image after firmware update:

The power supply must always be able to power on in the boot loader mode with minimal operating capabilities even if the FW image sent to the power supply is bad or corrupt. If in this mode the power supply must be able to still enter the FW upload mode to upload a proper FW image to the PSU.

## 10.4 TEC3200-54-074NA FIRMWARE IMAGE HEADER

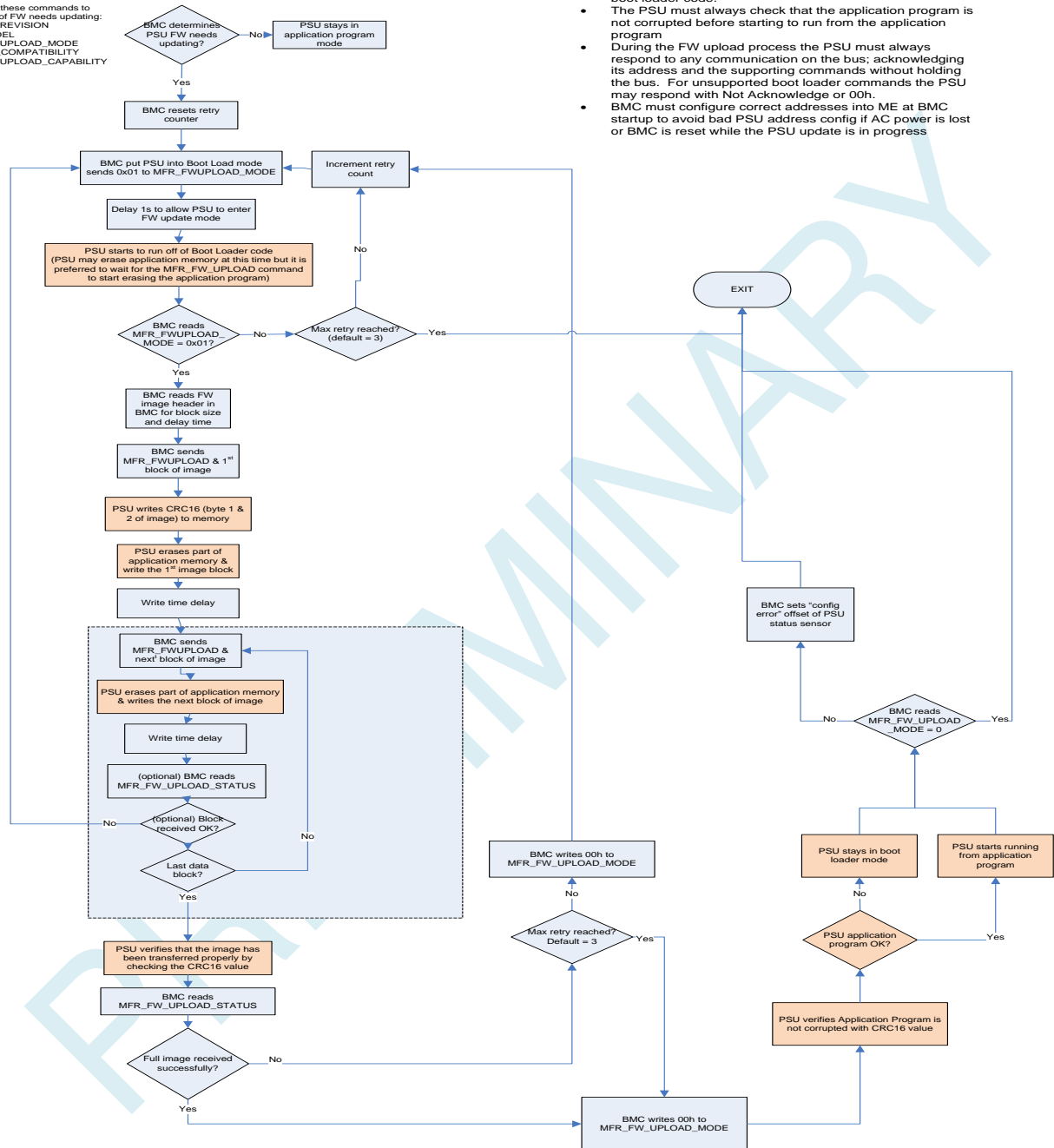
Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	T	Model Name 12 bytes
Byte 12	E	
Byte 13	C	
Byte 14	3	
Byte 15	2	
Byte 16	0	
Byte 17	0	
Byte 18	-	
Byte 19	N	
Byte 20	A	
Byte 21		
Byte 22		
Byte 23	Not used, for future use	Not used, for future use
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version).	Firmware Revision 3 bytes; in binary format
Byte 25	FW_MINOR_PRIMARY (not used by system)	
Byte 26	FW_MINOR_SECONDARY	
Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2 bytes
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

### 10.5 TEC3200-54-074RA FIRMWARE IMAGE HEADER

Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	T	Model Name 12 bytes
Byte 12	E	
Byte 13	C	
Byte 14	3	
Byte 15	2	
Byte 16	0	
Byte 17	0	
Byte 18	-	
Byte 19	R	
Byte 20	A	
Byte 21		
Byte 22		
Byte 23	Not used, for future use	Not used, for future use
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version).	Firmware Revision 3 bytes; in binary format
Byte 25	FW_MINOR_PRIMARY (not used by system)	
Byte 26	FW_MINOR_SECONDARY	
Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2 bytes
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

## 10.6 FIRMWARE UPDATE PROCESS

BMC uses these commands to determine if FW needs updating:  
MFR\_FW\_REVISION  
MFR\_MODEL  
MFR\_FW\_UPLOAD\_MODE  
MFR\_FW\_COMPATIBILITY  
MFR\_FW\_UPLOAD\_CAPABILITY

**IMPORTANT!**

- PSU may be in standby mode or ON mode during FW update process
- If the FW update process is interrupted at any point during the process; the PSU must always be able to return to the boot loader code.
- The PSU must always check that the application program is not corrupted before starting to run from the application program
- During the FW upload process the PSU must always respond to any communication on the bus; acknowledging its address and the supporting commands without holding the bus. For unsupported boot loader commands the PSU may respond with Not Acknowledge or 00h.
- BMC must configure correct addresses into ME at BMC startup to avoid bad PSU address config if AC power is lost or BMC is reset while the PSU update is in progress

Figure 15. PSU Upload Process

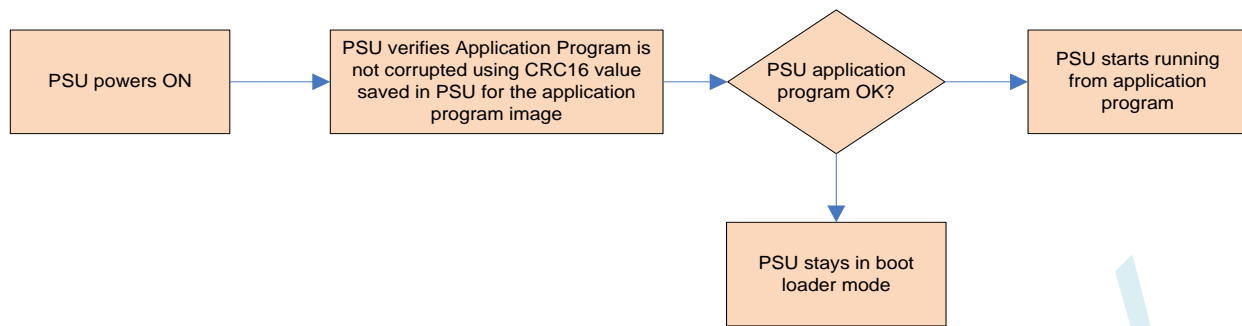


Figure 16. PSU flow during powering ON

## 10.7 RELATED COMMAND OF BOOTLOADER

### 1) Name: MFR\_HW\_COMPATIBILITY

Format: Read Word

Code: D4h

BYTES	VALUE	DESCRIPTION
low	ASCII code for first letter/number of the PSU HW compatibility.	This is a COMPATIBILITY value used to tell if there are any changes in the FW that create an incompatibility with the FW.
high	ASCII code for second letter/number of the PSU HW compatibility.	This value only changes when the PSU HW is changed creating an incompatibility with older versions of FW.

### 2) Name: MFR\_FWUPLOAD\_CAPABILITY

Format: Read Byte

Code: D5h

The system can read the power supply's FW upload mode capability using this command. For any given power supply; more than one FW upload mode may be supported. The supported FW upload mode(s) must support updating all available FW in the power supply.

BIT	VALUE	DESCRIPTION
0 (for future use)	1 = PSU support FW uploading in standby mode only	For future use
1 (for future use)	1 = PSU supports FW uploading in ON state; but all the new FW will not take effect until a power cycle with PSON#.	For future use
2	1 = PSU supports FW uploading in the ON state and no power cycle needed	Method used for updating the application program in the power supply
3-7	Reserved	

### 3) Name: MFR\_FWUPLOAD\_MODE

Format: Read/Write Byte

Code: D6h

BIT	VALUE	DESCRIPTION
0	0 = exit firmware upload mode 1 = firmware upload mode	Writing a 1 puts the power supply into firmware upload mode and gets it ready to receive the 1st image block via the MFR_FW_UPLOAD command. The system can use this command at any time to restart sending the FW image. Writing a 0 puts the power supply back into normal operating mode. Writing a 1 restarts This command will put the PSU into standby mode if the PSU supports FW update in standby mode only. If the power supply image passed to the PSU is corrupt the power supply shall stay in firmware upload mode even if the system requested the PSU to exit the FW upload mode.
1-7		Reserved

### 4) Name: MFR\_FWUPLOAD

Format: Block Write (block = size as defined by the image header)

Code: D7h

BYTES	VALUE	DESCRIPTION
Block size defined in header	Image header & image data	Command used to send each block of the FW image. Header should follow the format described in section 13.4. The image shall contain block sequencing numbers to make sure the PSU puts the right data blocks into the right memory space on the PSU MCU.



### 5) Name: MFR\_FWUPLOAD\_STATUS

Format: Read Word

Code: D8h

At any time during or after the firmware image upload the system can read this command to determine status of the firmware upload process.

Reset: all bits get reset to '0' when the power supply enters FW upload mode.

BIT	DESCRIPTION
0	1 = Full image received successfully
1	1 = Full image not received yet. The PSU will keep this bit asserted until the full image is received by the PSU.
2	1 = Full image received but image is bad or corrupt. Power supply can power ON, but only in 'safe mode' with minimal operating capability.
3 (for future use)	1 = Full image received but image is bad or corrupt. Power supply can power ON and support full features.
4	1 = FW image not supported by PSU. If the PSU receives the image header and determines that the PSU HW does not support the image being sent by the system; it shall not accept the image and it shall assert this bit.
5 – 15	Reserved

### 6) Name: MFR\_FW\_REVISION

Format: Block Read, 3 bytes

Code: D9h

BYTE	VALUE	DESCRIPTION
0	0 - 255	Minor revision; secondary
1	0 - 255	Minor revision; primary
2	0 - 255	Bit 7: 1-> Down grading of PSU FW has to be avoided. System BMC can elect to ignore this bit if needed but recommended to follow. 0-> No restriction in downgrading the PSU FW. BMC can update the PSU FW to be in sync with its known version. Bit 0-6: Major revision

### 7) MFR\_MODEL (existing Power Management Bus command)

Code: 9Ah

Maximum of 12 byte value; ending in terminator character.

### 8) MFR\_REVISION (existing Power Management Bus command)

Code: 9Bh



## 11 ELECTROMAGNETIC COMPATIBILITY

### 11.1 IMMUNITY

The power supply complies with the limits defined in EN 55024.

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Electrostatic Discharge	IEC / EN 61000-4-2	B
Radiated Immunity	IEC / EN 61000-4-3	A
Fast Transient / Burst	IEC / EN 61000-4-4	
Surge Immunity	IEC / EN 61000-4-5 (2 kV line to ground and 1 kV line to line)	A
Conducted Susceptibility	IEC / EN 61000-4-6	
Power Frequency Magnetic Immunity	IEC / EN 61000-4-8	
Voltage Dips and Interruptions	IEC / EN 61000-4-11	

### 11.2 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted & Radiated Emissions	EN 55032 / CISPR 32 / FCC	Class A 6 dB margin
Power Harmonics	EN 61000-3-2	Class A
Voltage Fluctuation and Flicker	EN 61000-3-3	Class A
Acoustic Noise	Variable speed fan(s) incorporated, measured accord. to ECMA 74 and reported according to ISO 9296.	TBD dBA

## 12 ENVIRONMENTAL

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Ambient Temperature	Operating TEC3200-12-074NA	-5		+55	°C
	Non-Operating	-40		+70	
Humidity	Operating, relative (non-condensing)	5		85	%
	Non-Operating, relative (non-condensing)	5		95	
Altitude *	Operating, T <sub>A</sub> = 45°C max.	0		5 000	ft
	Non-Operating	0		15 200	
Mechanical Shock (non-operating)	50 G Trapezoidal Wave, Velocity change = 170 in. / sec Three drops in each of six directions are applied to each of the samples.				
Vibration (non-operating) sinusoidal	1.5G, pk-pk, 10 Hz-500 Hz-10 Hz, 0.5 octave/min; 2 sweeps per axis. Three mutually perpendicular axes.				
Vibration (non-operating) random	2 Grms, 10 Hz-500 Hz, 60 mins per axis Three mutually perpendicular axes.				
Thermal Shock (non-operating)	50 cycles, 30°C /min. ≥ transition time ≥ 15°C /min duration of exposure to temperature extremes for each half cycle shall be 30 minutes.	-40		+70	°C
Audible Noise	@ 100% rated DC load and inlet T <sub>A</sub> = 25°C,			70	dB

\* The system ambient supports at 950 m (3000 feet) altitude. Maximum operating temperature is de-rated 1°C per 125 m above 950 m

## 13 RELIABILITY

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Mean time between failures (MTBF)	@ 230 VAC, T <sub>A</sub> = 50°C, 80% max. load, acc. to Telcordia SR-332	200 000			h



Asia-Pacific  
+86 755 298 85888

Europe, Middle East  
+353 61 49 8941

North America  
+1 866 513 2839

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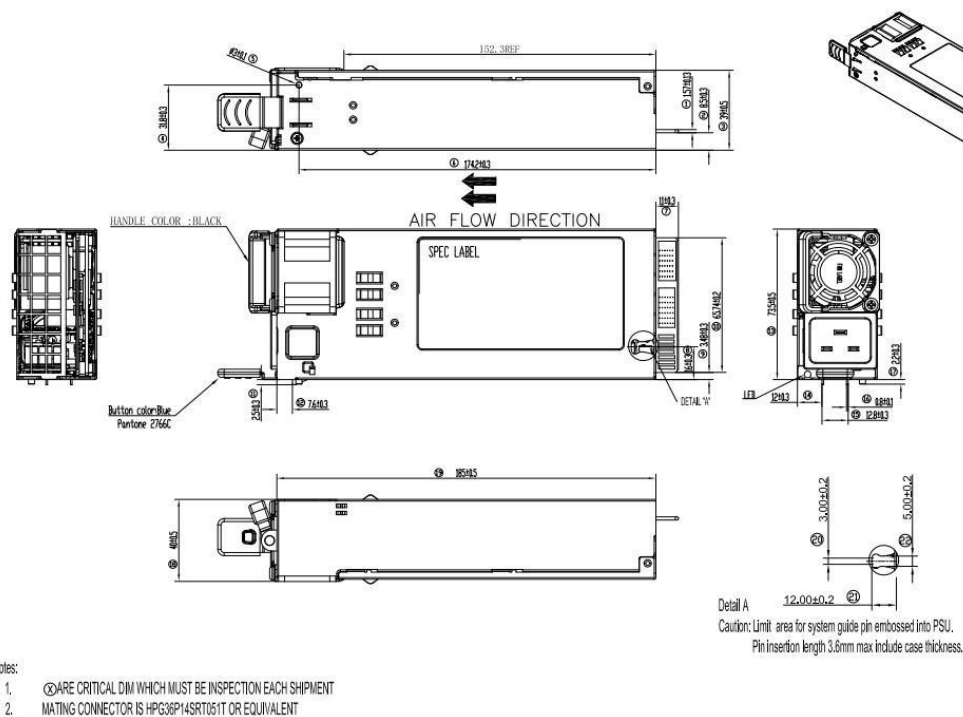
BCD.20287\_1

## 14 SAFETY / APPROVALS

PARAMETER	DESCRIPTION / CONDITION
Agency Approvals	<ul style="list-style-type: none"> <li>UL/CSA 62368-1 (USA/Canada)</li> <li>EN/IEC 62368-1 (Europe/International)</li> <li>CB Certificate &amp; Report, IEC 62368-1 (Report to include all country national deviations))</li> <li>CE – Low Voltage Directive 2006/95/EC (Europe)</li> <li>GB4943- CNCA Certification (China)</li> <li>GB 17625.1, GB/T 9254.1,</li> <li>FCC: EN 55035, EN 55032,</li> <li>47 CFR FCC part 15, ICES-003</li> </ul>
Hi-pot	2550 VDC

## 15 MECHANICAL

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Dimensions (W x H x L)			73.5 x 40.0 x 185		mm
			2.89 x 1.57 x 7.28		in
Weight			TBD		g



### 15.1 AIRFLOW DIRECTION

The normal airflow direction (NA) is from the card edge connector side to the AC inlet side of the power supply.  
The reverse airflow direction (RA) flows from the AC inlet side of the power supply to the card edge connector side.

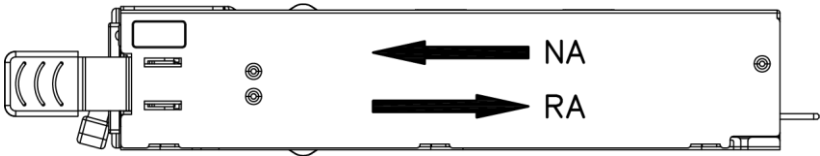


Figure 18. Airflow Direction

15.2 HANDLE RETENTION

The power supply has a handle to assist extraction. The module can be inserted and extracted without the assistance of tools. The power supply has a latch which retains the power supply into the system and prevents the power supply from being inserted or extracted from the system when the AC power cord is pulled into the power supply. The handle protects the operator from any burn hazard using the Customer Corporation Industrial designed plastic handle.

15.3 LED MARKING AND IDENTIFICATION

The power supply has a single bi-colored LED for indication of the power supply status Green & Amber. The below table showing the LED states for each power supply operating state.

POWER SUPPLY CONDITION	LED STATE
Output ON and OK	GREEN
No AC power to all power supplies	OFF
PSU standby state AC present / Only 12VSB on	1Hz Blink GREEN
Power supply is cold standby state or always standby state as defined in the Cold Redundancy section of the CRPS Common Requirements Specification	1Hz Blink GREEN
AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power.	AMBER
Power supply critical event causing a shutdown; failure, over current, short circuit, over voltage, fan failure, over temperature	AMBER
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blink Amber
Power supply FW updating	2Hz Blink GREEN



## 16 CONNECTORS

### 16.1 AC INLET CONNECTOR

The AC input connector is an IEC 320 C-20 power inlet. This inlet is rated for 16 A / 250 VAC.

### 16.2 DC OUTPUT CONNECTOR PIN LOCATIONS

The power supply has a card edge output that interfaces with 2\*25 card edge connector in the system.

The Matting connector at system side is OUPIIN (9393-F4P50N11AC30DA)

PIN-OUT	DEFINITION	PIN-OUT	DEFINITION
A1	GND	B1	NC
A2-8	GND	B2-8	GND
A9	NC	B9	NC
A10	+54V	B10	NC
A11-17	+54V	B11-17	+54V
A18	NC	B18	NC
A19	SDA	B19	A0
A20	SCL	B20	A1
A21	PS0N#	B21	12VSB
A22	SMBAlert#	B22	Cold Redundancy Bus
A23	Remote sense-	B23	+54VLS
A24	Remote sense+	B24	PRESENT#
A25	PWOK	B25	Vin_good

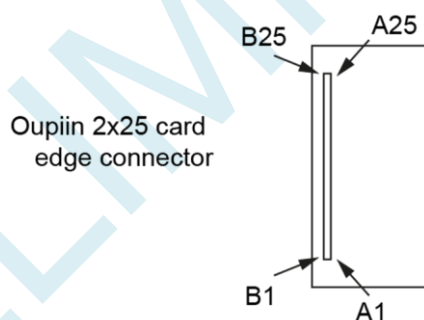


Figure 19. Back DC output golden finger port

For more information on these products consult: [tech.support@psbel.com](mailto:tech.support@psbel.com)

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