AX5V series

CLEARCLOCK™ OSCILLATOR FAMILY | LOW JITTER | 5.0X3.2MM XO

Description

Based on our PLL technology, the AX5V series is a programmable VCXO with LVPECL, LVDS, HCSL, and CML output logic options. Programmed at the factory prior to shipment, this series is perfect for quick turnaround solutions with a wide frequency range of up to 2100MHz. The AX5V series comes in a 5.0 x 3.2mm package with fixed VDD options from 1.8V, 2.5V and 3.3V, featuring a frequency pulling range of +/-150ppm minimum.

Features

- Available with any frequency from 15MHz to 2100MHz
- Supports LVPECL, HCSL, LVDS, CML
- Supports ±50ppm or ±100ppm all-inclusive stability
- Operating temperature ranges -40°C to 85°C, -20°C to 70°C or -40°C to 105°C.
- Industry standard 5.0 x 3.2mm footprint

Typical Applications

- Networking & communications
- 10G/40G/100G optical Ethernet
- RF systems, base stations (BTS)
- Datacenter
- PCI Express
- Test & measurement

Electrical Specifications

Parameters		Min.	Typ.	Max.	Units	Notes
Frequency Range	LVPECL	15		2100	MHz	Option “P”
	LVDS	15		2100		Option “D”
	HCSL	15		700		Option “H”
	CML	15		2100		Option “M”
Supply Voltage (Vdd) [Note 1]		2.97	3.3	3.63	V	Option “A”
		2.25	2.5	2.75		Option “B”
		1.71	1.8	1.89		Option “C”
Supply Current (Idd)	LVPECL		100	120	mA	@Vdd=3.3V
	LVDS		75	90		
	HCSL		80	100		
	CML		70	85		
Operating Temperature Range		-40		+85	°C	See Options
Storage Temperature		-55		+150	°C	
Frequency Stability over Operating Temperature Range		-25		+25	ppm	Options “D” or “F”
		-50		+50		Options “E”,”G” or “S”
First Year Aging [Note 2,3]		-3		+3	ppm	
All Inclusive Frequency Accuracy over 10 year product life [Note 2,4]		-50		+50	ppm	Specific to freq. stability options “D” or “F” (±25ppm)
		-100		+100		Specific to freq. stability options “E”,“G” and “S” (±50ppm)

Revision:
Initial Release 2/18/2026

Disclaimer

Check Inventory
Request Samples

Electrical Specifications *continued*

Parameters			Min.	Typ.	Max.	Units	Notes
Rise (Tr) / Fall (Tf) Time	LVPECL/LVDS/CML/HCSL				0.4	ns	20% ↔ 80% waveform
Duty Cycle			45		55	%	@ 50% Vdd
Start-up Time [Note 2]				< 5.0	10	ms	
Output High Voltage (VOH) Output Low Voltage (VOL)	LVPECL	V_{OH}	Vdd-1.165		Vdd-0.8	V	50Ω to Vdd–2.0V or Thevenin equivalent
		V_{OL}	Vdd-2.0		Vdd-1.55		
	LVDS	V_{OH}		1.4	1.6		100Ω between OUT and OUTN
		V_{OL}	0.9	1.1			
	HCSL	V_{OH}	0.66		1.15		50Ω into GND
		V_{OL}	0.0		0.15		
	CML	V_{OH}	Vdd-0.085		Vdd		50Ω to Vdd
		V_{OL}	Vdd-0.6		Vdd-0.32		
Output Enable & Disable Control (OE)		V_{IH}	0.8*(Vdd)			V	Output Enable; or No Connect
		V_{IL}			0.2*(Vdd)		Output Disable; High Impedance
Output Enable Time					2.5	ms	
Output Disable Time					10	µs	
Output Disable Current Consumption	LVPECL			99		mA	
	LVDS			74			
	HCSL			79			
	CML			69			
Control Voltage (Vc)			0.00	0.90	1.80	V	Vdd @ 1.8V
			0.25	1.25	2.25		Vdd @ 2.5V
			0.30	1.65	3.00		Vdd @ 3.3V
Frequency Pulling Range			±100			ppm	See Options
Linearity				1	10	%	
RMS Phase Jitter (12kHz -20MHz BW)[Note 5,6]							
251.0000MHz – 2100.0000MHz				130	200	fsec	@ Vdd=3.3V, BW:12kHz to 20MHz
126.0000MHz – 250.0000MHz				160	250		
41.0000MHz – 125.0000MHz				270	500		
15.0000MHz – 40.0000MHz				300	700		@ Vdd=3.3V, BW:12kHz to 5MHz

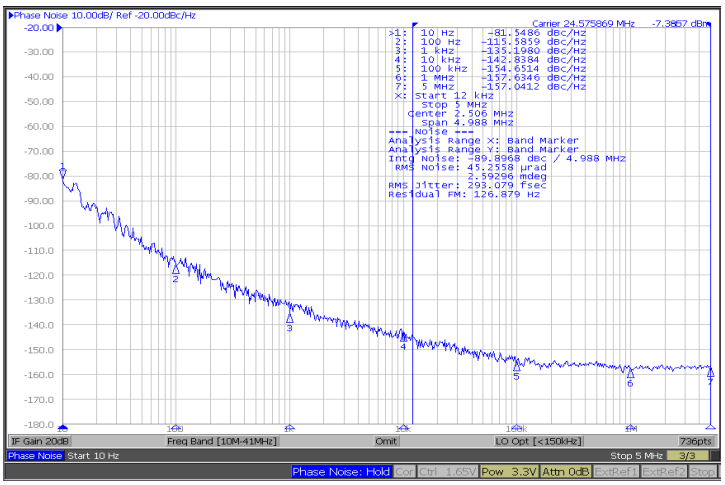
Note 1: Supply Voltage (Vdd) = 1.8V option not available with LVPECL output
Note 2: Relative to initial measured frequency @ +25°C
Note 3: Maximum Aging ±2 ppm (per year) after first year.
Note 4: Includes temperature stability, initial frequency accuracy @ 25°C ±3°C, load pulling, power supply variation, and 10 year aging frequency.
Note 5: Guaranteed by characterization.
Note 6: Phase jitter measured with Keysight E5052B Signal Source Analyzer not using a balun or buffer.

Phase Noise Test Setup

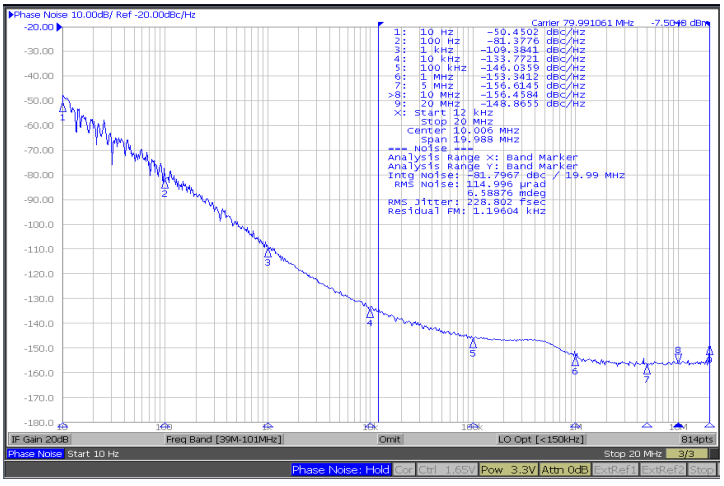
- Keysight E5052B Signal Source Analyzer
- Integration Bandwidth = 12kHz to 20MHz
- Spurious Activity (entire plot trace) = Omitted
- Specified Spur Omission Function = Enabled
- IF Gain = 20dB
- Correlation = 0
- Average = 3

Typical Phase Noise and Jitter Characteristics (@ 25ºC ± 3ºC)

F=24.5760MHz
Vdd=3.3V
RMS Phase Jitter = 293 fsec

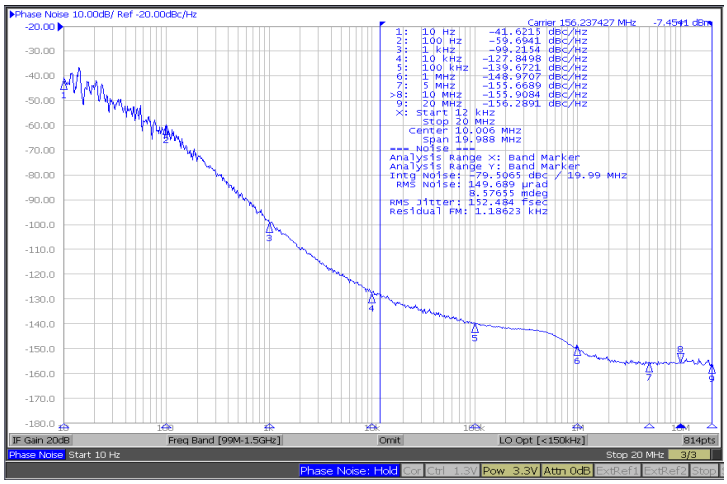


F=80.0000MHz
Vdd=3.3V
RMS Phase Jitter = 229 fsec

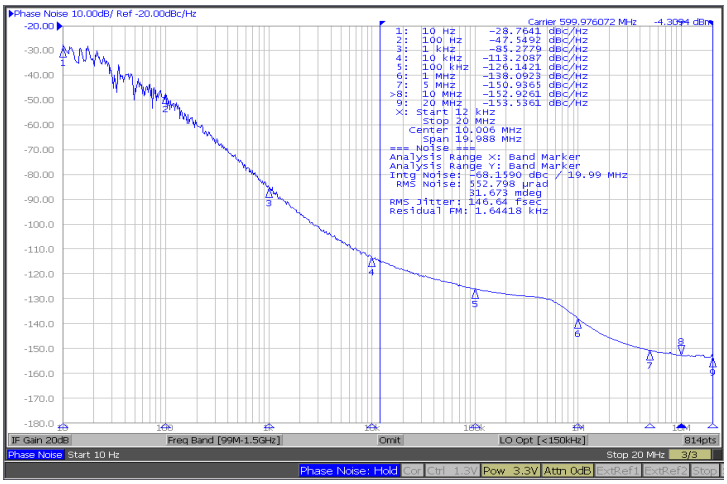


Typical Phase Noise and Jitter Characteristics Cont. (@ 25ºC ± 3ºC)

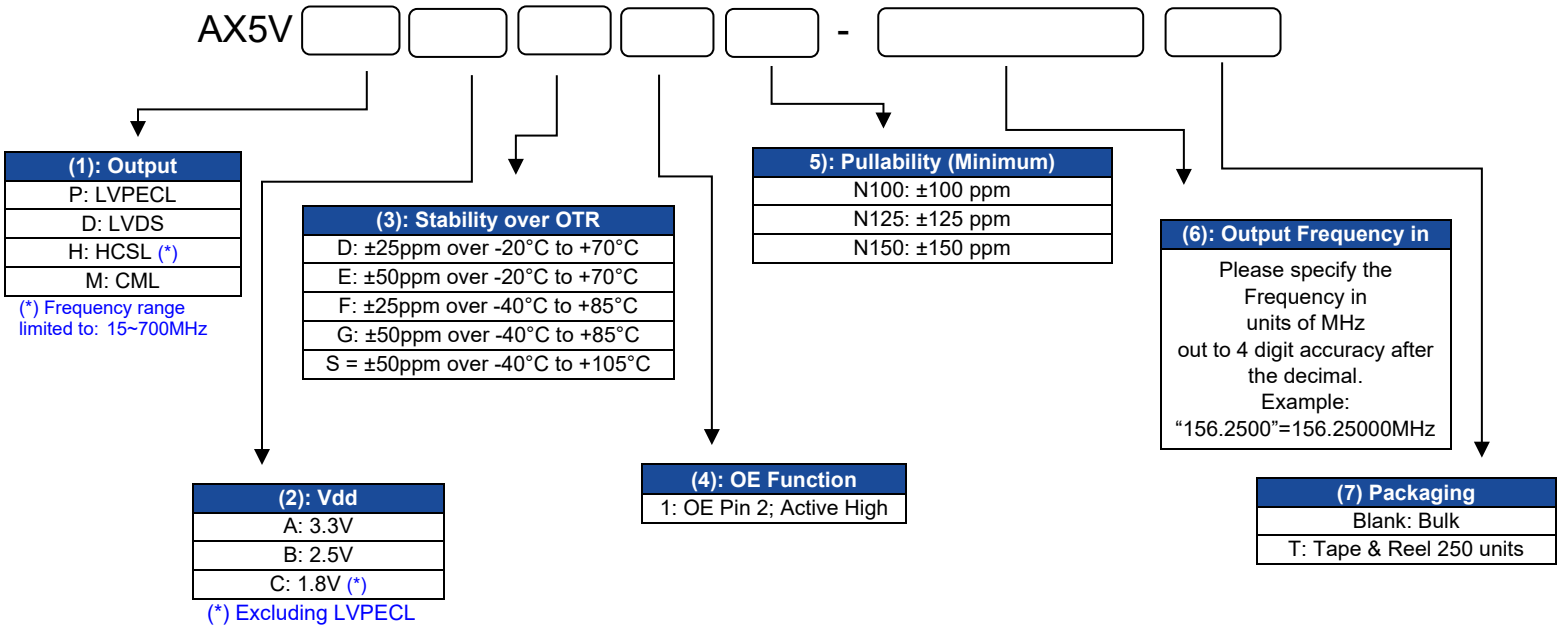
F=156.2500MHz
Vdd=3.3V
RMS Phase Jitter = 153 fsec



F=600.0000MHz
Vdd=3.3V
RMS Phase Jitter = 147 fsec



Option and Part Identification [Note 7]



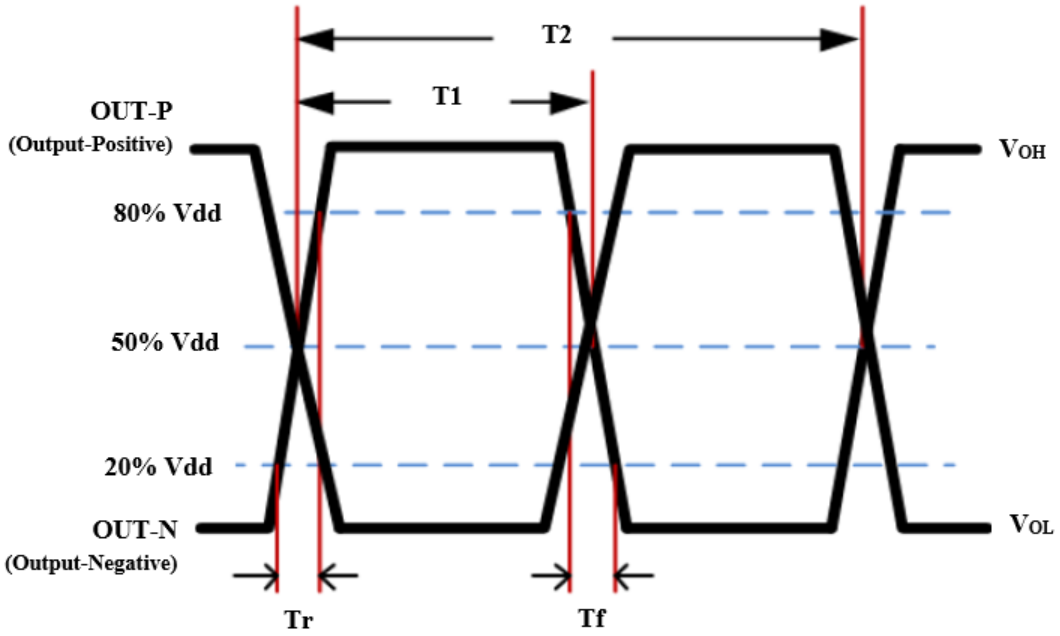
Part Number Example:

AX5VPAF1N100-644.53125T

Note 7: Contact Abracon for non-standard part number configurations and/or requests with carrier frequency callouts up to 5 & 6 digit accuracy after the decimal.

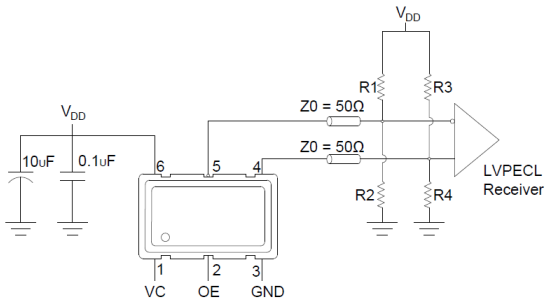
Differential Output Waveform

$$\text{Duty Cyle} = \left(\frac{T1}{T2}\right) * 100\% \text{ (measured at 50\% Vdd)}$$



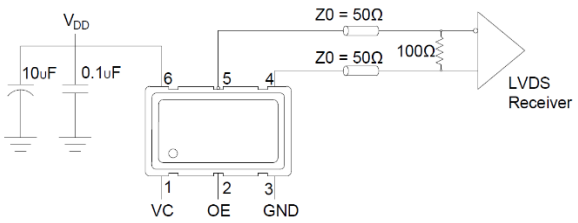
Recommended Test Circuit

LVPECL

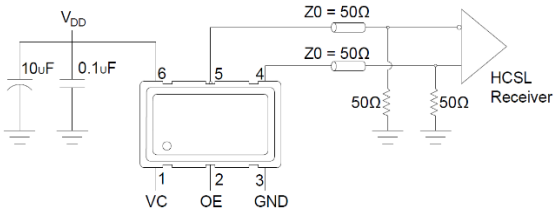


Vdd = 3.3V ; R1=R3=127Ω; R2=R4=82.5Ω
Vdd = 2.5V; R1=R3=250Ω; R2=R4=62.5Ω

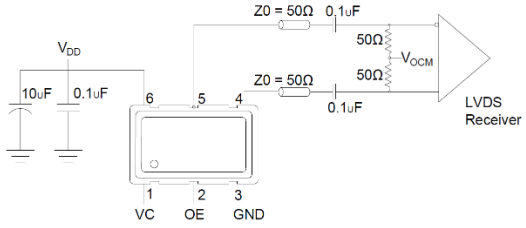
LVDS @ Vdd = 3.3V & 2.5V



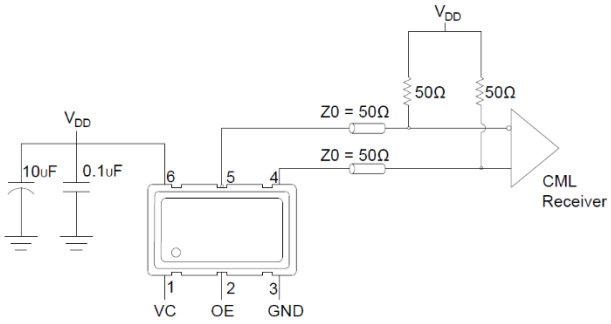
HCSL



LVDS @ Vdd = 1.8V*



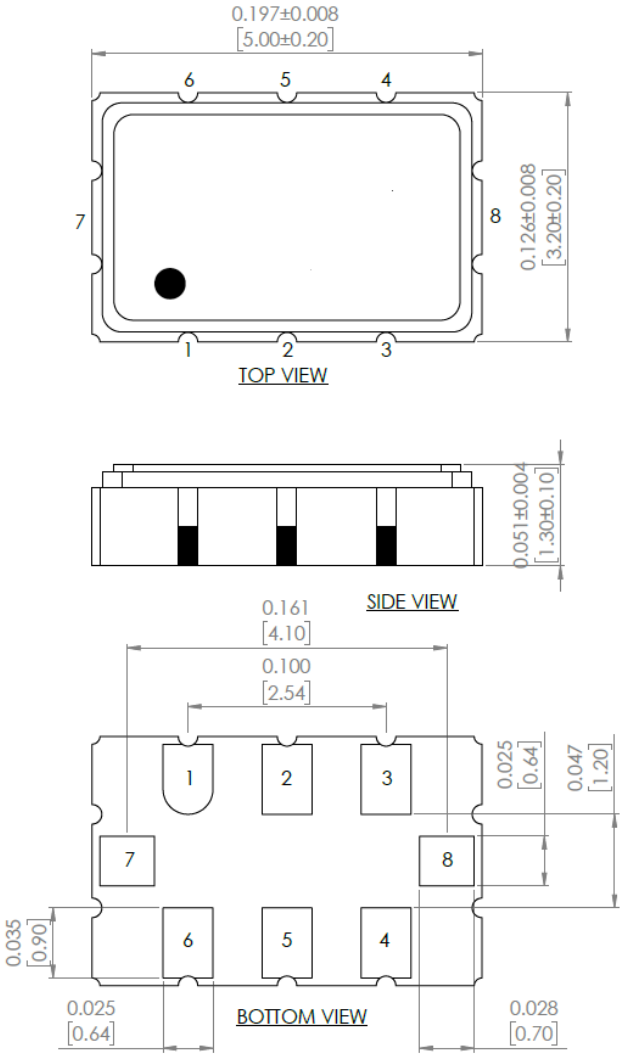
CML

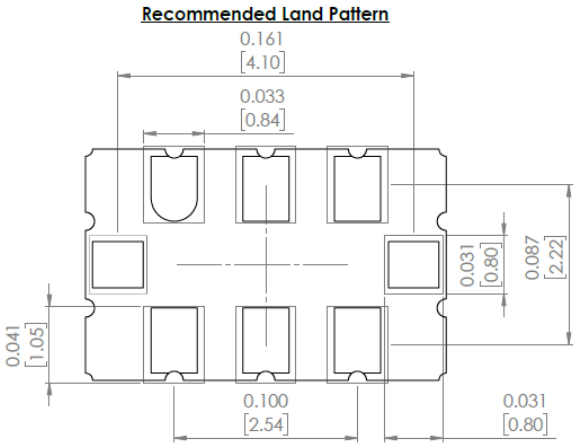


*The output common mode voltage V_{OCM}, is required to be supplied externally, where V_{OCM} = 1.3V.

AC coupling needs to be implemented between the clock device (oscillator) and the receiver circuit.

Mechanical Dimensions





Pin #	Function
1	Voltage Control
2	Output Enable/Disable
3	GND
4	Output
5	Complementary output
6	Supply Voltage (Vdd)
7	Do not connect
8	Do not connect

Dimensions: inches (mm)

Absolute Maximum Ratings[Note 8]

Parameters	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	Vss-0.5		4.5	V	
Input Voltage	Vss-0.5		V_{DD}+0.5	V	
Output Voltage	Vss-0.5		V_{DD}+0.5	V	
Maximum Junction Operating Temperature			150	ºC	
Ambient Operating Temperature Range	-40		85	ºC	Industrial
Ambient Operating Temperature Range	-40		105	ºC	Extended Industrial
Reflow Temperature			260	°C	See Reflow Profile
ESD Protection	4kV HBM, 300V MM, 2kV CDM				

Note 8: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability. The data sheet limits are not guaranteed if the device is operated beyond the recommended operating conditions.

Reflow Profile [JEDEC J-STD-020]

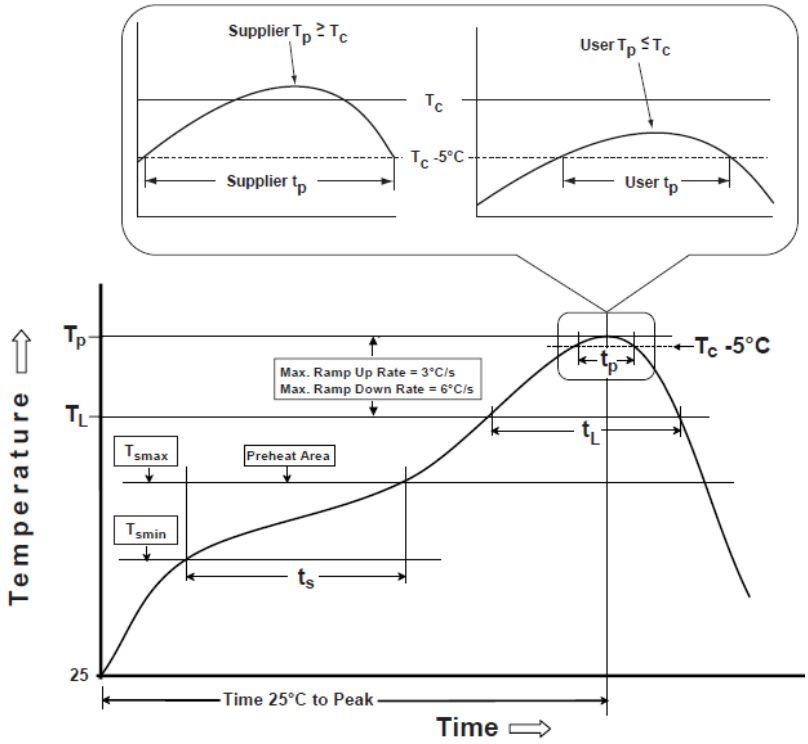


Table 1

SnPb Eutectic Process Classification Temperatures (T_c)		
Package Thickness	**Volume mm³ <350**	**Volume mm³ ≥350**
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2

Pb-Free Process Classification Temperatures (T_c)			
Package Thickness	**Volume mm³ <350**	**Volume mm³ 350-2000**	**Volume mm³ >2000**
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

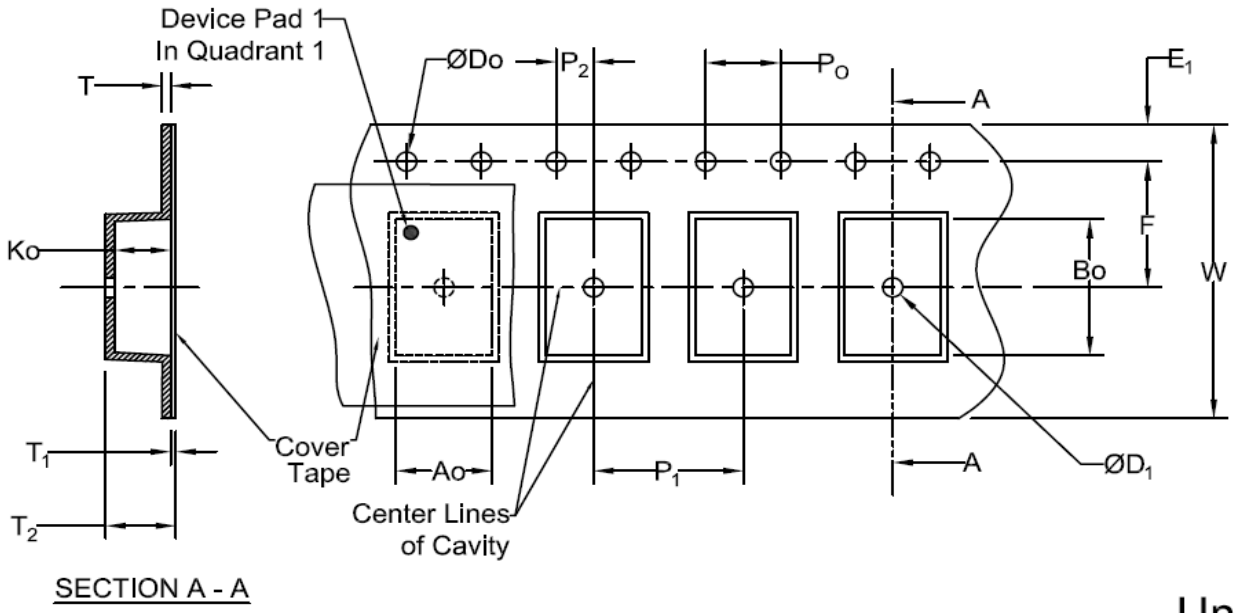
Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat / soak		
Temperature minimum (T_{smin})	100°C	150°C
Temperature maximum (T_{smax})	150°C	200°C
Time (T_{smin} to T_{smax}) (t_s)	60 - 120 sec.	60 - 120 sec.
Average ramp-up rate (T_{smax} to T_P)	3°C/sec. max	3°C/sec. max
Liquidous temperature (T_L)	183°C	217°C
Time at liquidous (t_L)	60 - 150 sec.	60 - 150 sec.
Peak package body temperature (T_P)*	**see Table 1**	**see Table 2**
Time (t_p)** within 5°C of the specified classification temperature (T_C)	20 sec.	30 sec.
Ramp-down rate (T_p to T_{smax})	6°C/sec. max	6°C/sec. max
Time 25°C to peak temperature	6 min. max	8 min. max
Reflow cycles	2 max	2 max

*Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.

**Tolerance for time at peak profile temperature (t_p) is defined as supplier minimum and a user maximum.

Packaging

Blank = Bulk
T = Tape & Reel 250 units/reel



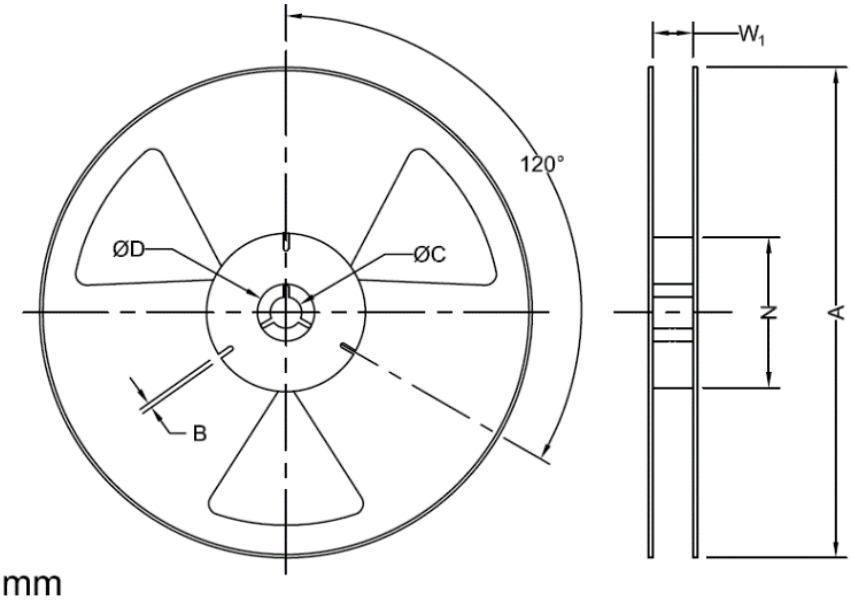
Unit: mm

Tape Specifications (mm)							
Width	Ao	Bo	Do	D_1 (Min)	E_1	F	Ko
12mm	*	*	1.5+0.1/-0.0	1.0	1.75±0.1	5.5±0.05	*

Tape Specifications (mm)							
Width	P_1	P_2	P_0	T (Max)	T_1 (Max)	T_2 (Max)	W (Max)
12mm	8.0±0.1	2.0±0.05	4.0±0.1	0.6	0.1	6.5	12.3

***Note: Compliant to EIA-481**

Dimensions: inches (mm)



Unit: mm

Tape Specifications (mm)							
Width	Qty/Reel	A (Nom)	B (Min)	C (Min)	D (Min)	N (Min)	*W_1
12mm	250	178	1.5	13.0+0.5/-0.2	20.2	50	12.4+2.0/-0.0

***Note: Measured at Hub**

Dimensions: inches (mm)