AK1B

ClearClock™ Oscillator Family | Clock Oscillator| 2.0x1.6mm XO

Description

Abracon's AK1B offers the latest high frequency fundamental crystal technology, with exceptional phase noise performance, with a noise floor of -166 dBc/Hz at 156.250MHz. The Abracon AK1B is available with a compact 2.0 x 1.6 x 0.75 mm package with a frequency stability of ±50 ppm over an operating temperature range of -40ºC to 105ºC. Additional advantages include a various power supply options ranging from 1.8V, 2.5V, 3.3V and a continuous voltage range of 2.375V to 3.63V.

Features

- Available in industry standard frequencies: 100MHz and 156.25MHz
- ±50ppm stability over industrial operating temperature (-40ºC to +105ºC)
- 1.8V, 2.5V, 3.3V, 2.375 V to 3.63V Continuous supply voltage options
- Industry standard 2.0 x 1.6 x 0.75 mm footprint
- Available in Abracon's global distribution network

Typical Applications

- Optical Transceivers and Modules
- Data Centers, Storage, and Servers
- Networking switches and gateways
- 100G/200G/400G/800G Ethernet
- Fibre Channel/SONET/SDH/PCIe
- Industrial and FPGA applications
- Test & measurement

Electrical Specifications

Parameters		Min.	Typ.	Max.	Unit	Notes
Frequency Range		100		156.25	MHz	
Standard Available Frequencies		100.000, 156.250			MHz	Contact Abracon for availability of frequencies not listed
Supply Voltage (V_{DD})		2.97	3.3	3.63	V	Option "A"
		2.375	2.5	2.625		Option "B"
		1.71	1.8	1.89		Option "C"
		2.375		3.63		Option "D"
Supply Current (I_{DD})	LVPECL			60	mA	At 156.2500MHz, 3.3V
	LVDS			20		
	HCSL			40		
Operating Temperature Range		-40		85	°C	Option "R"
		-40		105		Option "S"
Storage Temperature		-55		150	°C	
First Year Aging		-3		3	ppm	At 25°C
Frequency Stability [Note 1]		-50		50	ppm	Option "R" (-40°C to +85°C)
		-50		50		Option "S" (-40°C to +105°C)

Electrical Specifications Cont.

Parameters			Min.	Typ.	Max.	Unit	Notes
Rise (Tr) / Fall (Tf) Time[Note 3]	LVPECL				0.5	ns	R_L=50Ω to V_{dd}–2.0V on each output
	LVDS				0.5		R_L= 100Ω (Between Outputs)
	HCSL				0.6		R_L= 50Ω to GND, RS=0Ω on each output
Duty Cycle			45		55	%	
Start-up Time [Note 2]					2.0	ms	
Output High Voltage (VOH) Output Low Voltage (VOL)	LVPECL	V_{OH}	V_{DD}-1.105	V_{DD}-0.950	V_{DD}-0.860	V	R_L=50Ω into V_{dd}–2.0V on each output, Option "P"
		V_{OL}	V_{DD}-1.810	V_{DD}-1.700	V_{DD}-1.590		
	HCSL	V_{OH}	0.50		1.0		R_L= 50Ω to GND, RS=0Ω, Option "H" on each output
		V_{OL}	-0.150		0.150		
Output Voltage	LVDS	V_{OD}	247	350	454	mV	R_L= 100Ω (Between Outputs), Option "D".
		ΔV_{OD}			50	mV	
Offset Voltage		V_{OS}	1.125	1.250	1.375	V	
		ΔV_{OS}			50	mV	
Differential Output Voltage Swing (Vopp)		LVPECL	0.80			V	OUT-OUTN
		LVDS	0.50		0.90		
		HCSL	1.10		2.20		
Tri-state Function		V_{IH}	"1" (V_{IH}≥0.7*Vdd) or Open: Oscillation; "0" (V_{IL}<0.3*Vdd): No Oscillation/Hi Z			V	
		V_{IL}					
Output Enable Time					2.0	ms	
Output Disable Time					0.2	µs	
Output Disable Current Consumption					10	µA	OE (pad 1) ≤ 0.3*(V_{dd})
RMS Phase Jitter (12kHz to 20MHz from Carrier)			See Table 1 below				Vdd, output logic type and Carrier frequency dependent

Note 1: Includes post reflow frequency tolerance, temperature stability, load pulling, power supply variation and first year aging
Note 2: Relative to initial measured frequency @ +25°C
Note 3: Measured over 20% to 80% of waveform

Phase Noise Specifications

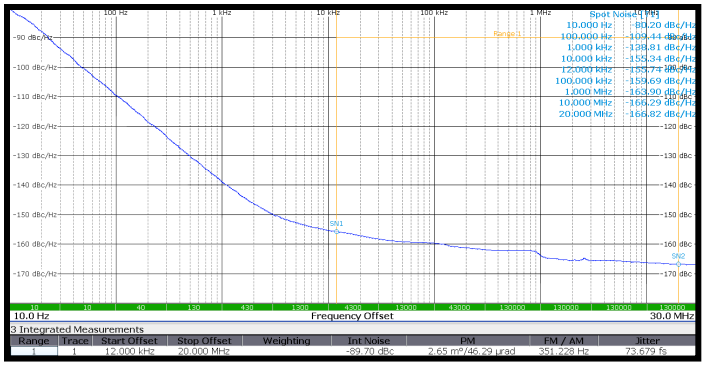
Table 1
RMS Phase Jitter 12kHz – 20MHz BW[Note 4,5]

Carrier Frequency	Output Logic	Supply Voltage (1.8V)		Supply Voltage (2.5V)		Supply Voltage (3.3V)	
		RMS Jitter		RMS Jitter		RMS Jitter	
		Typ. (fs)	Max (fs)	Typ. (fs)	Max (fs)	Typ. (fs)	Max (fs)
100	LVDS	79.3	100	73.7	85	73.7	80
	LVPECL	NA	NA	75.9	85	75.9	85
	HCSL	68.6	80	54.4	80	54.4	80
156.25	LVDS	53.4	80	34.5	50	34.5	50
	LVPECL	NA	NA	41.8	60	41.8	50
	HCSL	47.2	60	34.2	50	34.2	50

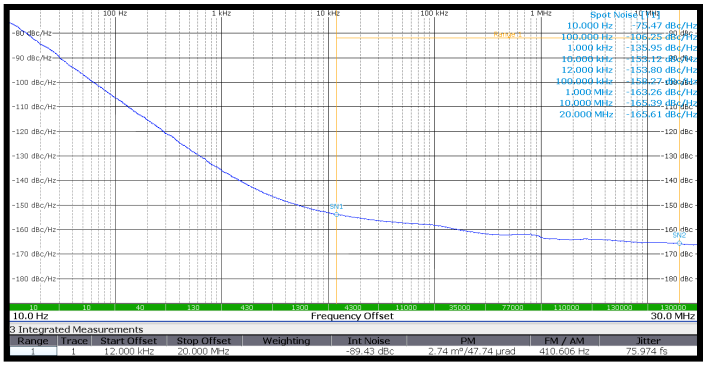
Note 4: Guaranteed by characterization; RMS Phase Jitter specifications are inclusive of any spurs
Note 5: Phase jitter measured with Rohde & Schwarz FSWP8

Phase Noise Plots [Note 5]

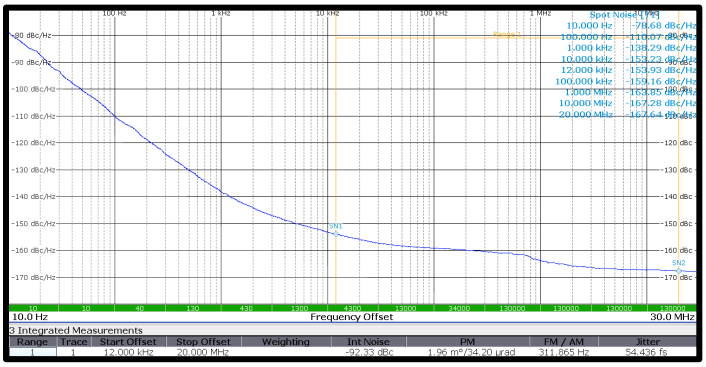
Plot #1: LVDS, 3.3V, 100MHz



Plot #2: LVPECL, 3.3V, 100MHz

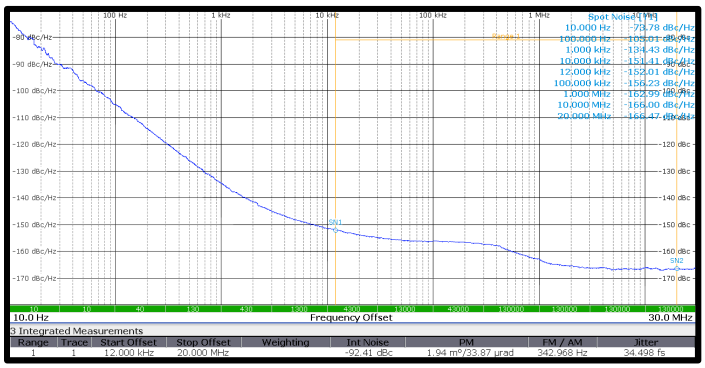


Plot #3: HCSL, 3.3V, 100MHz

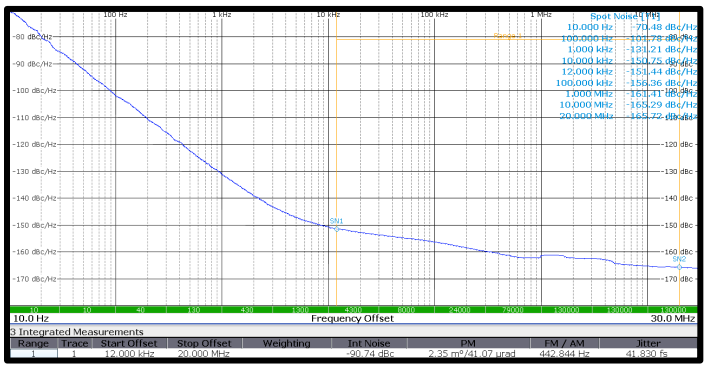


Phase Noise Plots Cont. [Note 5]

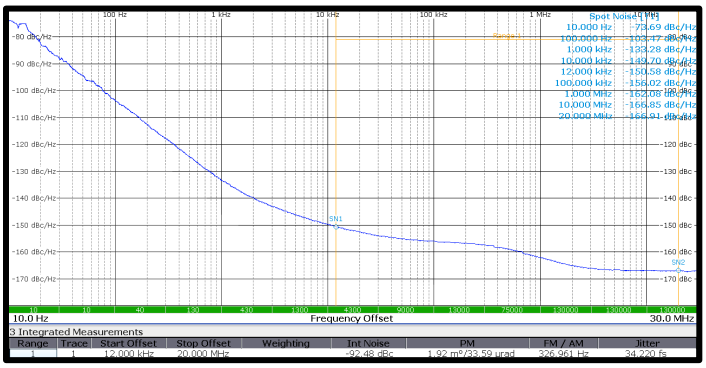
Plot #3: LVDS, 3.3V, 156.25MHz



Plot #5: LVPECL, 3.3V, 156.25MHz



Plot #6: HCSL, 3.3V, 156.25MHz



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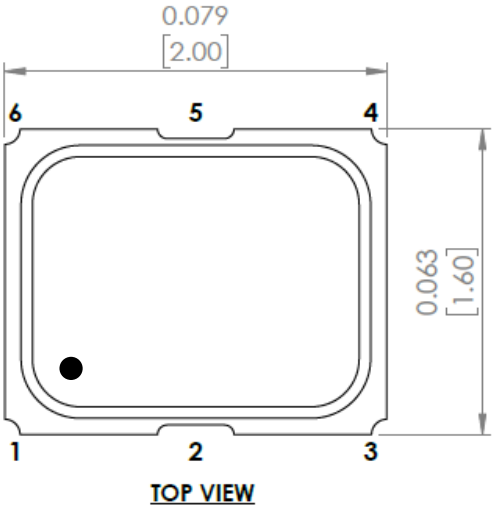
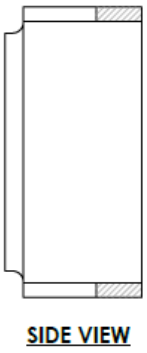
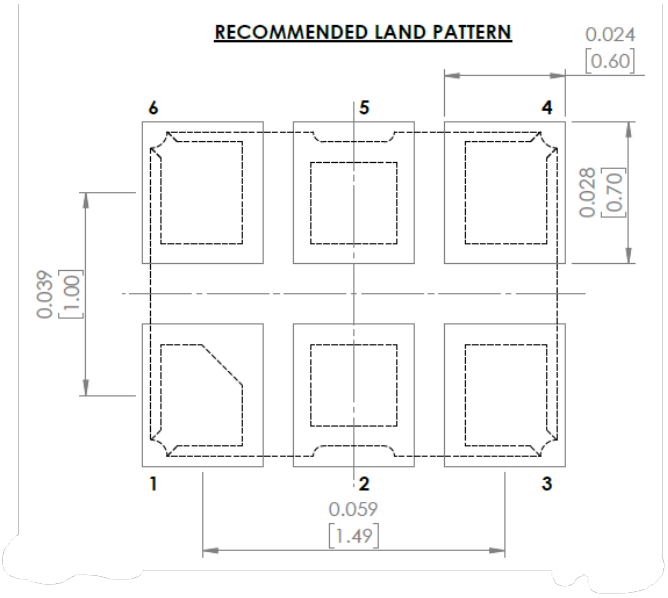
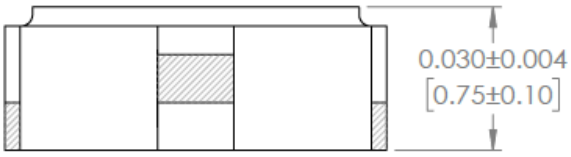
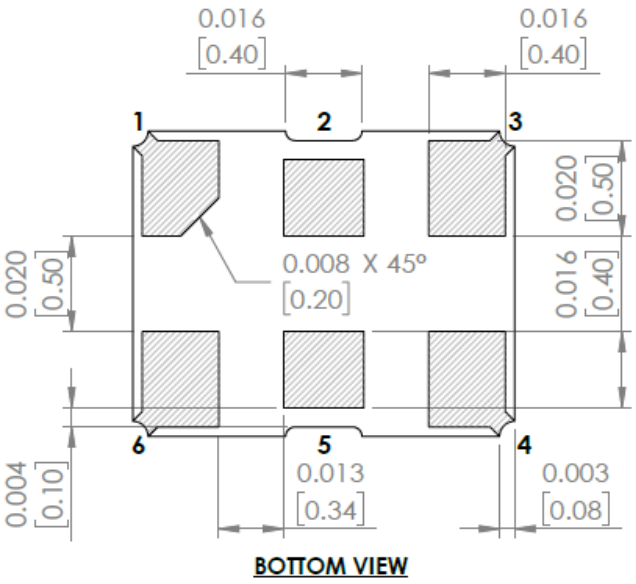
Mechanical Dimensions











Case 1 Pin #1=Output Enable/Disable Function *where* OE is Active HIGH	
Pin	**Description**
# 1	Output Enable = Logic High, "1", Vdd, or NC
	Output Disable = Logic Low, "0", GND
# 2	No Connect
# 3	GND
# 4	Output
# 5	Complementary output
# 6	Supply Voltage (Vdd)

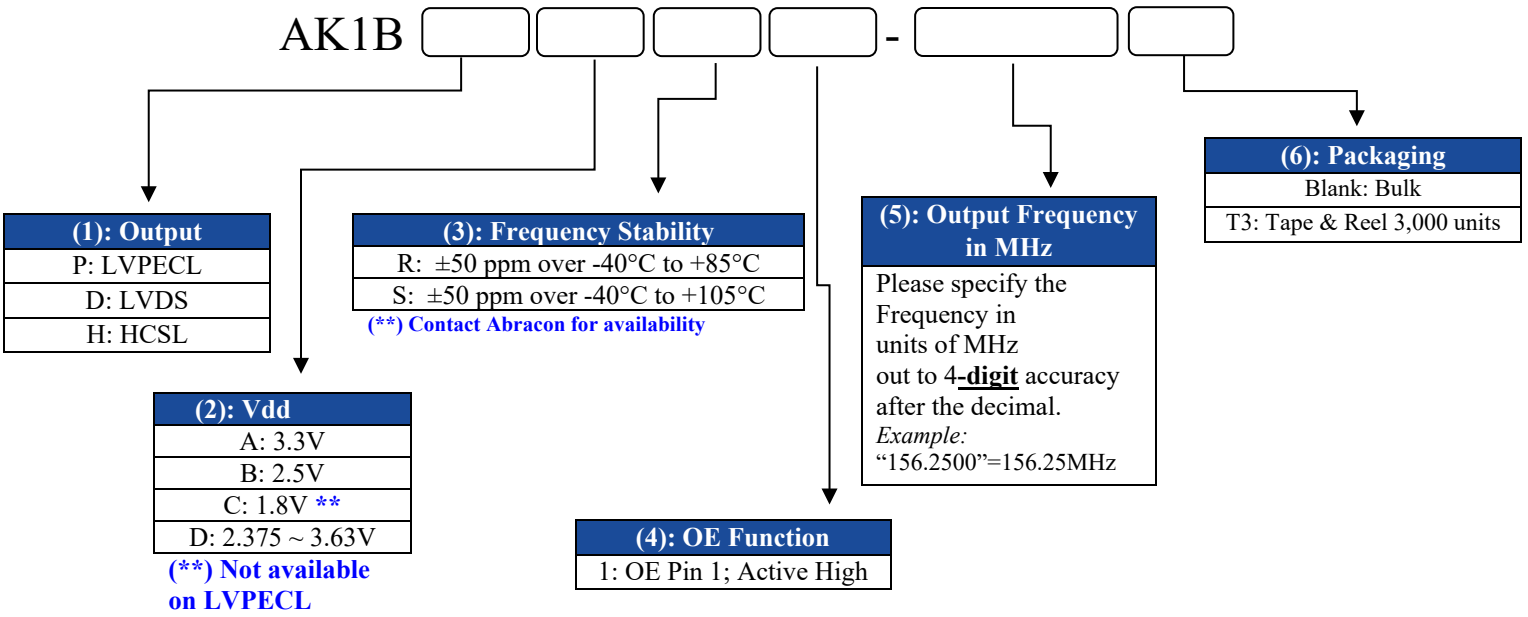
Dimensions: Inches [mm]

Revision: IR
Initial Release 6/13/2025

Disclaimer

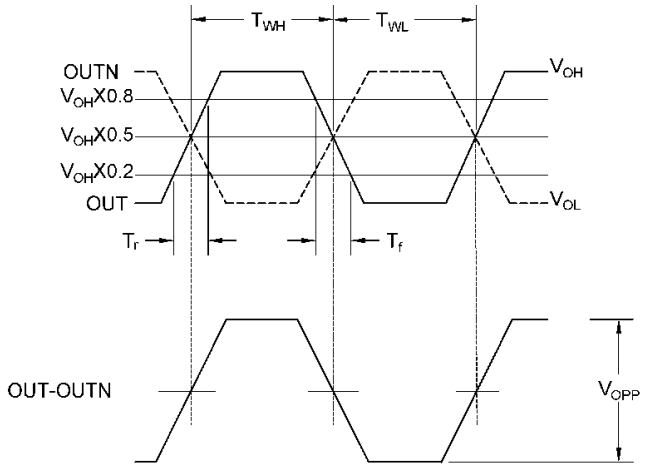
Check Inventory
Request Samples

Part Identification



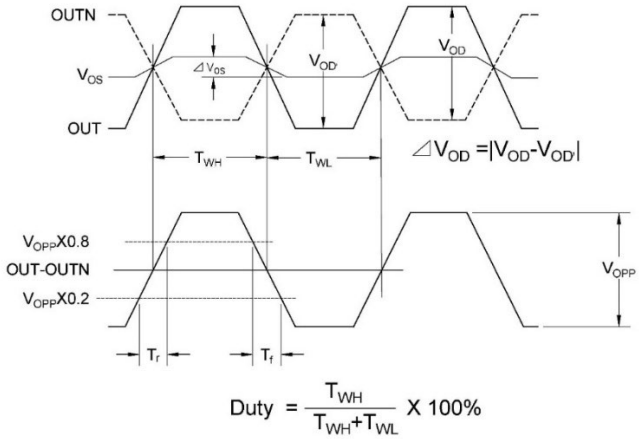
Output Waveform Diagram

LVPECL: Output Wave Form (Duty, Tr, Tf, V_{OH}, V_{OL}, Vopp)



$$\text{Duty Cycle} = \frac{T_{WH}}{T_{WH}+T_{WL}} \text{ X } 100\%$$

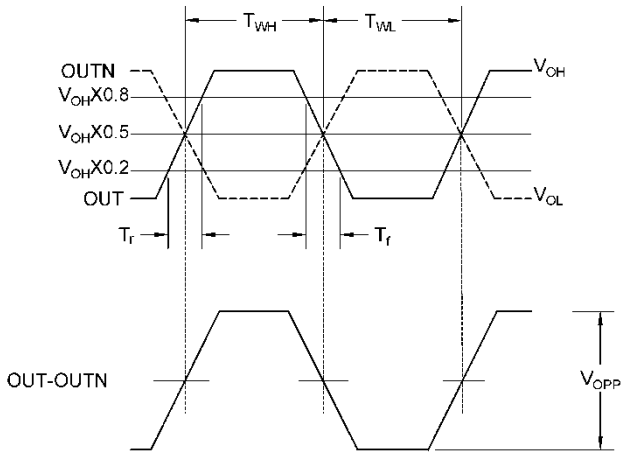
LVDS: Output Wave Form (Duty, Tr, Tf, V_{OD}, ΔV_{OD}, V_{OS}, ΔV_{OS}, Vopp)



$$\text{Duty} = \frac{T_{WH}}{T_{WH}+T_{WL}} \text{ X } 100\%$$

Output Waveform Diagram Cont.

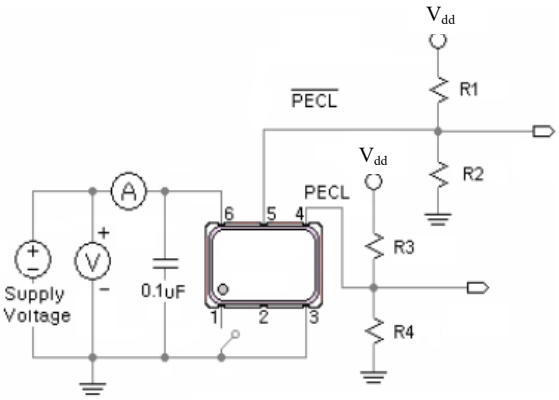
HCSL: Output Wave Form (Duty, Tr, Tf, V_{OH}, V_{OL}, Vopp)



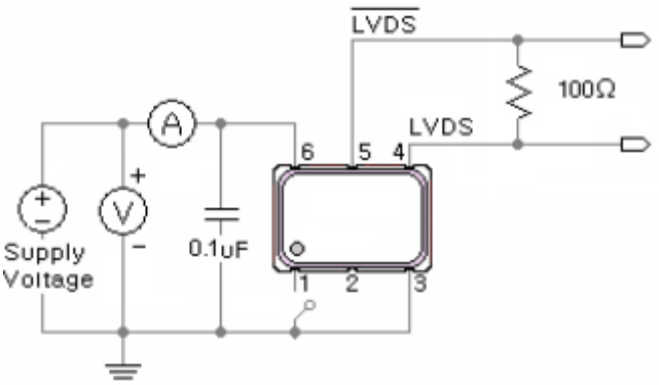
$$\text{Duty Cycle} = \frac{T_{WH}}{T_{WH}+T_{WL}} \text{ X } 100\%$$

Recommended Test Circuit [Note 6]

LVPECL

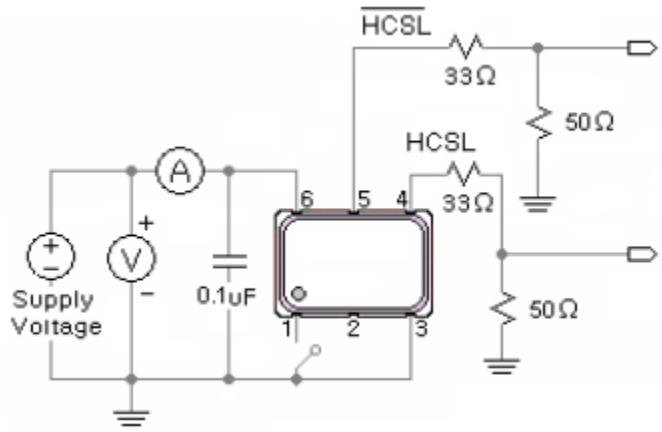


LVDS



Vdd=3.3V: R1=R3=127Ω; R2=R4=82.5 Ω
Vdd=2.5V: R1=R3=250Ω; R2=R4=62.5 Ω

HCSL



Note 6: Recommended test circuit images are representative of when the OE Function is located on Pin 1; when the OE Function is located on Pin 2, then Pin 1=No Connect & Pin 2=OE or No Connect.

Absolute Maximum Ratings [Note 7]

Parameters	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	Vss-0.5		4.5	V	
Input Voltage	Vss-0.5		V_{DD}+0.5	V	
Output Voltage	Vss-0.5		V_{DD}+0.5	V	
Maximum Junction Operating Temperature			150	ºC	
Ambient Operating Temperature Range	-40		85	ºC	Industrial
Ambient Operating Temperature Range	-40		105	ºC	Extended Industrial
Reflow Temperature			260	°C	See Reflow Profile
ESD Protection	4kV HBM, 300V MM, 2kV CDM				

Note 7: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability. The data sheet limits are not guaranteed if the device is operated beyond the recommended operating conditions.

Reflow Profile [JEDEC J-STD-020]

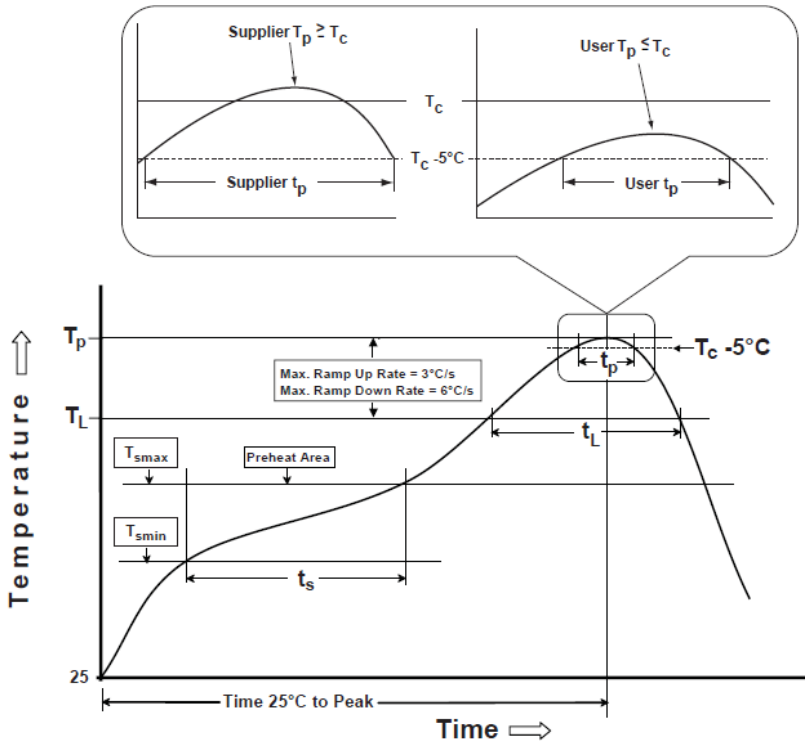


Table 1

SnPb Eutectic Process Classification Temperatures (T_c)		
Package Thickness	**Volume mm³ <350**	**Volume mm³ ≥350**
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2

Pb-Free Process Classification Temperatures (T_c)			
Package Thickness	**Volume mm³ <350**	**Volume mm³ 350-2000**	**Volume mm³ >2000**
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

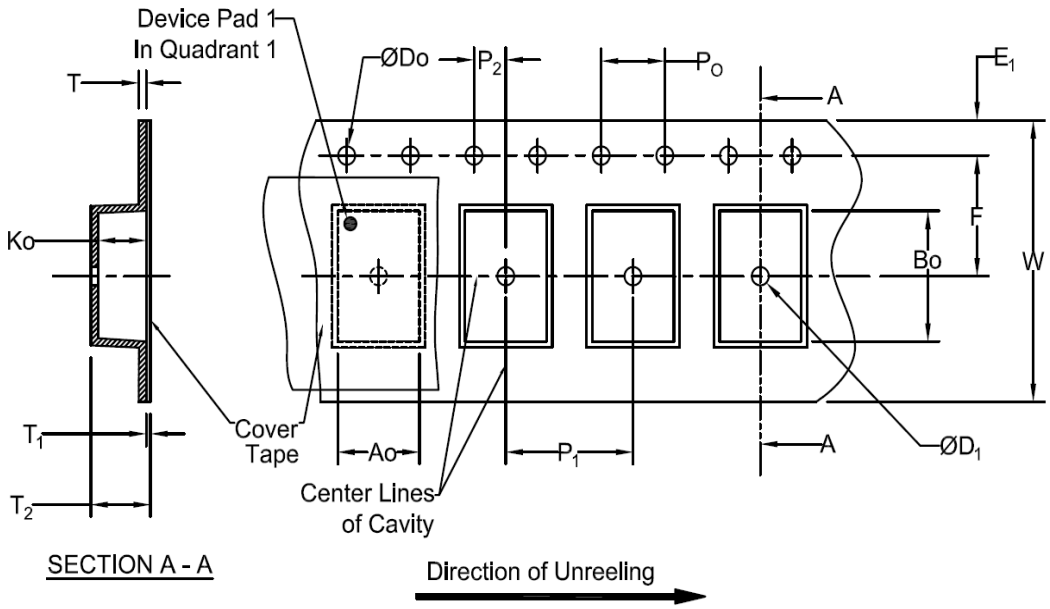
Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat / soak		
Temperature minimum (T_{smin})	100°C	150°C
Temperature maximum (T_{smax})	150°C	200°C
Time (T_{smin} to T_{smax}) (t_s)	60 - 120 sec.	60 - 120 sec.
Average ramp-up rate (T_{smax} to T_P)	3°C/sec. max	3°C/sec. max
Liquidous temperature (T_L)	183°C	217°C
Time at liquidous (t_L)	60 - 150 sec.	60 - 150 sec.
Peak package body temperature (T_P)*	**see Table 1**	**see Table 2**
Time (t_p)** within 5°C of the specified classification temperature (T_C)	20 sec.	30 sec.
Ramp-down rate (T_p to T_{smax})	6°C/sec. max	6°C/sec. max
Time 25°C to peak temperature	6 min. max	8 min. max
Reflow cycles	2 max	2 max

*Tolerance: perature (T_P) is defined as a supplier minimum and a user maximum.

**Tolerance: ofile temperature (t_p) is defined as supplier minimum and a user maximum.

Packaging

T3: 3,000pcs/reel

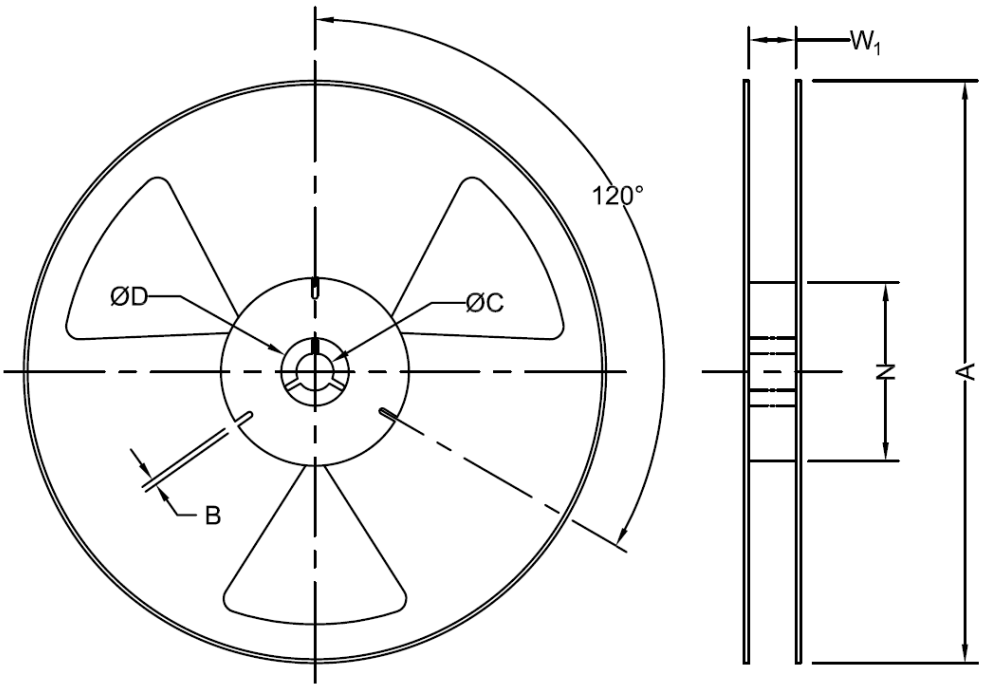


Tape Specifications (mm)							
Width	Ao	Bo	Do	D_1 (Min)	E_1	F	Ko
8mm	*	*	1.5+0.1/-0.0	1.0	1.75±0.1	3.5±0.05	*
Width	P_1	P_2	P_0	T (Max)	T_1 (Max)	T_2 (Max)	W (Max)
8mm	4.0±0.1	2.0±0.05	4.0±0.1	0.6	0.1	2.5	8.3

***Note: Compliant to EIA-481**

Dimensions: mm

Packaging Cont.



Reel Specifications (mm)							
Width	Qty/Reel	A (Nom)	B (Min)	C (Min)	D (Min)	N (Min)	*W_1
8mm	3000	178	1.5	13.0+0.5/-0.2	20.2	50	8.4+1.5/-0.0

***Note: Measured at Hub**

Dimensions: mm