Description

The AP53781 is a highly integrated USB Type-C® PD3.2 Dual-Role Power (DRP) controller to support Extended Power Range (EPR)/ Adjustable Voltage Supply (AVS) up to 28V and Standard Power Range (SPR) up to 21V.

The AP53781 can act as a power consumer by requesting power from a PD3.1 compliant adaptor and can also act as a power provider to supply a Type-C connector-equipped device (TCD). The AP53781 could consume as low as 50μA during the power-down mode.

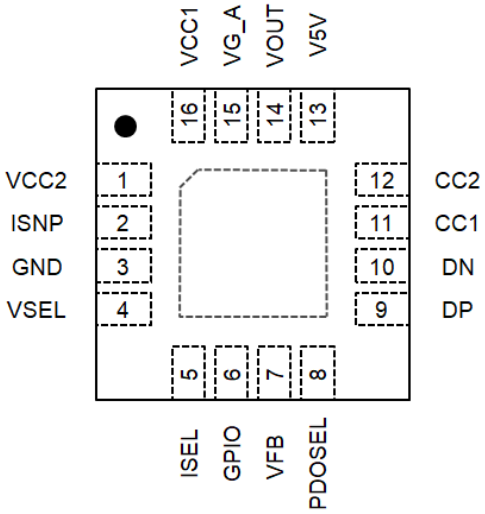
The AP53781 is operating in a system without an MCU. To be a power consumer, its desired Request Data Object (RDO) can be selected by the correspondence resistance values on the VSEL and ISEL pins for target voltage and current, respectively. To be a power provider, its Power Data Object (PDO) capability can be selected from a pre-determined 8 power profiles by a suitable resistance on the PDOSEL pin.

Meanwhile, the AP53781 integrates Rp/Rd termination resistors and switches for DRP control. It has QC2.0/3.0 functions and dead-battery mode during the sink role. Also, the VFB feedback control for external DC/DC controller is provided during the source role. The AP53781 operates from 3.6V up to 28V with low-side current sense topology.

The AP53781 offers short protection between Configuration Channel (CC1/CC2) pins to adjacent high-voltage pin up to 34V. The built-in firmware of the AP53781 offers comprehensive safety protection schemes, including overvoltage protection (OVP), undervoltage protection (UVP), and overcurrent protection (OCP).

Pin Assignments

(Top View)



W-QFN3030-16 (Type A1)

Features

- USB PD3.1 v1.8 Certified with TID: 11689
- Support Autonomous DRP Control
- Support EPR/AVS up to 28V with 100mV/Step
- Support SPR up to 21V
- Power-Down Consumption as Low as 50μA
- Source PDO Capability Selected Through External Resistor Setting
- Sink RDO Voltage/Current Selected Through External Resistors Settings
- Support QC2.0/3.0 Either for Sink or Source Role
- Support Gate Drivers for nMOS VBUS Power Switch
- Support Analog VFB Feedback for External DC/DC
- Operating Voltage 3.6V to 28V with Low-Side Current Sense
- Support VBUS and VOUT Discharge Paths
- Support Dead-Battery Mode
- Support OVP/UVP/OCP with Auto Restart
- VBUS Short Protection on CC1/CC2 Pins up to 34V
- VBUS Short Protection on DP/DN Pins up to 24V
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

- Power banks
- Power tools
- Wireless speakers
- E-bikes
- POS terminals
- Portable displays

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

The AP53781 is a highly integrated USB PD3.1 DRP controller suitable for operating in a system without MCU, as shown in Figure 1 below. After the power-on initialization, it alternates periodically the Type-C CC1/CC2 (CCx) pin connections between the pullup resistance Rp and pulldown resistance Rd to decide which role to act.

When AP53781 acts as a power consumer role, the desired RDO can be selected by the correspondence resistance values on the VSEL and ISEL pins for voltage and current, respectively. When it acts as a power source role, the PDO capability can be selected from a pre-determined 8 power profiles by a suitable resistance on the PDOSEL pin. And there is a current DAC embedded to support VFB feedback for external DC/DC controller during the source role.

Other than the USB PD3.1 profiles, the QC2.0/3.0 functions are also supported both in source and sink modes. In addition, the dead-battery mode is supported in case the AP53781 chip power is not available from local system.

The AP53781 provides OVP/UVP/OCP power protections for both the Provider and Consumer paths, where a 5mΩ low-side current sense topology is used for OCP. The discharge paths for VOUT and VBUS are provided to expedite the voltage recovery time of the power bus.

The AP53781 provides a high-voltage output pin to control the VBUS on and off by driving an external nMOS switch. It can be used to control the power bus connection between the internal system and outside.

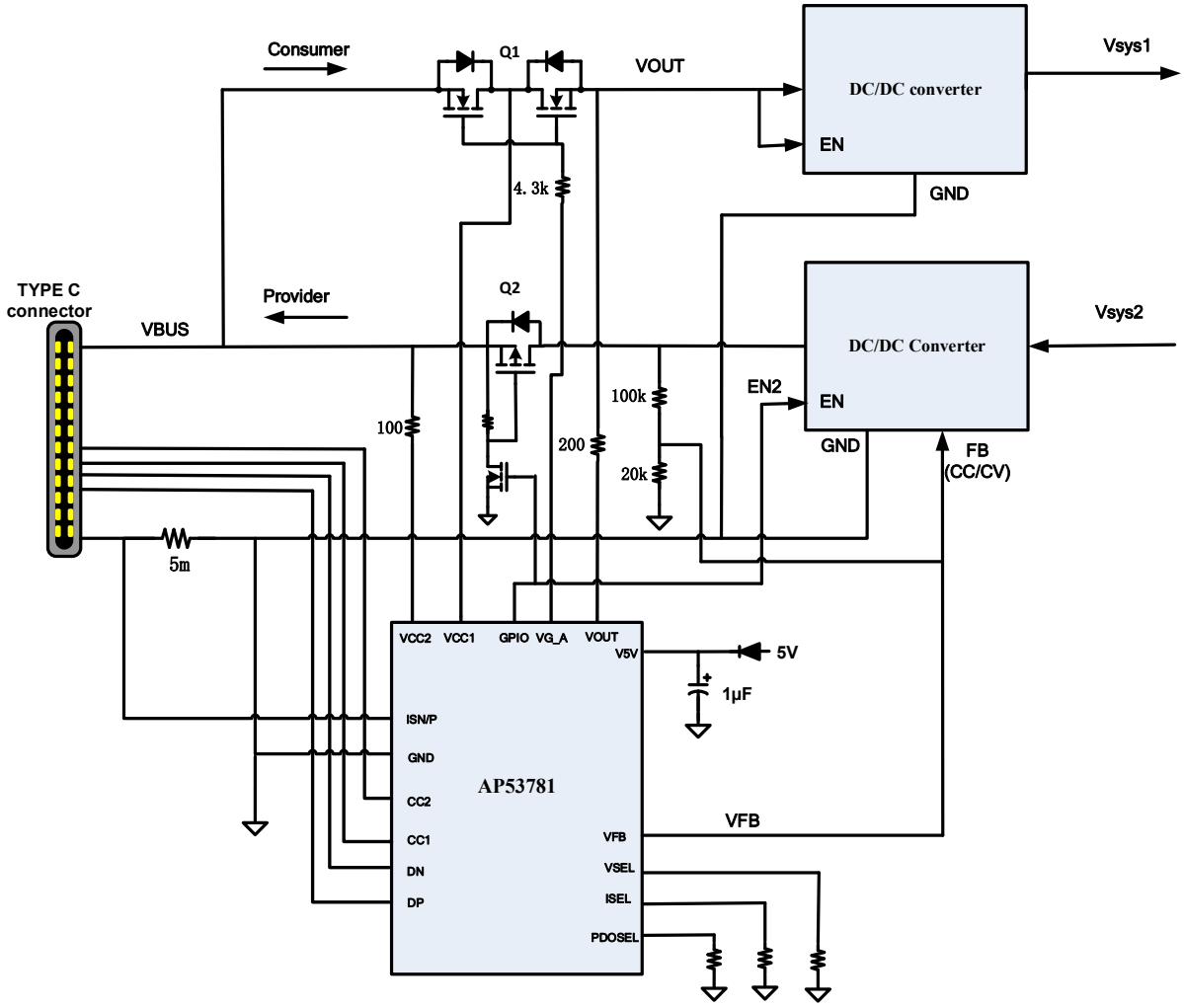


Figure 1. The AP53781 DRP Controller Without the Need of an External Host MCU

Pin Descriptions

Pin No.	Pin Name	Pin Function
1	VCC2	VBUS Voltage Detection Input
2	ISNP	Current Sense Node
3	GND	Ground
4	VSEL	RDO Voltage selection for sink consumer mode, connect an external resistor to ground to set the required voltage.
5	ISEL	RDO Current selection for sink consumer mode, connect an external resistor to ground to set the required current.
6	GPIO	General-Purpose Input/Output Pin
7	VFB	Analog Voltage Feedback Input for External PWM Controller
8	PDOSEL	PDO capability selection for source provider mode, connect an external resistor to ground to set the required power profile.
9	DP	DP of Type-C Connector
10	DN	DN of Type-C Connector
11	CC1	Configuration Channel 1 (CC1) of Type C
12	CC2	Configuration Channel 2 (CC2) of Type C
13	V5V	5V LDO output if VCC1 is powered. It can also be an alternative power supply input when VCC1 is unpowered. A 1μF cap is required to connect this pin to GND.
14	VOUT	VOUT terminal. It is used to detect output voltage and provides a discharge path with connecting an external 200Ω resistor in series.
15	VG_A	High-voltage gate driver with active high, connected to external nMOS switch.
16	VCC1	Chip power supply input when VBUS is active.
—	EPAD	Exposed pad is suggested to connect to Ground.

Functional Block Diagram

The AP53781 block diagram is shown in Figure 2 below, where the embedded MCU is used for the main operation of this DRP controller. Both source and sink roles support USB PD3.1 and QC protocols.

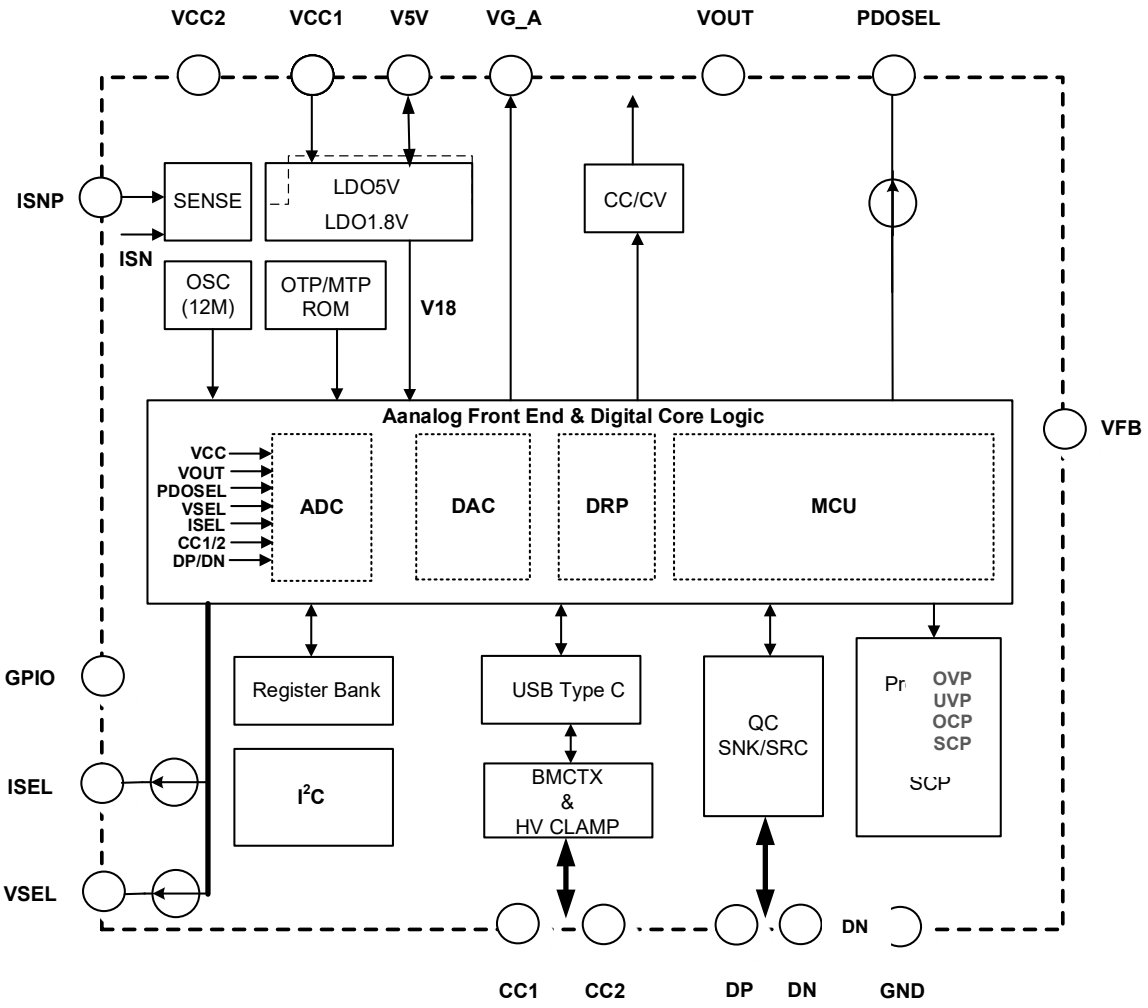


Figure 2. The AP53781 Block Diagram

Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{VCC1}, V_{VCC2}	Input Voltage at VCC1, VCC2 Pins	-0.3 to 34	V
V_{VFB}, V_{VSEL}, V_{ISEL}, V_{PDOSEL}, V_{GPIO}	Input Voltage at VFB, VSEL, ISEL, PDOSEL, GPIO Pins	-0.3 to 7	V
V_{ISNP}	Input Voltage at ISNP Pin	-0.3 to 2	V
V_{VOUT}	Input Voltage at VOUT Pin	-0.3 to 31	V
V_{VG_A}	Input Voltage at VG_A Pin	-0.3 to 38	V
—	Voltage from VG_A to VCC1 Pin	-38 to 7	V
V_{V5V}	Input Voltage at V5V Pin	-0.3 to 7	V
V_{CC1}, V_{CC2}	Input Voltage at CC1, CC2 Pins	-0.3 to 31	V
V_{DP}, V_{DN}	Input Voltage at DP, DN Pins	-0.3 to 24	V
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering, 10s)	+300	°C
ESD	Human Body Model	2	kV
ESD	Charged Device Model	750	V

Note: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

Package Thermal Information (Note 5)

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	31.3	°C/W
$R_{\theta JC(top)}$	Junction-to-Case (Top) Thermal Resistance	23.9	°C/W
$R_{\theta JB}$	Junction-to-Board Thermal Resistance	11.5	°C/W
Ψ_{JT}	Junction-to-Top Characterization Parameter	0.4	°C/W
Ψ_{JB}	Junction-to-Board Characterization Parameter	11.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-Case (Bottom) Thermal Resistance	5.8	°C/W

Note: 5. Test condition: device mounted on FR-4 substrate PC board, 2oz copper, with the minimum footprint.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{VCC1}, V_{VCC2}	Power Supply Voltage VCC1, VCC2 Pins	3.6	31	V
V_{V5V}	Input Voltage at V5V when no VBUS Power	3	5.5	V
V_{VFB}, V_{VSEL}, V_{ISEL}, V_{PDOSEL}, V_{GPIO}	Input Voltage at VFB, VSEL, ISEL, PDOSEL, GPIO Pins	0	5.5	V
V_{DP}, V_{DN}	Input Voltage at DP, DN Pins	0	3.7	V
T_A	Operating Ambient Temperature	-40	+85	°C
T_J	Operating Junction Temperature	-40	+125	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Power Supply Section (Note 6)						
V_{VCC1}	VCC1 Operating Voltage	—	2.5	3	3.5	V
V_{VCC1_HYS}	VVCC1 Hysteresis	—	—	0.3	—	V
I_{VCC1}	VCC1 Operating Current	—	—	2.5	6	mA
I_{VCC1_SLEEP}	VCC1 Input Current in Sleep Mode	CC1/2 detach	—	550	700	μA
$I_{VCC1\_SLEEP\_DRP}$	VCC1 Input Current in Sleep Mode under DRP Toggling Without Connection	—	—	30	50	μA
V_{VBUS_DB}	VBUS Voltage for Dead-Battery Mode	—	4	—	—	V
V5V Output						
V_{V5V}	V5V Output Voltage	—	4.4	5	5.4	V
I_{V5VOCP}	V5V Output Current Capability	—	—	30	—	mA
V_{VDRV_DO}	V5V Output Dropout	I_{VDRV} = 40mA (Note 9)	—	100	—	mV
Constant Voltage (CV) Control						
V_{VBUS_CV5}	VBUS Voltage for 5V CV Control	—	4.85	5	5.15	V
V_{VBUS_LSB}	VBUS Step per LSB	—	—	10	—	mV
V_{VBUS_Range}	VBUS Range	—	3.6	—	36	V
ΔVBUS%	VBUS Regulation Accuracy	VBUS = 3.6V to 28V	97	—	103	%
V_{CABLE}	Cable Compensation (Note 7)	VBUS = 3.6V to 28V	—	30	—	mV/A
Constant Current (CC) Control						
I_{CC_Range}	CC Range	—	1	—	5	A
CC_{1A3A}	Current Sense and CC Loop Correction	R_{SENS} = 5mΩ, I_L = 1A to 3A	-150	—	150	mA
CC_{3A5A}	Current Sense and CC Loop Correction	R_{SENS} = 5mΩ, I_L = 3A to 5A	-5	—	5	%
t_{CC}	CC Load Transient Current Settling Time	(Note 9)	—	—	250	ms
t_{CCCV}	CC to CV Transient Voltage Settling Time	(Note 9)	—	—	270	ms
SR_{IL}	Max Load Slew Rate for IL Changes.	(Note 9)	-150	—	150	mA/μs
Protection Function						
V_{OVP5V_SNK}	5V VBUS OVP @Sink	(Note 8)	6.3	7	7.7	V
V_{OVP9V_SNK}	9V VBUS OVP @Sink	(Notes 8, 9)	—	11	—	V
V_{OVP15V_SNK}	15V VBUS OVP @Sink	(Notes 8, 9)	—	17	—	V
V_{OVP20V_SNK}	20V VBUS OVP @Sink	(Notes 8, 9)	—	22	—	V
V_{OVP28V_SNK}	28V VBUS OVP @Sink	(Notes 8, 9)	—	30	—	V
$t_{DEBOUNCE\_OVP\_SNK}$	OVP Debounce Time @Sink	—	—	30	—	ms
V_{OVP5V_SRC}	5V VBUS OVP @Source	(Note 8)	5.5	6	6.5	V
V_{OVP9V_SRC}	9V VBUS OVP @Source	(Notes 8, 9)	—	10.8	—	V
V_{OVP15V_SRC}	15V VBUS OVP @Source	(Notes 8, 9)	—	18	—	V
V_{OVP20V_SRC}	20V VBUS OVP @Source	(Notes 8, 9)	—	24	—	V
V_{OVP28V_SRC}	28V VBUS OVP @Source	(Notes 8, 9)	—	30.8	—	V
$t_{DEBOUNCE\_OVP\_SRC}$	OVP Debounce Time @Source	—	—	3	—	ms

Notes:
6. There are 2 power suppliers for chip: VCC1 pin and V5V pin, as shown in Figure 6.
7. Cable compensation voltage can be adjusted by setting from 0 to N x V_{CABLE}, by setting where N is from 0 to 7.
8. OVP: 120%*PDO @Source, 110%*PDO @Source > 28V, 2V+RDO @Sink.
   UVP: 80%*PDO @Source, 80%*RDO @Sink.
   OCP: 110%*IPDO or 110%*IRDO.
   UVP_SINK_QC: set to 4V.
9. Guaranteed by design.

Electrical Characteristics (continued) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{UVP5V_SNK}	5V VBUS UVP @Sink	(Note 8)	3.5	4	4.5	V
V_{UVP9V_SNK}	9V VBUS UVP @Sink	(Notes 8, 9)	—	7.2	—	V
V_{UVP15V_SNK}	15V VBUS UVP @Sink	(Notes 8, 9)	—	12	—	V
V_{UVP20V_SNK}	20V VBUS UVP @Sink	(Notes 8, 9)	—	16	—	V
V_{UVP28V_SNK}	28V VBUS UVP @Sink	(Notes 8, 9)	—	22.4	—	V
$V_{UVP5V\_SINK\_QC}$	5V VBUS UVP @Sink (QC)	(Note 8)	3.5	4	4.5	V
$V_{UVP9V\_SINK\_QC}$	9V VBUS UVP @Sink (QC)	(Notes 8, 9)	3.5	4	4.5	V
$V_{UVP12V\_SINK\_QC}$	12V VBUS UVP @Sink (QC)	(Notes 8, 9)	3.5	4	4.5	V
$t_{DEBOUNCE\_UVP\_SNK}$	UVP Debounce Time @Sink	—	—	30	—	ms
V_{UVP5V_SRC}	5V VBUS UVP @Source	(Note 8)	3.5	4	4.5	V
V_{UVP9V_SRC}	9V VBUS UVP @Source	(Note 9)	—	7.2	—	V
V_{UVP15V_SRC}	15V VBUS UVP @Source	(Note 9)	—	12	—	V
V_{UVP20V_SRC}	20V VBUS UVP @Source	(Note 8)	—	16	—	V
V_{UVP28V_SRC}	28V VBUS UVP @Source	(Notes 8, 9)	—	22.4	—	V
$V_{UVP5V\_SRC\_QC}$	5V VBUS UVP @Source (QC)	(Note 8)	3.5	4	4.5	V
$V_{UVP9V\_SRC\_QC}$	9V VBUS UVP @Source (QC)	(Notes 8, 9)	—	7.2	—	V
$V_{UVP12V\_SRC\_QC}$	15V VBUS UVP @Source (QC)	(Notes 8, 9)	—	9.6	—	V
$t_{DEBOUNCE\_UVP\_SRC}$	UVP Debounce Time @Source	—	—	30	—	ms
OCP_{1A}	Over Current Protection (110%)	—	0.95	1.1	1.25	A
OCP_{3A}	Over Current Protection (110%)	—	3.15	3.3	3.45	A
OCP_{5A}	Over Current Protection (110%)	—	5.25	5.5	5.75	A
t_{OCP}	OCP Deglitch Time	—	—	30	—	ms
t_{SCP}	SCP Debounce Time @Source	—	—	4	—	μs
$t_{RESTART\_INTERVAL\_SCP}$	SCP Recovery Time @Source	—	—	0.8	—	s
T_{OTP}	Internal OTP Temperature	—	—	+130	—	°C
$T_{OTP-HYS}$	Internal OTP Temperature Hysteresis	—	—	+30	—	°C
CC1/CC2 (CCx) Pin Section						
V_{OH_CCX}	Pull High Voltage of CCx	—	3.0	3.3	3.6	V
I_{Rp_80}	CCx Pullup Current as SRC – Default	R_D = 5.1kΩ	—	80	—	μA
I_{Rp_180}	CCx Pullup Current as SRC – 1.5A	R_D = 5.1kΩ	—	180	—	μA
I_{Rp_330}	CCx Pullup Current as SRC – 3.0A	R_D = 5.1kΩ	303.6	330	356.4	μA
R_{D_V5V}	CCx Pulldown Resistance as SNK	—	4.6	5.1	5.6	kΩ
V_{ATH_80}	Attach Detection of CCx – Default	R_D = 5.1kΩ	—	0.408	—	V
V_{ATH_180}	Attach Detection of CCx – 1.5A Mode	R_D = 5.1kΩ	—	0.918	—	V
V_{ATH_330}	Attach Detection of CCx – 3.0A Mode	R_D = 5.1kΩ	—	1.68	—	V
V_{CCx_OVP}	CCx Overvoltage Protection	—	5.2	5.6	6.1	V
V_{RdCCX_80}	Source = 80μ for Dead Battery	—	—	0.93	—	V
V_{RdCCX_180}	Source = 180μ for Dead Battery	—	—	1.057	—	V
V_{RdCCX_330}	Source = 330μ for Dead Battery	—	—	1.178	—	V
t_{SLEEP}	Enter Sleep Mode Time after Cable Detached	—	—	3	—	s

Notes: 8. OVP: 120%*PDO @Source, 110%*PDO @Source > 28V, 2V+RDO @Sink.
UVP: 80%*PDO @Source, 80%*RDO @Sink.
OCP: 110%*IPDO or 110%*IRDO.
UVP_SINK_QC: set to 4V.
9. Guaranteed by design.

Electrical Characteristics (continued) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
USB PD Transceiver						
V_{OH_TxDC}	Output High of CCx for BMC Tx	(Note 9)	1.05	1.125	1.2	V
V_{OL_TxDC}	Output Low of CCx for BMC Tx	(Note 9)	—	—	0.075	V
V_{IH_RX}	Noise Margin for BMC Rx	(Note 9)	0.25	—	0.85	V
V_{TH_RX}	Vth of BMC_RX	(Note 9)	—	0.55	—	V
t_{R_Tx}	Rising Time of CCx for BMC Tx	(Note 9)	300	—	—	ns
t_{F_Tx}	Falling Time of CCx for BMC Tx	(Note 9)	300	—	—	ns
DP/DN and QC Section (Source + Sink)						
$V_{OVP\_DP/DN}$	DP/DN Line OVP Threshold	—	4.2	4.5	4.8	V
V_{DP/DN_APP}	DP/DN Apple Mode 2.7V Output	—	2.48	2.68	2.88	V
V_{DP/DN_0P6V}	DP/DN DCP 0.6V Output Voltage	Source Current 250μA	—	0.6	—	V
R_{DP/DN_DWN20k}	DP/DN 20k Pulldown Resistor	—	16	20	24	kΩ
$R_{DP/DN\_DWN900k}$	DP/DN 900k Pulldown Resistor	—	700	900	1100	kΩ
R_{DP/DN_short}	DPDN Short Resistor	—	5	20	40	Ω
R_{DN_IMP}	Impedance Check at DN	—	175	300	375	Ω
$V_{OH\_DP/DN}$	Output High Voltage of DP/DN	Source Current 4mA	2.9	3.1	3.6	V
$V_{OL\_DP/DN}$	Output Low Voltage of DP/DN	Sink Current 4mA	—	—	200	mV
VCONN Capability						
V_{CONN_DROP}	V_{CONN_DROP} Voltage (V5V-V_{CONN})	Source Current 20mA	—	600	—	mV
DRP Section						
I_{DRPNC}	DRP Current Consumption while Toggling Without Connection	—	—	30	—	μA
t_{DRP}	DRP t_{Rp} + t_{Rd} Cycle Time	—	—	80	—	ms
D_{Rp}	Duty of Rp During a DRP Cycle	—	—	50	—	%
VG_A Gate Driver						
$V_{VG\_A\_SO}$	VG_A Gate to Source Overdrive	V_{CC} = 5V	3	—	—	V
I_src	Driving Capability	V_{GS} @2.5V	—	10	—	μA
t_{ON}	Turn-On Time	V_{GS} @3.5V & C_{LOAD} = 10nF	—	6.5	—	ms
VBUS and VOUT Discharge Current						
I_{DISCHG_VBUS}	Discharge Current for VBUS Pin	V_{VBUS} = 5V (Note 9)	—	150	—	mA
I_{DISCHG_VOUT}	Discharge Current for VOUT Pin	V_{VOUT} = 5V (Note 9)	—	90	—	mA

Note: 9. Guaranteed by design.

Electrical Characteristics (continued) (@T_A =+25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ADC Section						
N_{ADC}	Resolution	—	—	8	—	bit
V_{VREF_ADC}	Reference Voltage of ADC	—	2.026	2.046	2.066	V
DNL_{ADC}	DNL	—	—	4	—	LSB
INL_{ADC}	INL	—	—	2	—	LSB
f_{SADC}	ADC Sampling Frequency	—	—	66	—	kHz
VSEL, ISEL, PDOSEL Section						
I_{VSEL}	VSEL Current Source	(Note 9)	—	20.6	—	μA
I_{VSEL_Var}	VSEL Current Variation	(Note 9)	-5	—	+5	%
I_{ISEL}	ISEL Current Source	(Note 9)	—	20.4	—	μA
I_{ISEL_Var}	ISEL Current Variation	(Note 9)	-5	—	+5	%
I_{PDOSEL}	PDOSEL Current Source	(Note 9)	—	20	—	μA
I_{PDOSEL_Var}	PDOSEL Current Variation (Note 7)	(Note 9)	-5	—	+5	%
GPIO Pin						
V_{IH}	Input High Threshold Voltage of GPIO	—	1.4	—	—	V
V_{IL}	Input Low Threshold Voltage of GPIO	—	—	—	0.4	V
V_{OL}	Output Low Level Voltage of GPIO	Sink Current 4mA	—	—	300	mV
t_R	Rising Time	(Note 9)	—	—	300	ns
t_F	Falling Time	(Note 9)	—	—	300	ns

Notes: 7. Cable compensation voltage can be adjusted by setting from 0 to N x V_{CABLE}, by setting where N is from 0 to 7.
9. Guaranteed by design.

Functional Overview

AP53781 Overview

The AP53781 is a highly integrated USB Type-C DRP port controller that complies with the latest USB PD3.1 standards and is applied in systems without an external MCU. The desired Sink RDO and Source PDO data are pre-loaded in the embedded one-time-programmable (OTP) memory and could be selected by external resistors on the predetermined pins.

The AP53781 includes a USB Type-C CC logic and PD transceiver, DRP operation and power control, constant current and constant voltage (CC/CV) feedback loops, power protections for Sink and Source, RDO and PDO selection, and an embedded 8-bit 1T 8051 compatible MCU to handle protocol handshake. It is designed to support Extended Power Range (EPR)/Adjustable Voltage Supply (AVS) up to 28V and Standard Power Range (SPR) up to 21V.

Type-C Configuration Channel (CC) Logic

The CC logic block includes all termination resistors (Rp and Rd), control switches, cable detection and connection logic. Rp and Rd resistors are required to implement connection detection, plug orientation detection, and USB Source/Sink role establishing as required by the USB Type-C specification.

As the example shown in Figure 3, the AP53781 is acting as a sink device and communicating with a cable and a PD source device. There are two CC pins on the connector, CC1 and CC2, used to implement a configuration process to establish and manage the Source-to-Sink connection. The Source side and Sink side will assign a pull-high resistor Rp and a pull-low resistor Rd on CC1 pin respectively, and the e-Marker chip for cable will show a Ra resistance at CC2 pin.

The CC1 pin voltage amplitude will depend on the resistor dividing effect of source Rp, sink Rd during the cable insertion. The AP53781 can then decide if the cable is attached, detached, or e-Marker embedded by detecting the CC2 voltage. At the same time, the CC1 voltage is used to configure which side serves as Type-C Source or Sink, and the Type-C cable plug orientation.

After the Source to Sink connection is built up, the V_{CONN} switch is turned on by Source to feed power to the cable through unconnected CC2 pin, and then the data path from Source to Sink is accomplished. Meanwhile, the VBUS switch is turned on to provide 5V from Source to VBUS, and its current capability is assigned by the pullup resistor or current source on its CC pin.

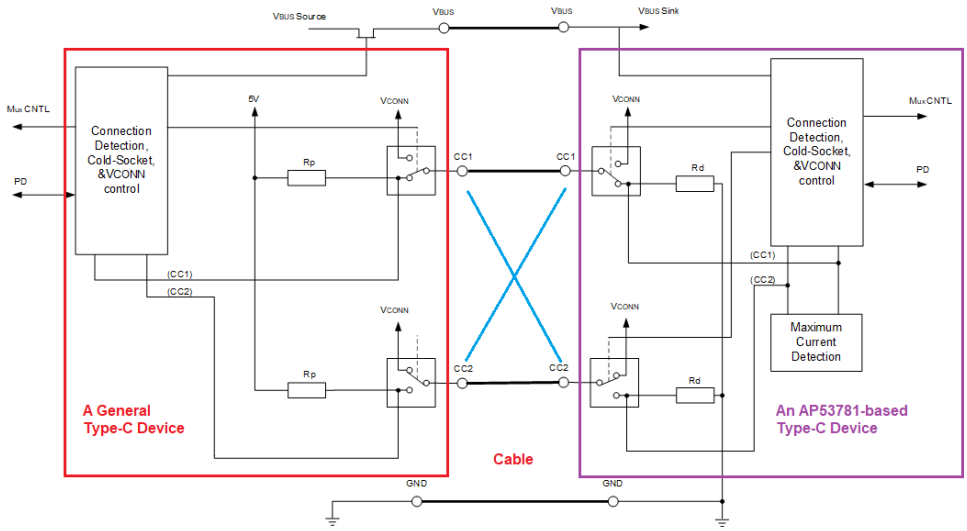


Figure 3. The AP53781-based Type-C/PD device connects with another Type-C/PD device at the opposite end of the cable.

DRP Operation

The AP53781 acts as a USB PD DRP controller after the cable is plugged in. It toggles periodically the Type-C CCx pin connections between the pulldown resistance Rd and pullup resistance Rp as shown in Figure 4. When the AP53781 detects a Rd connected externally to CCx pin, it will act as a power provider and its PDO data are assigned by PDOSEL pin. If the AP53781 detects a Rp connected externally to CCx pin, it will act as a power consumer and its RDO data are assigned by the ISEL and VSEL pins. The Rp+Rd toggle period is fixed at 80ms, and 50% duty for Rp and Rd respectively. Here, the Rp resistor is implemented as a current source, I_{Rp}.

Functional Overview (continued)

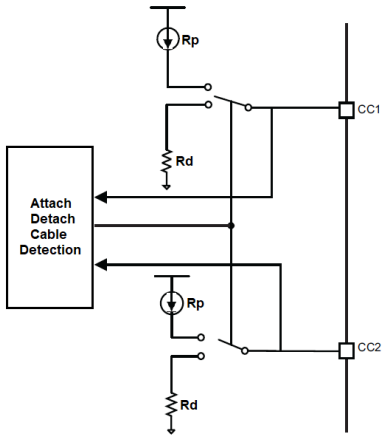


Figure 4. The AP53781 toggles CCx pin connections between Rp and Rd during the DRP handshake.

USB PD Physical Layer

The USB PD physical layer includes a USB Type-C baseband transceiver, physical-layer logic, and buffer for PD message handling, as shown in Figure 5. This transceiver performs the Bi-phase Mark Coding (BMC) and the 4b/5b encoding and decoding functions as well as integrating the analog frontend circuit. USB-PD messages are transmitted using a BMC signaling. The BMC signal is output on the same pin (CC1 or CC2, aligned with the orientation of the reversible USB Type-C cable) that is DC biased due to the Rp (or Rd) cable attach mechanism. The transmitter driver overdrives the CC DC bias while transmitting, but returns to a Hi-Z state, allowing the DC voltage to return to the CC level when it is not transmitting. All the communication is half-duplex, and the physical layer should implement collision avoidance to minimize communication errors on the channel.

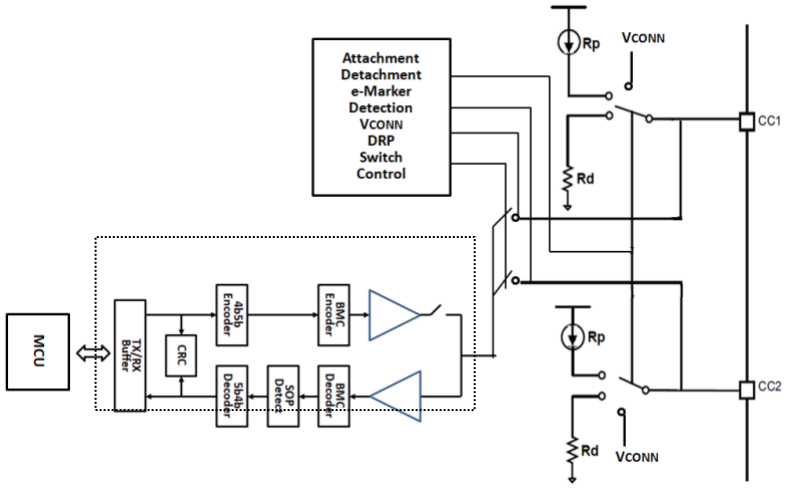


Figure 5. The USB PD uses BMC signaling and CC pin to communicate with another USB PD device.

Chip Power Overview

The AP53781 is powered from either VCC1 pin or V5V pin. Once the VBUS is enabled, either from provider or consumer, the VBUS power will go through the body diode of the VBUS switch, and then enter VCC1. The VCC1 will enable analog block and V5V LDO to power the core 5V circuitry and output a 5V voltage source with limited loading for external applications. The extra LDOs step the voltage down from 5V to 3.3V and 1.8V to power the I/O pins and digital core circuitry. The power supply plan is shown in Figure 6.

When the AP53781 is not active in either provider mode or consumer mode, the VCC1 power is not available from VBUS, and an external power supply with 5V level should be inserted from the V5V pin. The external 5V supply will enter the internal V5V power path through the external diode to provide for the entire chip circuit and external application.

Functional Overview (continued)

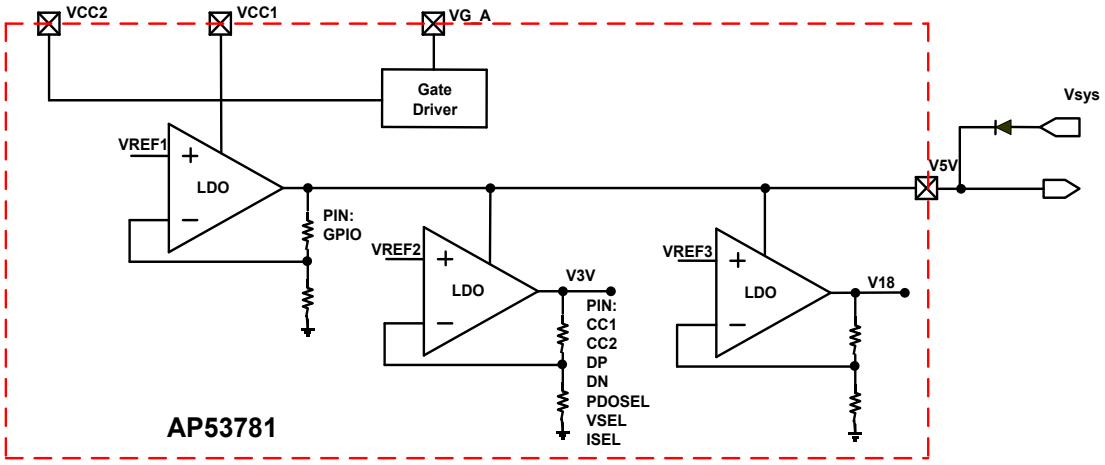


Figure 6. The AP53781 Chip Power Plan

Dead-Battery Mode

When neither V5V pin nor VCC1 pin can provide chip power, the AP53781 enters the dead-battery mode by presenting a Rd resistance on its respective CCx pins. Once an active Type-C device is attached to this AP53781, the Rd resistance will allow the AP53781 to act as a Sink device and enable a 5V output on the VBUS if the plugged-in device is a Type-C Source or DRP controller. The 5V power supply will go through the body diode of the VBUS nMOS Q1 switch and feed into VCC1 pin to power on the AP53781 again, as shown in Figure 7.

The AP53781 then enters the power-on initialization sequence by setting up its internal registers and receives PDO and sends RDO parameters according to the corresponding resistance on ISEL, VSEL pins.

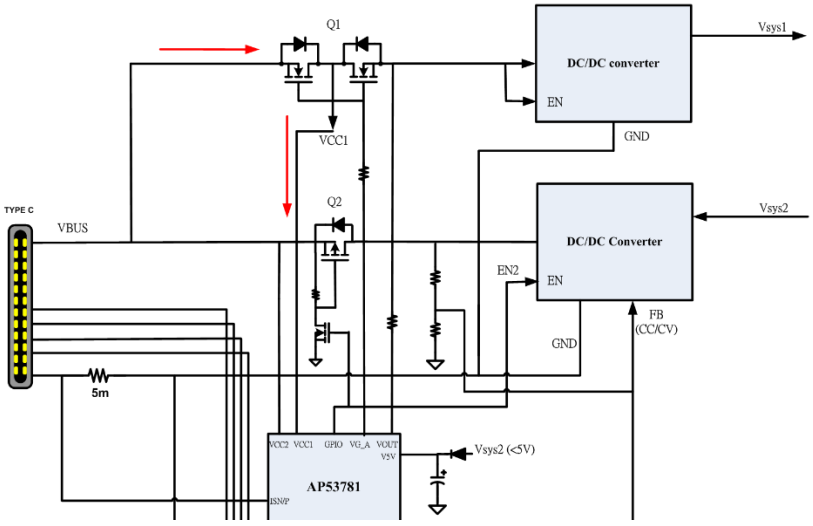


Figure 7. The Power Path in Dead-Battery Mode

Power Protection in Source and Sink Modes

The AP53781 supports OVP/UVP/OCP power protection functions for source provider path and sink consumer path. The AP53781 provides a high-voltage VG_A to drive an external low cost high-side nMOS switch for VBUS power on/off control. A 4.3kΩ resistance is suggested to connect the VG_A pin to the external nMOS gate. Figure 8 shows the consumer and provider paths for an AP53781-based system.

During the consumer mode, once the RDO contracts are matched between source side and sink side, the VG_A is pulled high to enable the nMOS switch and then VBUS can provide power to the DC/DC converter input. While in the provider mode, once the PDO contracts are matched between source and sink, a GPIO can be pulled high to enable the pMOS switch and then the DC/DC converter can provide power to VBUS.

Functional Overview (continued)

The OVP threshold is set at 120% of contracted PDO and RDO output. Once the VBUS voltage is higher than OVP threshold, the corresponding VBUS MOS is turned off and an internal discharge path from VBUS pin to ground is turned on to reduce the overvoltage duration.

The UVP threshold is set at 75% of contracted PDO and RDO output. Once the VBUS voltage drops to UVP threshold, the corresponding VBUS MOS is turned off to avoid the abnormal operation of the electrical appliances.

The AP53781 integrates a low-side current sense amplifier that can detect current levels ranging from 100mA up to 6A across a 5mΩ external resistor. The OCP threshold is set at 110% of PDO and RDO's maximum load. Once the VBUS output current is higher than OCP threshold, the AP53781 will shut down the corresponding VBUS MOSFET. If AP53781 acts as a Source, a "Hard Reset" command will be sent to the Sink device at the same time.

Based on high-voltage process, the AP53781 offers VBUS short protection for CCx pins up to 34V.

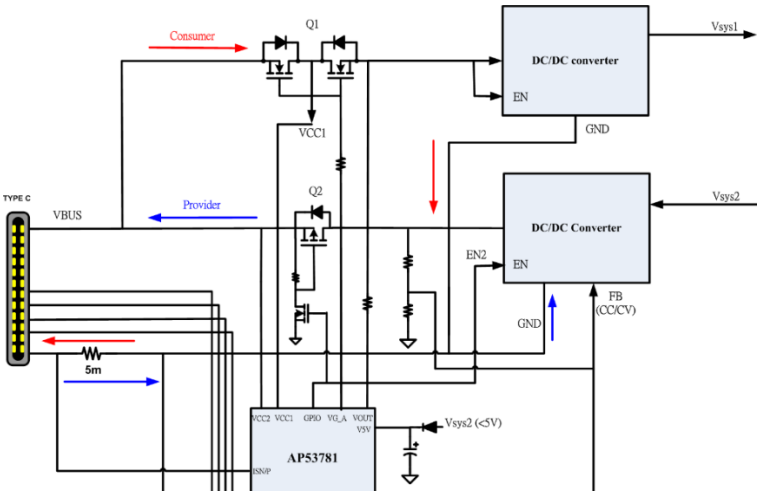


Figure 8. The Consumer and Provider Paths for an AP53781-Based System

VBUS and VOUT Discharge Path

To meet the timing requirements of the USB PD specification and field experience, the AP53781 supports VBUS and VOUT discharge paths to speed up the voltage decreasing of power path, where VCC2 and VOUT pins are respectively connected to an internal MOSFET and discharge resistor. Through firmware control, the discharge paths act as a bleeder to help discharge the energy stored in the output capacitor. With this mechanism, VBUS can be regulated to 5V upon the detachment of a connected device, or to a lower desired output voltage level upon a request from the protocol handshake result, such as RDO and PDO voltage transition, and power protection. A 200Ω resistor between VOUT node and VOUT pin is required. Also, a 100Ω resistor between VBUS node and VCC2 pin is required.

VBUS Voltage Regulation and VFB Feedback

The AP53781 includes constant voltage (CV) loop for VBUS voltage regulation. Once the AP53781 acts as a Source role, it will generate the PDO voltage to provide the attached device after the protocol handshake.

It uses a current DAC to sink or source the corresponding current directly from the external DC/DC feedback pin according to requested PDO voltage, as shown in Figure 9. Due to the negative feedback loop, the current flowing through R1 is changed to keep VFB staying constant. Therefore, the VBUS is transitioned to a new level.

The current DAC in VFB pin has an LSB of 0.1μA. That means if the feedback R1/R2 network of the external DC/DC is 100kΩ/2kΩ, then the VBUS voltage change resolution is 10mV per step. It is recommended to choose R1/R2 resistors with 1% accuracy for a better matching in VBUS voltage.

$$\mathrm{VBUS} = \frac{\mathrm{VFB} * (\mathrm{R2} + \mathrm{R1})}{\mathrm{R2}} + ID * R1$$

$$\text{VBUS Transition by } ID * R1$$

Functional Overview (continued)

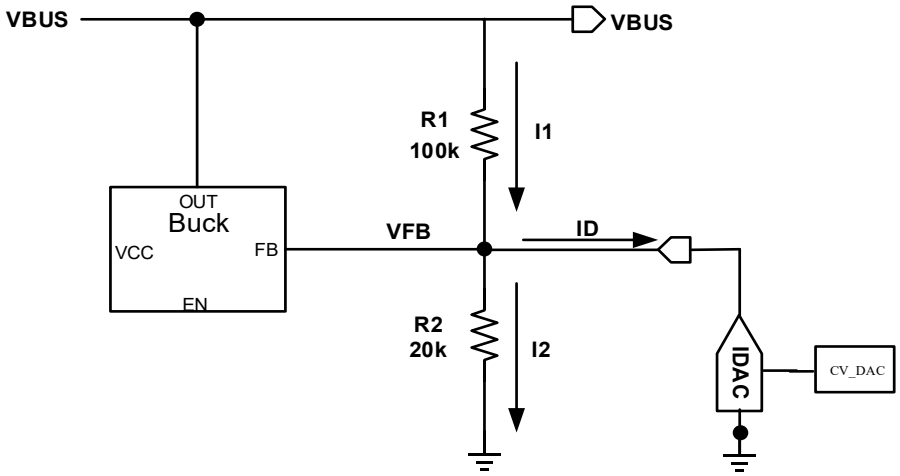


Figure 9. The current DAC is used to sink or source a current from the external DC/DC feedback network.

Constant Current Loop

The AP53781 provides a constant current (CC) loop to provide the PD AVS function or other kinds of protocol which uses CC function. The CC loop, as shown in Figure 10 implemented by sensing the low-side IR drop on Rsense resistor and transfer to voltage by internal current sense then pass to internal digital filter block. This proprietary digital control scheme will adjust the ID of IDAC (in Figure 10) according to both voltage and current information.

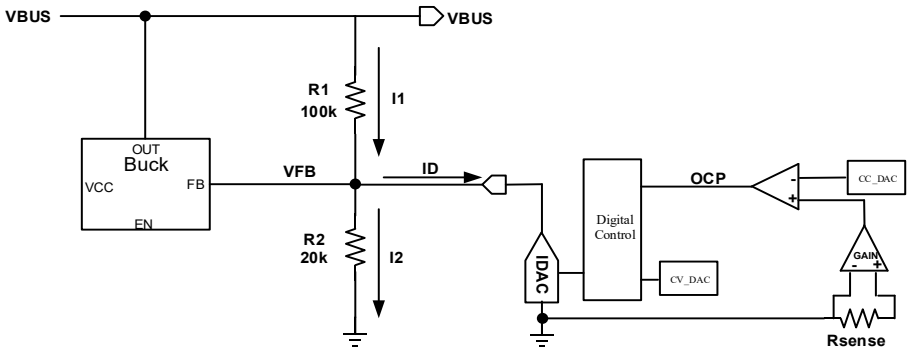


Figure 10. The Constant Current Loop

ADC Converter

The AP53781 supports an internal successive approximation ADC. The input to the ADC is an analog multiplex that connects multiple inputs from various voltage and current sources in the chip. The proper signal could be digitized at the predetermined time and controlled by the firmware. The ADC output is available to be read and used by the embedded MCU. Through data processing and appropriate algorithm, the AP53781 can make a precise management of the DRP controller.

Functional Overview (continued)

QC Sink Support

The AP53781 not only provides QC on source side but also provides the QC on sink side for protocol communication handshake. The High Voltage Dedicated Charging Port (HVDCP) Detection Flow for QC Sink Support is shown in Figure 11 below.

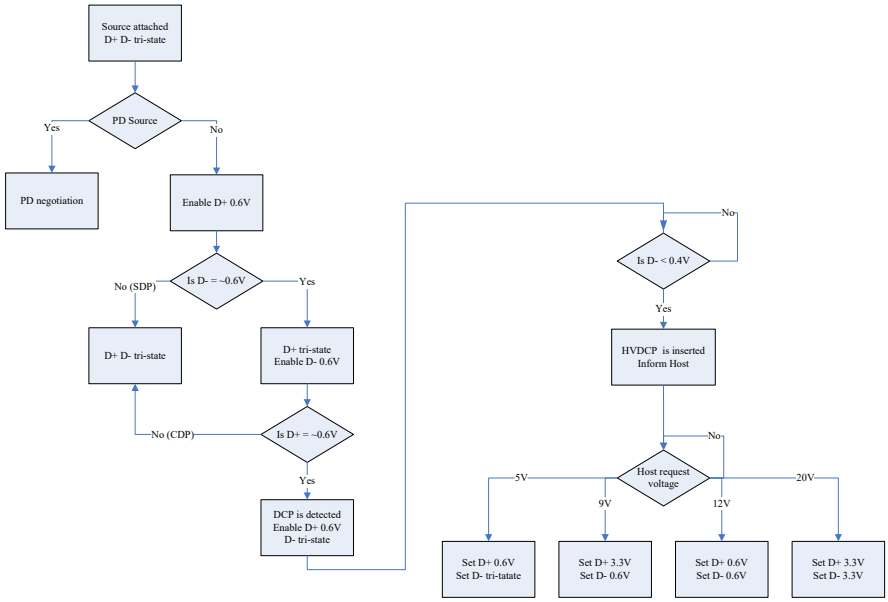


Figure 11. The AP53781 provides HVDCP detection flow for QC sink support

RDO Power Selection

When acting as a sink controller, AP53781 generates a RDO to negotiate power profile with a PD source controller. To easily set up the voltage and current values through hardware setting, up to eight resistors are supported both for voltage and current selections which are connected to VSEL and ISEL pins. It is recommended to use the resistors with ±1% accuracy or better, to connect to the VSEL and ISEL pins to ensure the request selection. The mapping between VSEL/ISEL selection and resistance values are illustrated in Table 1. The resistance is monitored in real time, and a “Request” is sent when the resistance changes.

If the current requirement is greater than 3A, a suitable e-Marker cable with over 3A current rating is needed.

Index	1	2	3	4	5	6	7	8	Notes
VSEL	5V	9V	12V	15V	20V	28V	5V	5V	
Resistance (kΩ, 1%)	100	82	66	52	39	26	15	5.1	Resistor OPEN => 5V. Resistor shorted to Ground => 5V

Index	1	2	3	4	5	6	7	8	Notes
ISEL	Auto	1A	1.5A	2A	2.5A	3A	4A	5A	
Resistance (kΩ, 1%)	100	82	66	52	39	26	15	5.1	Resistor OPEN => Auto. Resistor shorted to Ground => 5A

Table 1. The preloaded VSEL and ISEL data in AP53781DMZ16-13-FA01 supports PD3.1 SPR.

Data Role Swap Function

The FW loaded in P/N AP53781DMZ16-13-FA01 has default configuration to accept Data Role Swap request from Port Partner.

Functional Overview (continued)

RDO Matching Mechanism

After the POR initiation, the AP53781 starts the PD negotiation with the external PD source. All of the source capability information is received and stored into its internal registers during the handshake. The matching mechanism of PDO selection used in AP53781 is summarized in Table 2, where voltage matching is performed first, and then current matching is proceeded in case voltage match happens.

Source PDO	Voltage Match Criteria (Note 10)	Current Match Criteria (Note 10)
Fixed PDO	$V_{FIXED} = V_{VSEL}$	$I_{ISEL} \le I_{MAX}$

Note: 10. V_{VSEL}: voltage selected by V_{SEL} pin
I_{ISEL}: current selected by ISEL pin
V_{FIXED}: voltage of Fixed PDO
I_{MAX}: maximum current of PDO
PDP: output power of AVS PDO (W)

Table 2. RDO Matching Mechanism Used in the AP53781 Sink Controller

After voltage matching process is completed, the PDOs that meet the voltage matching criteria will perform current matching flow again. During the current matching process, fixed PDO with I_{MAX} greater than I_{ISEL} will be selected.

During the PD handshake between the TCD and the external PD source, the AP53781 acquires and stores source capability into relevant registers. If there are valid source capabilities that match with the RDO selection before timeout, the AP53781 policy engine then requests a suitable power profile from the source adapter.

Voltage Drop Compensation

When AP53781 works as a sink, if VBUS is 4% lower than requested voltage, AP53781 will request a voltage increase up to requested voltage +1.3V in PPS mode.

PDO Power Selection

There are a total of 8 preloaded PDO power profiles in the OTP memory of the AP53781 when it acts as a source controller, as shown in Table 3. By connecting the corresponding 1% precision resistor to PDOSEL pin to get the desired power profile, system designers could field customize the AP53781 to fit different output power requests. The selection resistance is monitored in real time, and a new “Source Capabilities” is sent when the resistance changes.

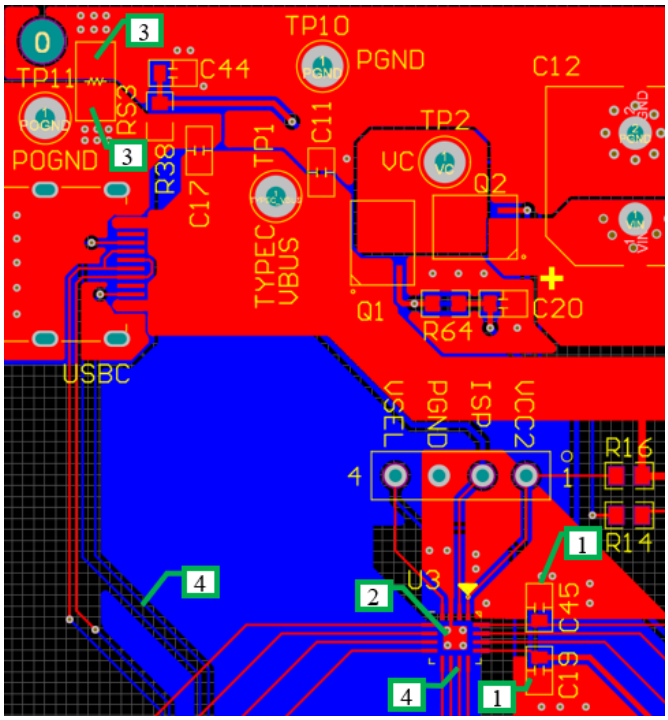
OUTPUT POWER										
Power Profile NO	Power Data									Selection Resistance (kΩ, 1%)
	SPR Fixed PDO						SPR AVS		QC/BC1.2	
1	25W	5V / 3A	9V / 2.78A	12V / 2.08 A					5V~12V / 18W	52
2	30W	5V / 3A	9V / 3A	12V / 2.5 A	15V / 2A	20V / 1.5A	9V~15V / 2A	15V~20V / 1.5A	5V~12V / 27W	39
3	35W	5V / 3A	9V / 3A	12V / 2.9A	15V / 2.33A	20V / 1.75A	9V~15V / 2.33A	15V~20V / 1.75A	5V~12V / 27W	26
4	45W	5V / 3A	9V / 3A	12V / 3A	15V / 3A	20V / 2.25A	9V~15V / 3A	15V~20V / 2.25A	5V~12V / 27W	15
5	65W	5V / 3A	9V / 3A	12V / 3A	15V / 3A	20V / 3.25A	9V~15V / 3A	15V~20V / 3.25A	5V~12V / 27W	5.1
6	15W	5V / 3A							5V / 15W	66
7	7.5W	5V / 1.5A							DCP	82
8	2.5W	5V / 0.5A							SDP	100
										Resistor OPEN =>2.5W Resistor shorted to Ground => 65W

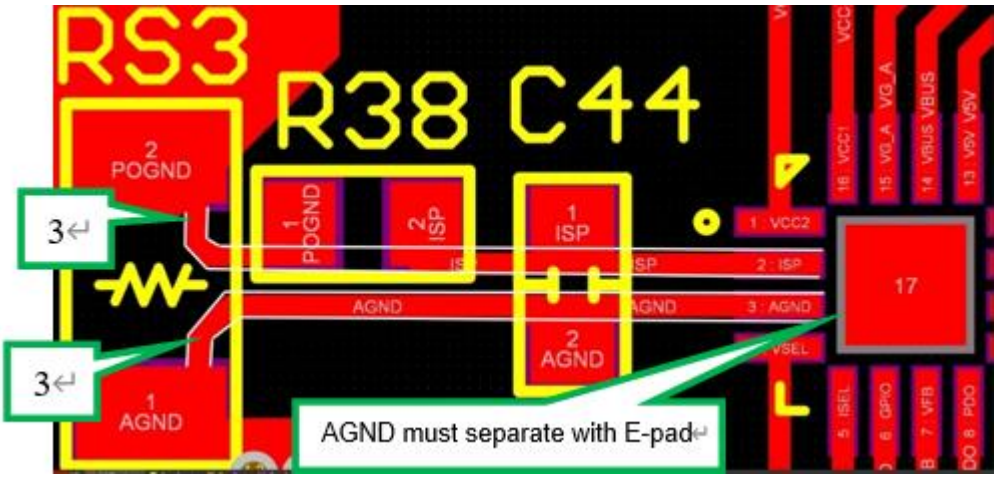
Table 3. The Preloaded PDO Data in AP53781DMZ16-13-FA01 can Support PD3.2 SPR up to 65W.

PCB Layout Guideline

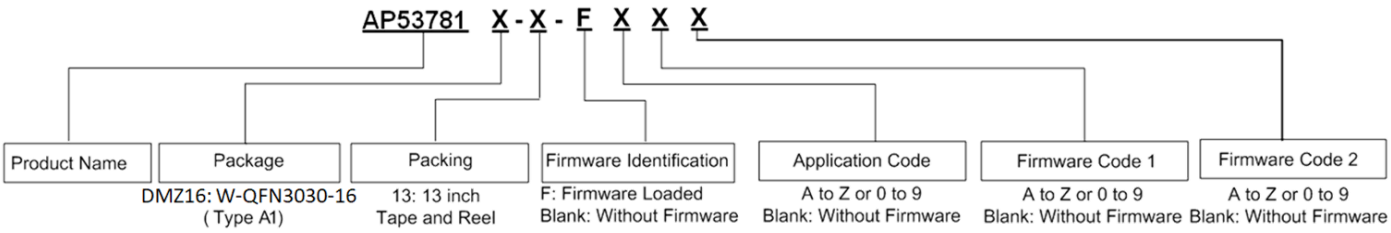
Suitable PCB layout is critical for stable operation and better ESD performance. Follow some guidelines as below:

1. Place the Vcc/V5V decoupling capacitor as close to the pins as possible.
2. The exposed pad of the IC must be connected to GND. It is better for noise immunity.
3. Current sensing traces must start directly from the footprint pads of the current sensing resistor.
4. Use traces to connect CC1/CC2 pins to the USB Type-C receptacle as short as possible.





Ordering Information (Note 11)



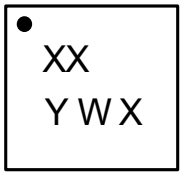
Orderable Part Number (Note 12)	Package	Identification Code	Firmware Inside	Packing	
				Qty.	Carrier
AP53781DMZ16-13-FA01	W-QFN3030-16 (Type A1)	AY	Standard Firmware (Function as Described in Datasheet)	3000	13” Tape & Reel
AP53781DMZ16-13-FXXX			Customized Firmware		

Note: 11. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.
12. It is recommended to order Standard Firmware device based on functions described in the datasheet. For without firmware and customized options, please contact us or your local Diodes representative.

Marking Information

W-QFN3030-16 (Type A1)

(Top View)

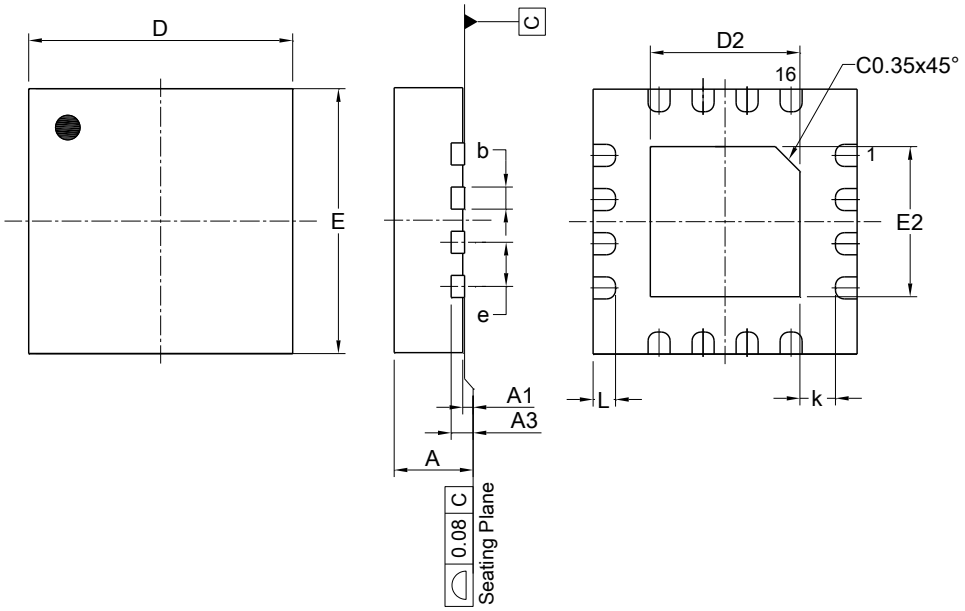


XX : Identification Code
Y : Year : 0 to 9 (ex: 6 = 2026)
W : Week : A to Z : week 1 to 26;
a to z : week 27 to 52; z represents
week 52 and 53
X : Internal Code

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN3030-16 (Type A1)

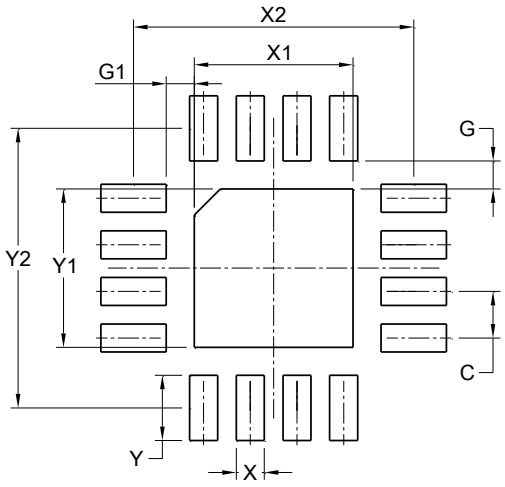


W-QFN3030-16 (Type A1)			
Dim	**Min**	**Max**	**Typ**
A	0.70	0.80	0.75
A1	0.00	0.05	0.02
A3	0.203 REF		
b	0.18	0.30	0.25
D	2.90	3.10	3.00
D2	1.65	1.75	1.70
E	2.90	3.10	3.00
E2	1.65	1.75	1.70
e	0.50 BSC		
k	0.20	--	--
L	0.20	0.30	0.25
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN3030-16 (Type A1)



Dimensions	Value (in mm)
C	0.500
G	0.300
G1	0.300
X	0.300
X1	1.700
X2	3.000
Y	0.700
Y1	1.700
Y2	3.000

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per J-STD-202 e3
- Weight: 0.017 grams (Approximate)

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