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Chapter 1. Introduction

The growing popularity of standard USB PD3.1 chargers for mobile phones and notebook PCs spurs the demand for designers to leverage standard PD3.1 chargers to replace purposely and individually built chargers for battery-powered electronic devices, reducing e-waste.

The AP33771C Evaluation Board (EVB) is intended to be used as an evaluation vehicle for charging applications between a USB Type-C® connector-equipped Device (**TCD**, energy sink) and a USB-C connector-equipped PD charger or adaptor (**PDC**, energy source) through a USB-C to USB-C cable.

Figure 1 illustrates a TCD embedded with a PD3.1 sink controller IC (i.e. [AP33771C](#)). This is physically connected to a PDC, embedded with a USB PD3.1 source controller (e.g. AP43771) through a suitable USB-C to USB-C cable. Based on the USB PD3.1 compliance protocol, the AP33771C may go through the USB PD3.1 standard negotiation process with the AP43771, and then the TCD will retrieve power from the PDC.

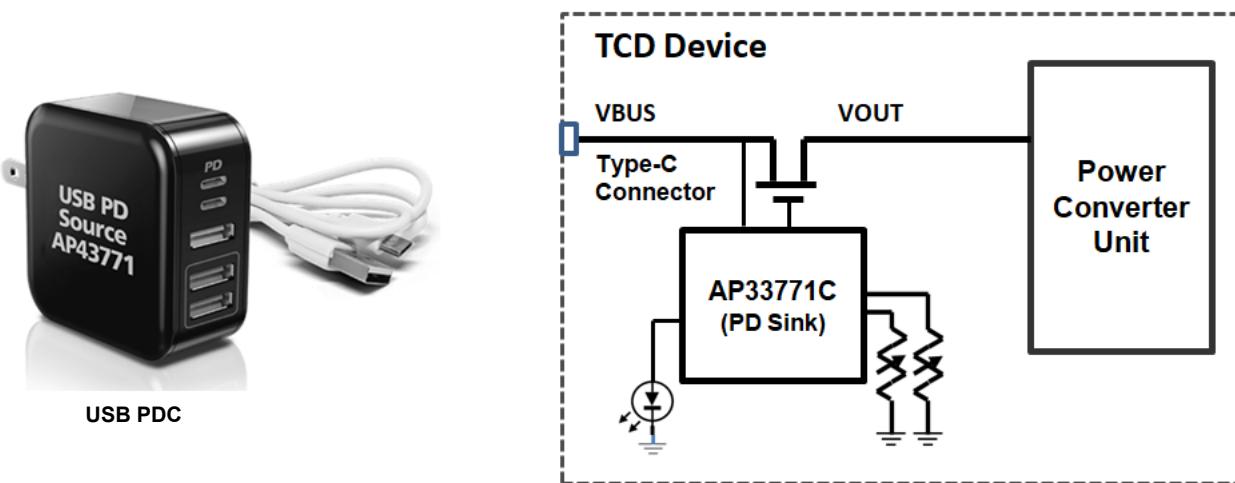


Figure 1 – A typical TCD with the AP33771C PD3.1 Sink Controller requesting power from a USB PDC

To improve the AP33771C's user experience as a USB sink controller in TCDs, the AP33771C has built-in firmware to deal with automatic cable voltage drop compensation, as well as legacy USB Type-A charging through a USB-A to USB-C cable.

The AP33771C's EVB User Guide explains a simple resistor-setting arrangement to request the desired input voltage and current for a typical TCD. The grant voltage and current back from a PDC, for a successful match with the source capability, can cover the power request.

Chapter 2. AP33771C Sink Controller

2.1 Package Pinout

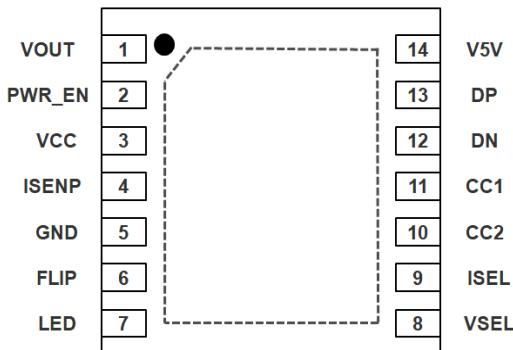


Figure 2 – Package Pinout

2.2 Pin Descriptions

Pin No.	Pin Name	Type (Notes)	Pin Function
1	VOUT	AHV	Terminal for VOUT monitoring.
2	PWR_EN	AHV	To control external VOUT. Connected to external NMOS switch, ON (High) or OFF (Low).
3	VCC	AHV	The power supply of the AP33771C. A 1 μ F cap is required to connect this pin to GND pin.
4	ISENP	AHV	Current-sense positive node.
5	GND	GND	Ground
6	FLIP	DO	Flip indicator of Type-C plug. Is low if CC is connected to CC1 and high if connected to CC2.
7	LED	DO	LED indicator of the system status
8	VSEL	AI	Voltage selection pin, connect resistance to ground to set Voltage.
9	ISEL	AI	Current selection pin, connect resistance to ground to set Current.
10	CC2	AIO	USB Type-C configuration channel 2
11	CC1	AIO	USB Type-C configuration channel 1
12	DN	AIO	USB 2.0 data negative node
13	DP	AIO	USB 2.0 data positive node
14	V5V	AP	5V LDO output if VCC is on. A 1 μ F cap is required to connect this pin to GND.
-	EPAD	GND	Exposed pad is suggested to connect to Ground

Table 1 – Pin Descriptions of the AP33771C PD Sink Controller

Notes:

- AHV – Analog High-Voltage pin
- AP – Power for Analog Circuit and Analog Input/Output pins, 5.0V operation
- AI – Analog Input pin
- AIO – Analog Input/Output pin; DP/DN & CC1/CC2 are 3.3V operation
- DO – Digital Output pin; all are 5.0V operation.

Chapter 3. AP33771C EVB Descriptions

3.1 EVB Schematics

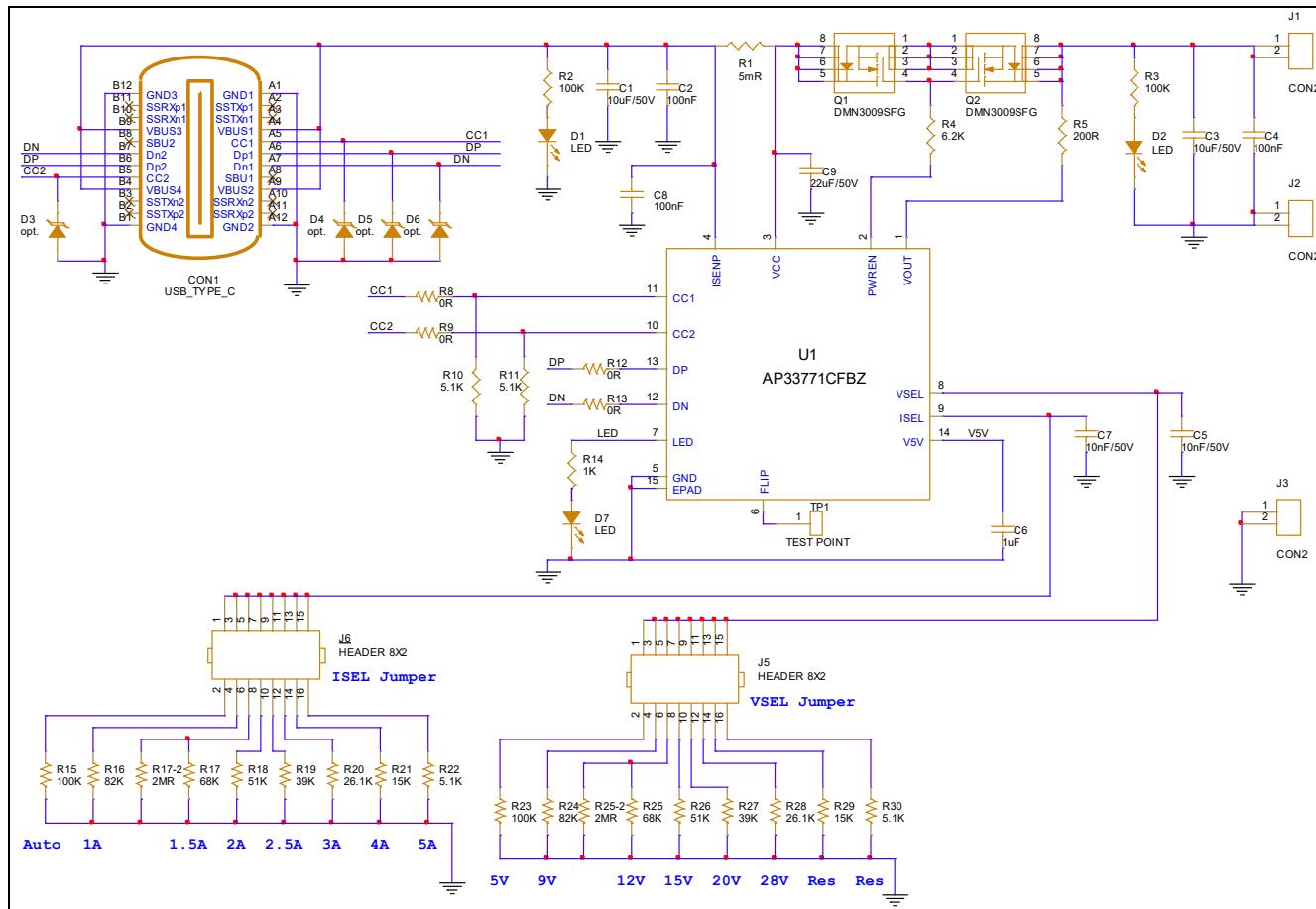


Figure 3 – Schematics of the AP33771C Evaluation Board

The AP33771C, a USB Type-C PD sink controller, is used to request power from an attached USB PD source adaptor through simple external resistor settings. The AP33771C EVB schematic is shown in Figure 3.

The voltage and current requests are expressed by appropriate resistors connected to the VSEL and ISEL pins, respectively. After initializing power-on, the AP33771C automatically evaluates all PDOs from the PD source capability and finds the matched PDO according to its internal matching criteria. If part of the PDO is matched, the MOS switch is turned on to connect VBUS to VOUT.

The AP33771C supports dead-battery functionality and can be woken up as soon as an active PD adaptor is plugged into the TCD's USB Type-C receptacle. After the power link is set up between the source and sink, OVP, UVP, and OCP protections are enabled to monitor the power-charging status. In addition, moisture detection between DP and DN is implemented during cable insertion. In case power protection is triggered, the AP33771C shuts down the VOUT enable NMOS switch and discharges the VOUT voltage. Meanwhile, the AP33771C provides an LED indication for the system's operating status and supports FLIP indication of the USB-C attachment.

3.2 EVB TOP View

The AP33771C EVB is illustrated in Figure 4 using 50mm x 25mm dimensions, with key portions listed below:

- VOUT connection
- Voltage and current selection
- LED indications for system status
- CC flip indication pin
- LED indication of VBUS and VOUT

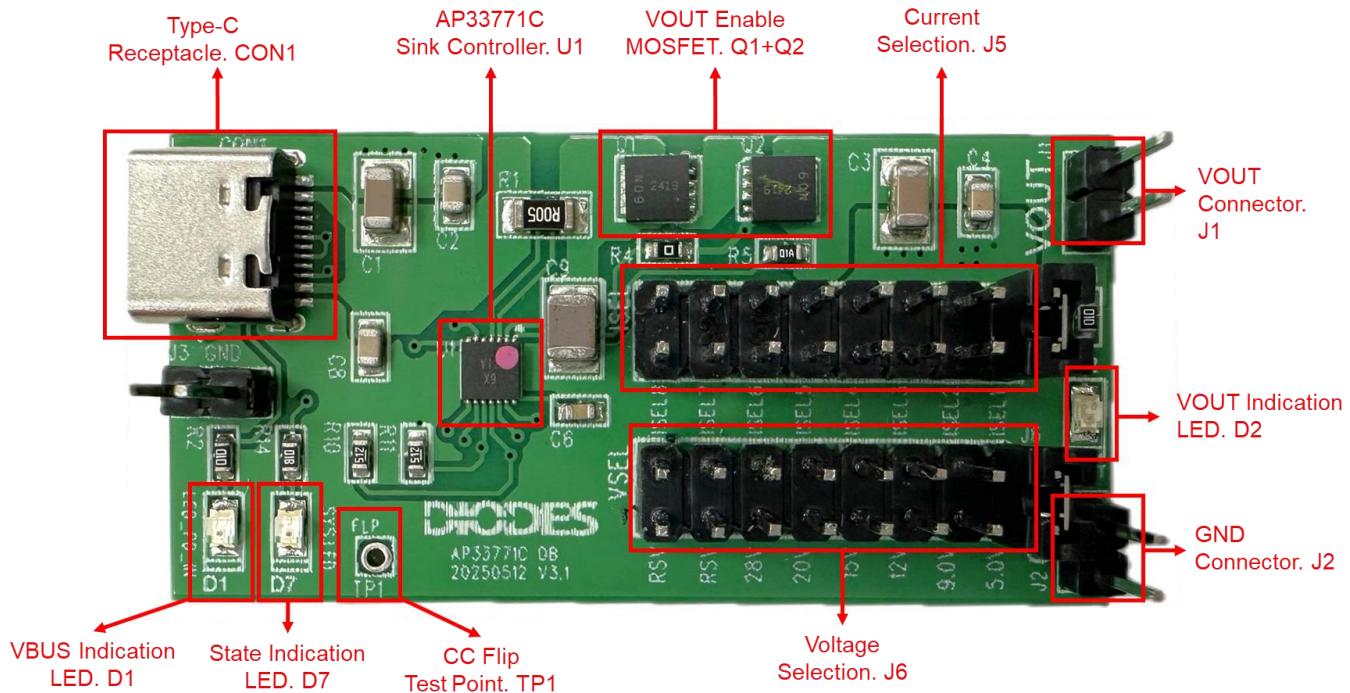


Figure 4 – AP33771C Evaluation Board top view and its key portions

3.3 EVB Quick Setup

Steps for quick setup are shown in Figure 6.

Step 1: Connect resistor-setting jumpers (J6); for example, setting up 20V2A.

Step 2: Connect J1/J2 to a load.

Step 3: Connect the Type-C connector to a USB PD adaptor (PDC), and power on the EVB with the USB PD adaptor (D2/D7 will illuminate).

The AP33771C Evaluation Board will output the requested voltage and current on the load after the above steps.

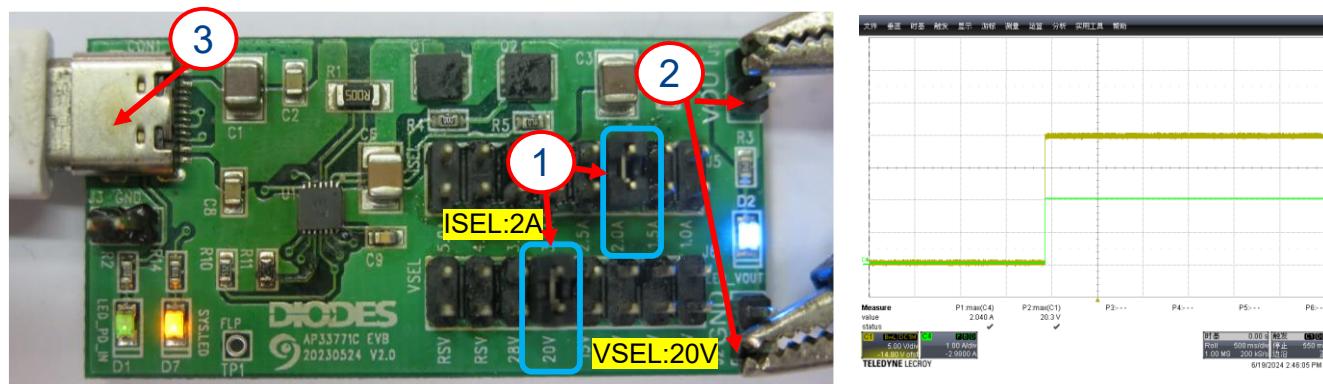


Figure 5 – AP33771C EVB setup sequence

3.4 EVB Function Description

Jumper Locations

The AP33771C EVB provides users a simple resistor-setting through jumpers, which enables USB PD negotiation between the TCD device and an external PDC. If the negotiation is successful, the PDC delivers the requested voltage and current to the TCD device through VBUS in the USB-C cable. If negotiation is not successful, the PDC goes back to 5V PDO. During the evaluation, VOUT can be connected to a load to check the current negotiation result. The jumpers on the EVB are listed in Table 2 below.

Location	Function
J1	VOUT Connector for External Load
J5	Voltage Selection Jump
J6	Current Selection Jump

Table 2 – Jumpers and functions of the Evaluation Board

Voltage and Current Selections

VSEL and ISEL settings determine the selected voltage and current to negotiate with the power source. The mapping between the VSEL/ISEL's amplitudes and resistance values are illustrated in Table 3 below, where it is suggested to use the resistors with 1% accuracy.

Voltage Selection								
Index(J6)	1	2	3	4	5	6	7	8
VSEL	5V	9V	12V	15V	20V	28V	Reserved	Reserved
Resistance (KΩ)	100	82	66	52	39	26	15	5.1
Resistor	R23	R24	R25	R26	R27	R28	R29	R30
Current Selection								
Index(J5)	1	2	3	4	5	6	7	8
ISEL	Auto	1A	1.5A	2A	2.5A	3A	4A	5A
Resistance (KΩ)	100	82	66	52	39	26	15	5.1
Resistor	R15	R16	R17	R18	R19	R20	R21	R22

Table 3 – Voltage selection and current selection versus J5 and J6 connector settings

During the AP33771C's voltage-selection process, the Extended Power Range (EPR) has priority over the Standard Power Range (SPR). The Adjustable Voltage Supply (AVS) and Programmable Power Supply (PPS) PDOs also have priority over Fixed PDOs. This reminds system designers that if the current requirement is greater than 3A, a suitable e-Marker cable with over 3A current rating is necessary.

LED for System State Indication

The AP33771C's LED pin is used to reflect the system's states. Below, Table 4 summarizes the LED indications and VOUT ON/OFF for each corresponding state.

State	LED Indication	VOUT	Comments
INIT	NA	OFF	During VBUS/Rd attachment and AP33771C initialization
CHARGING	4-sec Breathing	ON	Successful negotiation or entering Non-PD Mode; charging start
MISMATCH	Full Light	OFF	Voltage or current mismatch
MOISTURE	2-sec Flicker	OFF	DP/DN abnormal impedance detected
FAULT	0.6-sec Flicker	OFF	OVP, OCP, or UVP occurrence

Table 4 – LED Indications of System States

CC Flip Test Point

The AP33771C uses the FLIP pin for CC flip indication, as shown in Table 5 below. If the CC is not flipped, the FLIP pin output is low. If the CC is flipped, the FLIP pin output is high.

CC Flip Indication		
CC Detection	CC1 Detected	CC2 Detected
FLIP Output	0 (Low)	1 (High)

Table 5 – CC Flip Indication

LEDs for VBUS and VOUT Indications

The AP33771C uses LEDs, D1 and D7, for VBUS and VOUT state indications respectively.

D1's on or off status indicates whether the USB PDC power is delivered to VBUS. D7's on or off status indicates if the VBUS power is switched to VOUT for load consumption.

3.5 EVB System BOM

The BOM list of the EVB schematic is shown in Table 6 below.

Item	Quantity	Reference	Part
1	1	CON1	USB_TYPE_C(MUSB12-01-247)
2	3	C1,C3	10uF/50V
3	3	C2,C4,C8	100nF/50V
4	2	C5,C7	10nF/50V
5	1	C6	1uF/50V
6	1	C9	22uF/35V
7	1	D1	LED
8	1	D2	LED
9	1	D7	LED
10	4	D3,D4,D5,D6	NC
11	2	Q1,Q2	DMN3009SFG
12	1	R1	5mR
13	4	R2,R3,R15,R23	100K
14	4	R8,R9,R12,R13	0R
15	1	R4	6.2K
16	1	R5	200R
17	4	R10,R11,R22,R30	5.1K
18	1	R14	1K
19	2	R16,R24	82K
20	2	R17,R25	68K
21	2	R18,R26	51K
22	2	R19,R27	39K
23	2	R20,R28	26.1K
24	2	R21,R29	15K
25	2	R17-2,R25-2	2M
26	1	TP1	TEST POINT
27	1	U1	AP33771CFBZ-13-FA02
28	3	J1,J2,J3	CON2
29	2	J6,J5	HEADER 8X2

Table 6 – BOM list of the AP33771C EVB's schematics

Chapter 4. USB PD Source-to-Sink Application Examples

Figure 6 and usage cases 1-6 show the different scenarios and procedures of the TCD's power profile request from a PDC power source.

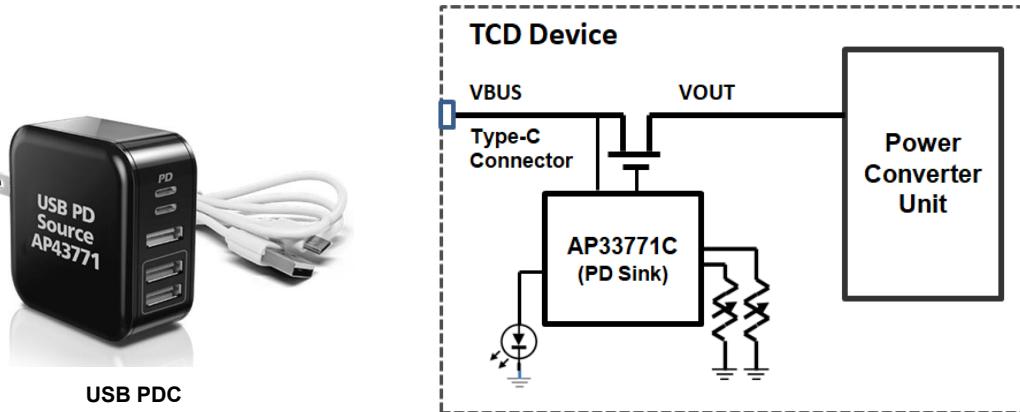


Figure 6 – The application scenarios are based on a typical TCD device requesting power profile from a USB PDC

Case 1:	PDC=45W PDO: APDO: 5V/3A 3.3V~21V/1A 9V/3A 15V~28V/45W 12V/2.5A 15V/2A 20V/1.5A 28V/1.5A	TCD = 28V and 1.5A VSEL= 28V RVSEL= 26KΩ VBUS = 28V ISEL=1.5A RISEL= 82KΩ VOUT = 28V
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A TCD requests 28V and 1.5A from a given 45W PDC source with fixed PDOs: 5V/3A, 9V/3A, 12V/2.5A, 15V/2A, 20V/1.5A, 28V/1.5A, 3.3V~21V/1A, 15V~28V/45W.

Step 1: set VSEL to “26KΩ” to get 28V, set ISEL to “82KΩ” to get 1.5A.

Step 2: AP33771C starts to handshake with the powered PDC as soon as a Type-C cable is connected.

Step 3: according to Matching Mechanism, APDO 15V~28V/45W can match ISEL.

Step 4: VOUT = 28V, because VSEL and ISEL are all matched, then the MOS switches are enabled.

Case 2:	PDC=56W PDO: APDO: 5V/3A 3.3V~21V/1A 9V/3A 15V~28V/45W 12V/2.5A 15V/2A 20V/1.5A 28V/2A	TCD = 28V and 2A VSEL= 28V RVSEL= 26KΩ VBUS = 28V ISEL= 2A RISEL= 66KΩ VOUT = 28V
---------	---	---

TCD requests 28V and 2A from a given 56W PDC source with fixed PDOs: 5V/3A, 9V/3A, 12V/2.5A, 15V/2A, 20V/1.5A, 28V/2A, 3.3V~21V/1A, 15V~28V/45W.

Step 1: set VSEL to “26KΩ” to get 28V, set ISEL to “66KΩ” to get 2A.

Step 2: AP33771C starts to handshake with the powered PDC as soon as a Type-C cable is connected.

Step 3: according to Matching Mechanism, APDO can't match ISEL, search Fixed PDOs.

Step 4: VOUT = 28V, because VSEL and ISEL are all matched, then the MOS switches are enabled.

Case 3:	PDC=45W	TCD = 28V and 2A
PDO:	APDO:	
5V/3A	3.3V~21V/1A	VSEL= 28V Rvsel= 26KΩ VBUS = 15V
9V/3A	15V~28V/45W	ISEL= 2A RISEL= 66KΩ VOUT = 15V
12V/2.5A		
15V/2A		
20V/1.5A		
28V/1.5A		

TCD requests 28V and 2A from a given 45W PDC source with fixed PDOs: 5V/3A, 9V/3A, 12V/2.5A, 15V/2A, 20V/1.5A, 28V/1.5A, 3.3V~21V/1A, 15V~28V/45W.

Step 1: set VSEL to “26KΩ” to get 28V, set ISEL to “66KΩ” to get 2A.

Step 2: AP33771C starts to handshake with the powered PDC as soon as a Type-C cable is connected.

Step 3: according to Matching Mechanism, 28V can't match ISEL, search for PDOs below 28V.

Step 4: VOUT = 15V, because 15V/2A can match ISEL request, then the MOS switches are enabled.

Case 4:	PDC=45W	TCD = 28V and 2.5A
PDO:	APDO:	
5V/3A	3.3V~21V/1A	VSEL= 28V Rvsel= 26KΩ VBUS = 12V
9V/3A	15V~28V/45W	ISEL= 2.5A RISEL= 52KΩ VOUT = 12V
12V/2.5A		
15V/2A		
20V/1.5A		
28V/1.5A		

TCD requests 28V and 2.5A from a given 45W PDC source with fixed PDOs: 5V/3A, 9V/3A, 12V/2.5A, 15V/2A, 20V/1.5A, 28V/1.5A, 3.3V~21V/1A, 15V~28V/45W.

Step 1: set VSEL to “26KΩ” to get 28V, set ISEL to “52KΩ” to get 2.5A.

Step 2: AP33771C starts to handshake with the powered PDC as soon as a Type-C cable is connected.

Step 3: according to Matching Mechanism, 28V can't match ISEL, search for PDOs below 28V.

Step 4: VOUT = 12V, because 12V/2.5A can match ISEL request, then the MOS switches are enabled.

Case 5:	PDC=45W	TCD = 28V and 3A
PDO:	APDO:	
5V/3A	3.3V~21V/1A	VSEL= 28V RVSEL= 26KΩ VBUS = 9V
9V/3A	15V~28V/45W	ISEL= 3A RISEL= 39KΩ VOUT = 9V
12V/2.5A		
15V/2A		
20V/1.5A		
28V/1.5A		

TCD requests 28V and 3A from a given 45W PDC source with fixed PDOs: 5V/3A, 9V/3A, 12V/2.5A, 15V/2A, 20V/1.5A, 28V/1.5A, 3.3V~21V/1A, 15V~28V/45W.

Step 1: set VSEL to “26KΩ” to get 28V, set ISEL to “39KΩ” to get 3A.

Step 2: AP33771C starts to handshake with the powered PDC as soon as a Type-C cable is connected.

Step 3: according to Matching Mechanism, 28V can't match ISEL, search for PDOs below 28V.

Step 4: VOUT = 9V, because 9V/3A can match ISEL request, then the MOS switches are enabled.

Case 6:	PDC=45W	TCD = 28V and 3.5A
PDO:	APDO:	
5V/3A	3.3V~21V/1A	VSEL= 28V RVSEL= 26KΩ VBUS = 5V
9V/3A	15V~28V/45W	ISEL= 3.5A RISEL= 26KΩ VOUT = 0V
12V/2.5A		
15V/2A		
20V/1.5A		
28V/1.5A		

TCD requests 28V and 3.5A from a given 45W PDC source with fixed PDOs: 5V/3A, 9V/3A, 12V/2.5A, 15V/2A, 20V/1.5A, 28V/1.5A, 3.3V~21V/1A, 15V~28V/45W.

Step 1: set VSEL to “26KΩ” to get 28V, set ISEL to “26KΩ” to get 3.5A.

Step 2: AP33771C starts to handshake with the powered PDC as soon as a Type-C cable is connected.

Step 3: according to Matching Mechanism, 28V can't match ISEL, search for PDOs below 28V.

Step 4: VOUT = 0V, because all PDOs can't match ISEL, then the MOS switches are disabled.

Chapter 5. Compliance test

The AP33771C EVB passes all test items in the Ellisys USB-PD Compliance tester, as shown in Figure 7 below.

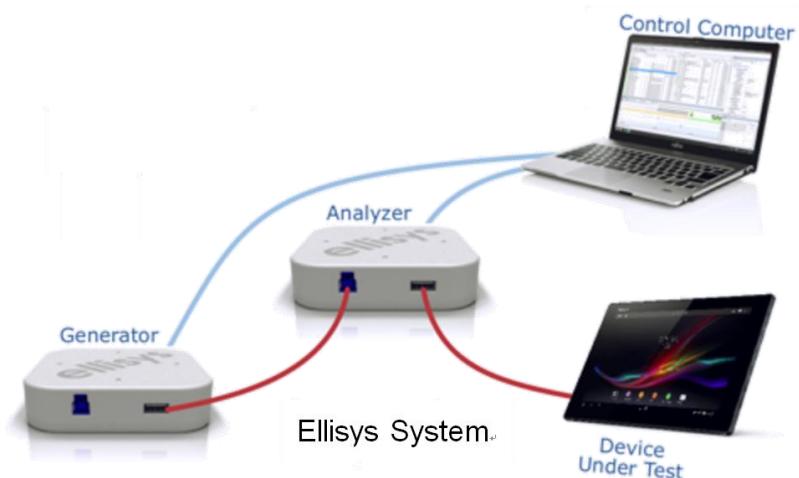
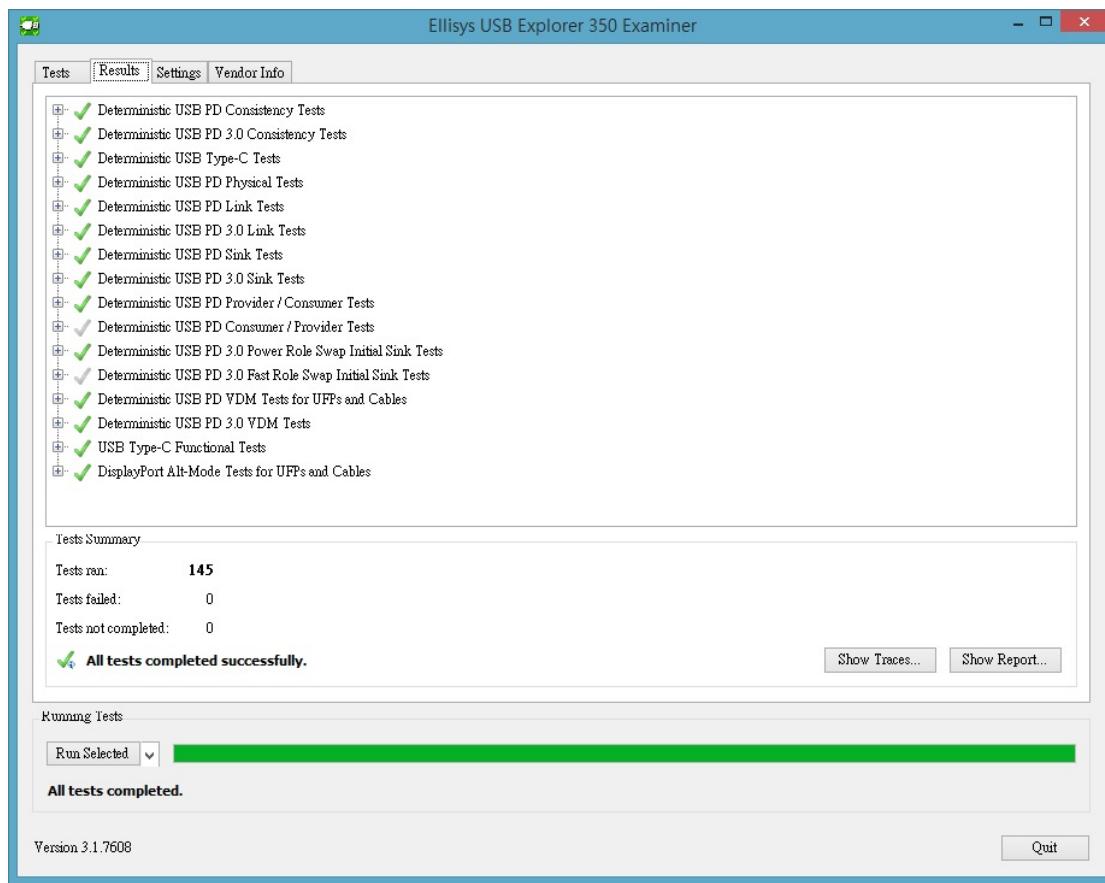


Figure 7 – Ellisys USB PD test environment and test item list

Chapter 6. Design Considerations

6.1 Termination of CC1/CC2 channels

Since the AP33771C has no internal R_d resistor embedded, the designer must place a $5.1K\ \Omega$ resistor on both CC1 and CC2 to GND, as shown in Figure 8 below. A lack of any R_d will cause the AP33771C to misrecognize the direction of the CC, and will not enter the PD negotiation process.

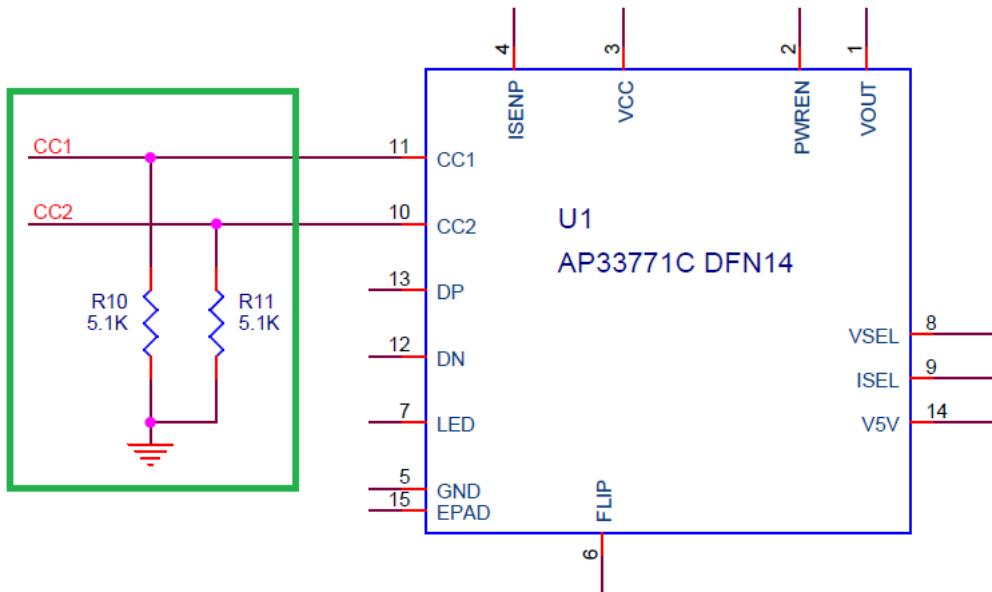


Figure 8 – Make sure the connection of external R_d resistors on CC1 and CC2

6.2 ESD Considerations

The AP33771C EVB is designed for functional evaluation without an ESD protection component on board. Do not use the AP33771C EVB to test ESD. For manufacturing, users must consider adding suitable ESD protection devices or optimize their PCB designs.

Chapter 7. Revision History

Revision	Issue Date	Comment
1.0	11/16/2023	Initial Release

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