Description

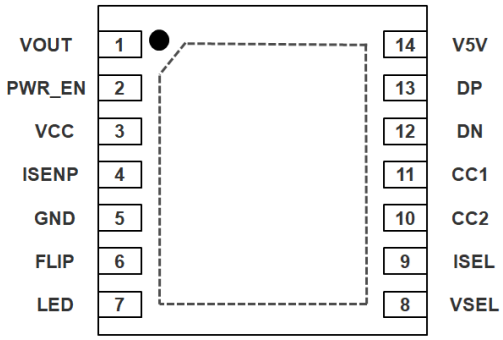
The AP33771C is a highly integrated USB Type-C® PD3.1 sink controller to support Extended Power Range (EPR)/Adjustable Voltage Supply (AVS) up to 28V and Standard Power Range (SPR)/ Programmable Power Supply (PPS) up to 21V. The device is targeted for DC power request and control for Type-C Connector-equipped Devices (TCDs) through simple external resistor setting.

For a simple TCD without a system MCU, the AP33771C initiates desired power request based on resistance values connected on the VSEL pin (voltage) and ISEL pin (current), after Power-On Reset (POR), see Table 2 for details.

The AP33771C offers short protection between CC1/CC2 pins to adjacent high-voltage pin up to 34V. Smart built-in firmware of the AP33771C offers comprehensive safety protection schemes, including overvoltage protection (OVP), undervoltage protection (UVP), overcurrent protection (OCP), overtemperature protection (OTP), and moisture detection of the Type-C connector. An LED indicator is used to show the PD power negotiation status. The automatic cable voltage drop compensation is implemented to cover practical usage situations. The AP33771C can also indicate the insertion orientation of the Type-C attachment.

Pin Assignments

(Top View)



W-DFN3030-14 (Type A1)

Features

- USB PD3.1 v1.6 Certified with TID: 9960
- Operating Voltage Range of VCC: 3V to 31V
- Supports PD3.1 EPR/AVS up to 28V and SPR/PPS up to 21V
- Voltage/Current Selections Through Resistors Settings
- Support FLIP Indication of the Type-C Attachment
- Support OVP with Hard Reset and Auto Restart
- Support UVP, OCP, and OTP with Output Latch Off
- Driver for Output Enable nMOS Switch
- Supports Dead Battery Function
- Automatic Cable Voltage Drop Compensation
- VBUS Short Protection on CC1/CC2 Pins up to 34V
- Support Moisture Detection of the Type-C Connector
- LED Indication for Different Negotiation Results
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

- USB Type-C connector-equipped battery-powered devices
- USB Type-C connector-equipped DC-power input devices
- USB PD3.1 testers

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Application Circuit

The AP33771C, a USB Type-C power delivery sink controller, is used to request power from an attached USB PD source adapter through simple external resistor settings, as shown in Figure 1 below.

After the POR initialization, the voltage and current requests are set according to resistors connected to VSEL and ISEL pins, respectively. The AP33771C automatically evaluates all PDOs from PD Source capability and finds the matched PDO according to its internal matching criteria, see Table 3 for details. If some of the PDO is matched, the MOS switch is turned on to connect VBUS to VOUT.

The AP33771C supports the dead battery function, and can be woken up as soon as a PD adapter is plugged in the TCD Type-C receptacle. After the power link is set up between the source and sink, OVP, UVP, and OCP protections are enabled to monitor the power charging status. In addition, moisture detection between the signal line and ground is implemented during the cable insertion. In case power protection is triggered, the AP33771C shuts down the VOUT enable nMOS switch, to disconnect VBUS from VOUT. The AP33771C provides an LED indication for the system operating status and supports FLIP indication of the Type-C attachment orientation.

The AP33771C supports Type-C PD compliance charger (through Type-C to Type-C cable) or legacy Type-A charger (through Type-A to Type-C cable). The automatic cable voltage drop compensation is implemented to cover practical usage situations for TCDs as well.

The back-to-back nMOS switches shown in Figure 1 could be simplified to a simple nMOS switch for the TCD when there is no concern on reverse current from power module back to VBUS.

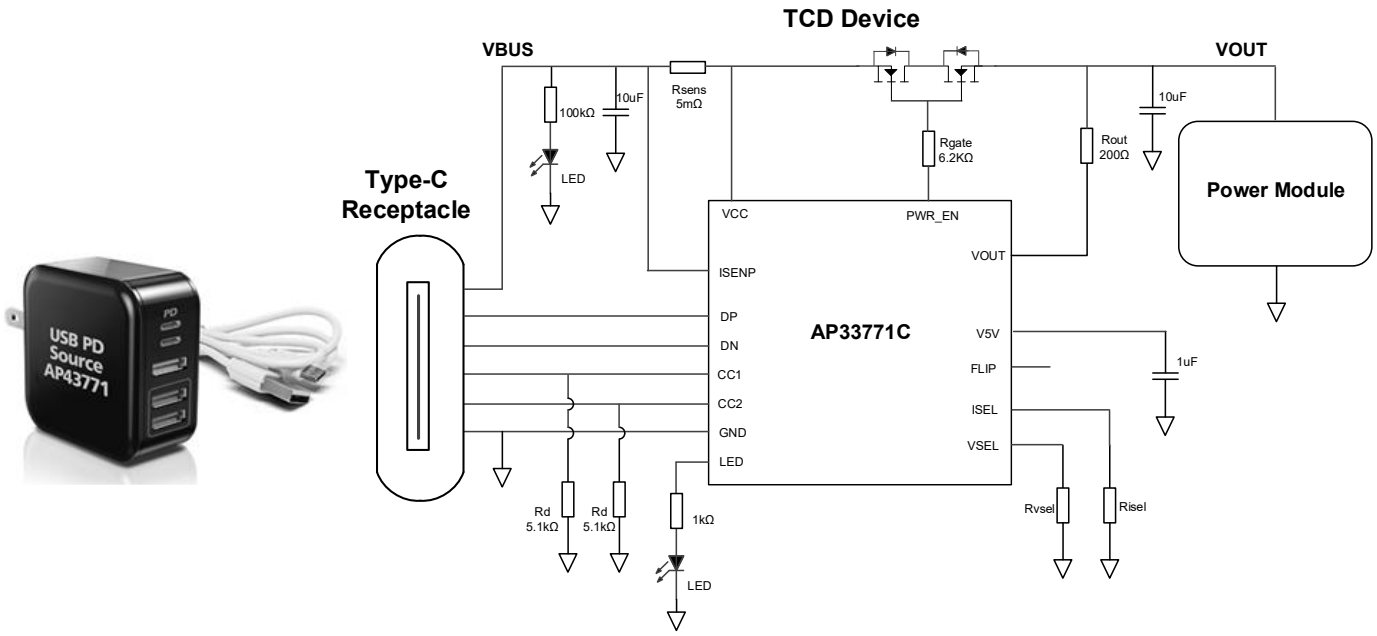


Figure 1. Typical System Configuration of AP33771C PD3.1 Sink Controller in a TCD

Pin Descriptions

Pin No.	Pin Name	Type (Note 4)	Function
1	VOUT	AHV	Terminal for VOUT Monitoring.
2	PWR_EN	AHV	To Control External VOUT. Connected to external nMOS switch, ON (High) or OFF (Low).
3	VCC	AHV	The Power Supply of the AP33771C. A 1μF cap is required to connect this pin to GND pin.
4	ISENP	AHV	Current Sense Positive Node.
5	GND	GND	Ground
6	FLIP	DO	Flip Indicator of Type-C Plug. Is low if CC is connected to CC1 and high if connected to CC2.
7	LED	DO	LED Indicator of the System Status
8	VSEL	AI	Voltage selection pin, connect resistance to ground to set Voltage.
9	ISEL	AI	Current selection pin, connect resistance to ground to set Current.
10	CC2	AIO	Type-C Configuration Channel 2
11	CC1	AIO	Type-C Configuration Channel 1
12	DN	AIO	USB 2.0 Data Negative Node
13	DP	AIO	USB 2.0 Data Positive Node
14	V5V	AP	5V LDO output if VCC is on. A 1μF cap is required to connect this pin to GND.
—	EPAD	GND	Exposed pad is suggested to connect to Ground

Note: 4. AHV – Analog High Voltage pin.
AP – Power for Analog Circuit and Analog Input/Output pins, 5.0V operation.
AI – Analog Input pin.
AIO – Analog Input/Output pin. DP/DN & CC1/CC2 are 3.3V operation.
DO – Digital Output pin. All are 5.0V operation.

Table 1. Pin Descriptions of AP33771C Sink Controller

Functional Block Diagram

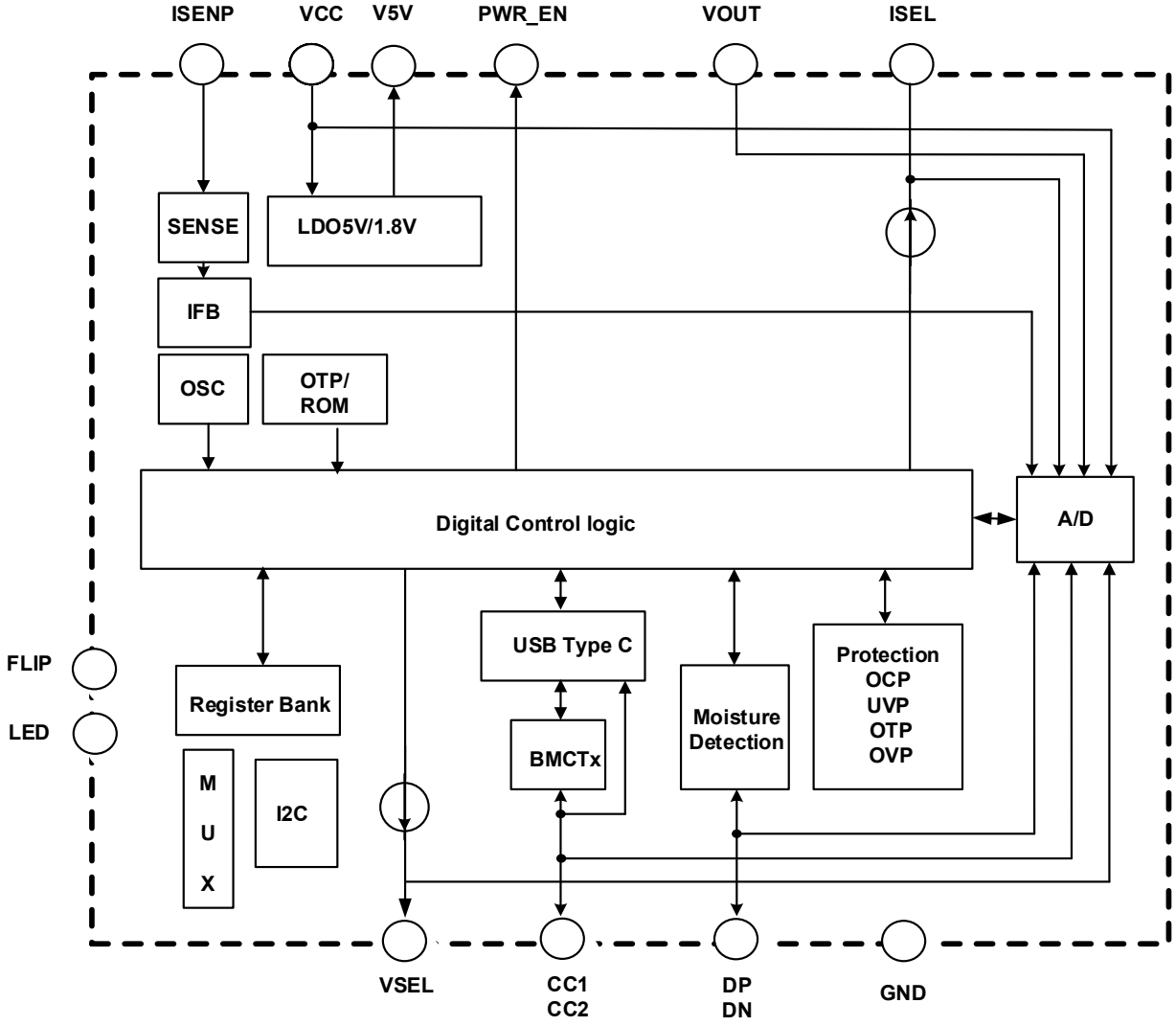


Figure 2. The Functional Block Diagram of AP33771C PD3.1 Sink Controller

Absolute Maximum Ratings (Note 5)

Symbol	Parameter	Rating	Unit
V_{VCC}	Input Voltage at VCC Pin	-0.3 to 34	V
V_{V5V}	Input Voltage at V5V Pin	-0.3 to 7	V
V_{VSEL}, V_{ISEL}, V_{LED}, V_{FLIP}	Input Voltage at VSEL, ISEL, LED, FLIP Pins	-0.3 to 7	V
V_{VOUT}, V_{ISENP}	Input Voltage at VOUT, ISENP Pins	-0.3 to 31	V
V_{PWR_EN}	Input Voltage at PWR_EN Pin	-0.3 to 38	V
—	Voltage from PWR_EN to VCC Pin	-30 to 4	V
V_{CC1}, V_{CC2}	Input Voltage at CC1, CC2 Pins	-0.3 to 34	V
V_{DP}, V_{DN}	Input Voltage at DN, DP Pins	-0.3 to 7	V
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering, 10s)	+300	°C
ESD	Human Body Model	2	kV
ESD	Charged Device Model	750	V

Note: 5. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

Package Thermal Information (Note 6)

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	50.04	°C/W
$R_{\theta JC(top)}$	Junction-to-Case (Top) Thermal Resistance	34.80	°C/W
$R_{\theta JB}$	Junction-to-Board Thermal Resistance	30.82	°C/W
Ψ_{JT}	Junction-to-Top Characterization Parameter	2.04	°C/W
Ψ_{JB}	Junction-to-Board Characterization Parameter	29.89	°C/W
$R_{\theta JC(bot)}$	Junction-to-Case (Bottom) Thermal Resistance	20.33	°C/W

Note: 6. Test condition: device mounted on FR-4 substrate PC board, 2oz copper, with the minimum footprint.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{VCC}	Power Supply Voltage at VCC Pin	3.3	31	V
V_{V5V}	Input Voltage at V5V Pin	4.37	5.33	V
V_{DP}, V_{DN}	Input Voltage at DP, DN Pins	2.75	3.25	V
T_J	Junction Temperature Range	-40	+125	°C
T_A	Operating Ambient Temperature	-40	+85	°C

Electrical Characteristics (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC SECTION						
V_{ST}	Startup Voltage	—	2.5	2.8	3.5	V
V_{UVLO}	Minimum Operating Voltage	—	2.3	2.7	3	V
V_{VCC_HYS}	VCC Hysteresis (V_{ST}-V_{UVLO})	—	0.05	—	—	V
I_{VCC_OPR}	Operating Supply Current	V_{VCC} = 5V	—	3.3	6	mA
CC1/CC2 SECTION						
V_{L_RD3A}	Low-Voltage Threshold Used to Distinguish R_D Attached or Detached for 3A Delivery	—	—	1.35	—	V
V_{H_RD3A}	High-Voltage Threshold Used to Distinguish R_D Attached or Detached for 3A Delivery	—	—	2.0	—	V
VOLTAGE SELECTION AND CURRENT SELECTION						
I_{VSEL}	VSEL Current Source (Note 7)	—	—	20.5	—	μA
I_{VSEL_Range}	VSEL Current Source Range (Note 7)	—	-5	—	+3	%
I_{ISEL}	ISEL Current Source (Note 7)	—	—	20	—	μA
I_{ISEL_Range}	ISEL Current Source Range (Note 7)	—	-5	—	+3	%
FLIP and LED SECTION						
V_O	FLIP, LED Output Voltage Range (Note 7)	V_{VCC} = 5V	4.37	4.85	5.33	V
I_{SS}	FLIP, LED Sink/Source Capability (Note 7)	—	2	—	—	mA
PROTECTION FUNCTION SECTION						
V_{OVP5V}	OVP_5V Enable Voltage (Notes 7, 8)	—	—	7	—	V
V_{OVP20V}	OVP_20V Enable Voltage (Notes 7, 8)	—	—	22	—	V
V_{OVP28V}	OVP_28V Enable Voltage (Notes 7, 8)	—	—	30	—	V
$t_{DEBOUNCE\_OVP}$	OVP Debounce Time (Note 9)	—	—	30	—	ms
t_{OV_DELAY}	Delay from OVP Threshold Trip to nMOS Gate Turn-Off (Note 7)	—	—	—	50	ms
T_{OTP}	Internal OTP Temperature	—	—	+130	—	°C
V5V SECTION						
V_{V5V}	V5V Output Range	—	4.37	4.85	5.33	V
I_{V5V}	V5V Source Capability	—	—	30	—	mA

Notes: 7. Guaranteed by design.
8. OVP setting @PDO +2V.
9. OVP blanking time during V_O transition from high output voltage to low output voltage, such as 9V to 5V, or 12V to 5V.

Functional Description

Overview

The AP33771C, a highly integrated USB Type-C PD3.1 sink controller, supports EPR/AVS up to 28V and provides SPR/PPS up to 21V. The device is targeted for DC power request and control for flexible Type-C Connector-equipped Devices (TCDs) without an embedded host MCU. The AP33771C generates a Request Data Object (RDO) of voltage and current through resistor settings in VSEL and ISEL pins, and automatically initiates the PD negotiation process with the attached Type-C PD compliance charger (through Type-C to Type-C cable) or legacy Type-A charger (through Type-A to Type-C cable) after the POR initialization.

VCC and VOUT

VCC pin is the power supply input of the AP33771C, which is derived from the VBUS output of the PD source. A low pass filter or capacitor decoupling on VCC pin is suggested.

The AP33771C monitors the output voltage at VOUT pin, which is connected to the nMOS switch output. A 200Ω resistor between MOS output and AP33771C VOUT pin is required, to limit the discharge current.

CC1/CC2 Connection and FLIP Indication

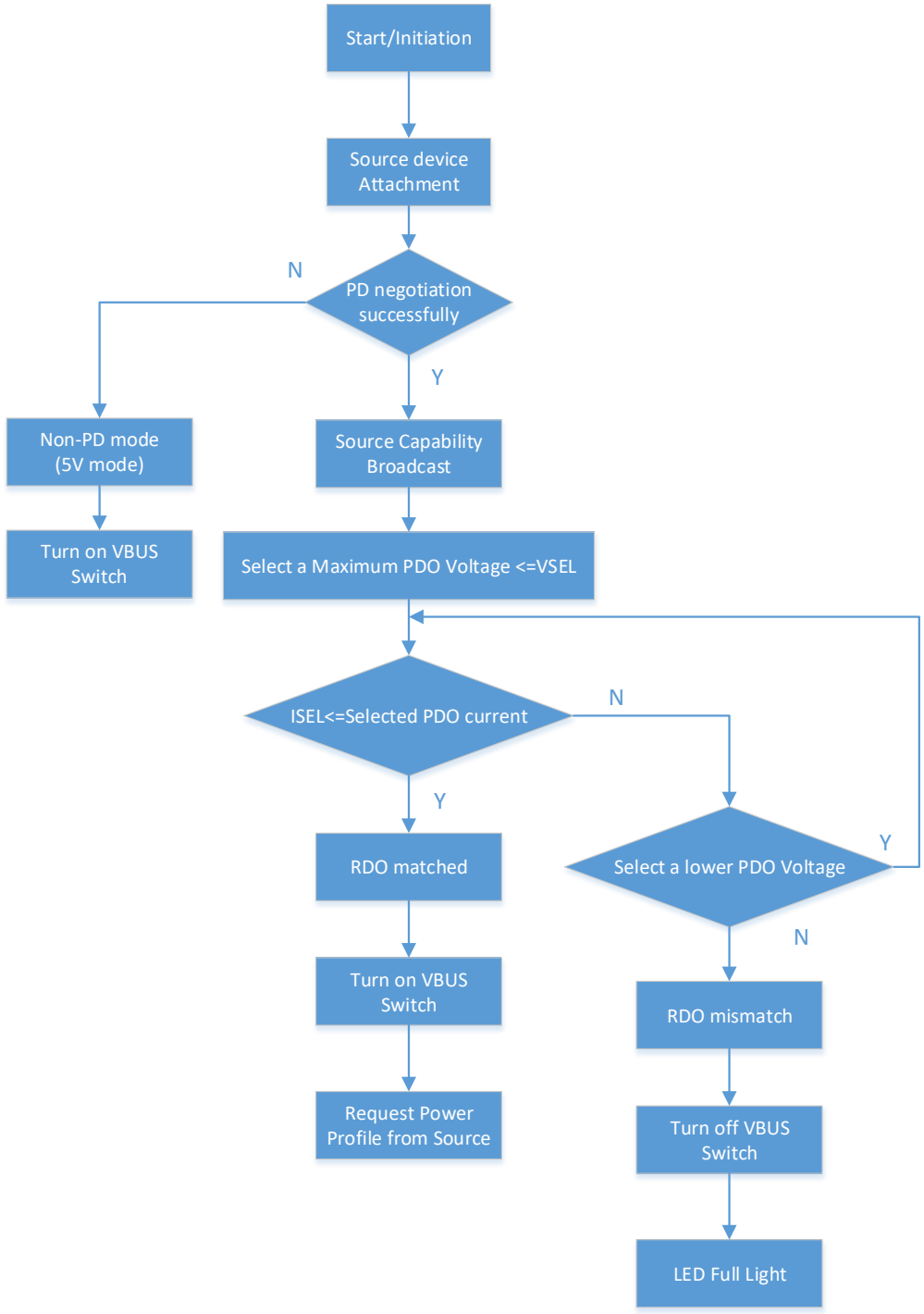
The Configuration Channel pins (CC1/CC2) are used for connection and attachment detection, plug orientation determination and system configuration. As soon as the PD source adapter is plugged into the AP33771C-embedded TCD device, one of the CC pins will be pulled down through Rd resistor connect on the pins and the CC/VCONN connection and data path routing are established accordingly. At the same time, the source adapter enables VBUS and VCONN power supply and then starts broadcasting PD source capabilities and PD negotiation through CC pin, which is connected to the internal Bi-phase Mark Code (BMC) block.

During the cable attachment, the configuration information and source capabilities are stored in the AP33771C internal registers. The AP33771C uses FLIP pin for CC flip indication. If CC is connected to CC1 (non-flipped), the FLIP output is low. If CC is connected to CC2 (flipped), the FLIP output is high.

Functional Description (continued)

Power Policy Management Flowchart

Below is the power policy management flowchart of AP33771C. Any source side power device connected to AP33771C, AP33771C will follow this flow to handle power requests and related actions.



Functional Description (continued)

Sink RDO Selection

The AP33771C sink controller generates a RDO of voltage and current to negotiate a power profile with a PD source controller. The voltage and current values are determined from the hardware setting. With the constant current source output from the VSEL and ISEL pins, system designers can connect suitable resistors, and the AP33771C measures the voltage levels at these 2 pins through internal ADC. Up to eight resistors are supported both for voltage and current selections. It is recommended to use the resistors with ±1% accuracy or better, to connect to the VSEL and ISEL pins to ensure the request selection. The mapping between VSEL/ISEL selection and resistance values are illustrated in Table 2 below. It reminds system designers that if current requirement is greater than 3A, a suitable e-Marker cable with over 3A current rating is needed. While "Auto" is selected, sink controller will request PDO by VSEL only.

Index	1	2	3	4	5	6	7	8
VSEL	5V	9V	12V	15V	20V	28V	Reserved	Reserved
R_{VSEL} (kΩ, 1%)	100	82	66	52	39	26	15	5.1
ISEL (AP33771CFBZ-13-FA01)	1A	1.5A	2A	2.5A	3A	3.5A	4A	5A
ISEL (AP33771CFBZ-13-FA02)	Auto	1A	1.5A	2A	2.5A	3A	4A	5A
R_{ISEL} (kΩ, 1%)	100	82	66	52	39	26	15	5.1

Table 2. The Mapping Between VSEL/ISEL Amplitudes and Resistance Values

Matching Mechanism

After the POR initiation, the AP33771C starts the PD negotiation with the external PD source. All of the source capability information is received and stored into its internal registers during the handshake. The matching mechanism of PDO selection used in AP33771C is summarized in Table 3, where voltage matching is performed first, and then current matching is proceeded in case voltage match happens.

Source PDO	Voltage Match Criteria (Note 10)	Current Match Criteria (Note 10)
Fixed PDO	$V_{VSELMIN} \le V_{FIXED} \le V_{VSEL}$	$I_{ISEL} \le I_{MAX}$
PPS APDO	$V_{MIN} \le V_{VSEL} \le V_{MAX}$	$I_{ISEL} \le I_{MAX}$
AVS APDO	$V_{MIN} \le V_{VSEL} \le V_{MAX}$	$V_{VSEL} \times I_{ISEL} \le PDP$

Note: 10. V_{VSEL} : Voltage selected by V_{SEL} pin
I_{ISEL} : Current selected by ISEL pin
V_{FIXED} : Voltage of Fixed PDO
V_{MIN} : Minimum voltage of PPS/AVS PDO
V_{MAX} : Maximum voltage of PPS/AVS PDO
I_{MAX} : Maximum current of PDO
PDP : Output power of AVS PDO (W)
$V_{VSELMIN}$: Predetermined minimum value of V_{VSEL}

Table 3. RDO Matching Mechanism used in the AP33771C Sink Controller

If the PD source supports EPR mode and VSEL is set ≥ 28V, the AP33771C will enter EPR mode and enable EPR request first. If more than one PDO are matched, the PPS/AVS PDOs have higher priority over the fixed PDOs. If more than one PPS/AVS PDO are matched, the PDO with the lowest voltage takes precedence over the others. Typically, higher PPS/AVS voltages are accompanied by lower I_{MAX} currents.

During the voltage matching of fixed PDO, the selection criterion is to select the PDO closest to V_{VSEL} in descending order from the PDOs equal to V_{VSEL}. The fixed PDO selection has a lower limit, $V_{VSELMIM}$, which is a predetermined parameter during firmware programming. If the selected fixed PDO is lower than $V_{VSELMIN}$ the system enters the mismatch state. For the AP33771C, the predetermined value of $V_{VSELMIN}$ is set to 5V.

After voltage matching process is completed, the PDOs that meet the voltage matching criteria will perform current matching flow again. During the current matching process, fixed PDO or PPS APDO with I_{MAX} greater than I_{ISEL} will be selected, and AVS APDO with PDP greater than $V_{VSEL} \times I_{ISEL}$ will be selected.

During the PD handshake between the TCD and the external PD source, the AP33771C acquires and stores source capability into relevant registers. If there are valid source capabilities that match with the RDO selection before timeout, the AP33771C policy engine then requests a suitable power profile from the source adapter. If there is still no valid source capability matched to the RDO after timeout, the AP33771C indicates mismatch information through the LED indicator, see Table 5 for details.

Functional Description (continued)

NMOS VOUT Enable Switch

Taking VBUS voltage as input, the built-in charge-pump circuit generates a high-voltage gate driver (PWR_EN) to drive an external high-side nMOS switch. A 6.2kΩ resistance is suggested to connect the PWR_EN to the nMOS gate. Once the PDO negotiations are matched between source side and sink side, PWR_EN goes high and enables the nMOS switch and VBUS is connected to VOUT. Otherwise, PWR_EN will remain low, the nMOS switch will not be turned on, and VBUS is disconnected from VOUT.

The MOS VOUT enable switch is also turned off for power protection. When output overvoltage, undervoltage, overcurrent, overtemperature, or moisture detection occurs, the associated VOUT MOS switch is turned off to protect the host system from possible damage.

Power Protection

The AP33771C offers short-protection between CC1/CC2 pins to adjacent high-voltage pin up to 34V. In addition, the smart built-in firmware of the AP33771C offers comprehensive safety protection schemes, including OVP, UVP, OCP, and OTP. When the power protection occurs, the associated VOUT MOS switch is turned off to disconnect VBUS from VOUT.

The AP33771C triggers the OVP protection when VBUS voltage is higher than OVP threshold voltage. Table 4 below summarizes the correspondence between V_{REQ} and OVP threshold voltage, where V_{REQ} is the requested voltage after successful power negotiation with the PD source controller, and OVP threshold is set to be 2V above V_{REQ}. If VBUS voltage is higher than OVP threshold after the de-bounce time limit, the AP33771C will issue hard reset to the source adapter and enter the FAULT state by turning off nMOS switch to disconnect VBUS from VOUT. The AP33771C will auto restart after the OVP.

Index	1	2	3	4	5	6	7	8
V_{REQ}	5V	9V	12V	15V	20V	28V	Reserved	Reserved
OVP Threshold	7V	11V	14V	17V	22V	30V	—	—

Table 4. Correspondence Between V_{REQ} and OVP Threshold Voltage

The AP33771C also triggers the UVP protection when VBUS voltage is lower than UVP threshold voltage. The UVP threshold voltage is set at 80% of the requested voltage (V_{REQ}).

The AP33771C supports OCP to control the output load condition. When the OCP function is enabled, the AP33771C monitors the output current through detection of IR drop on the 5mΩ Rsense resistor. Once the TCD device draws more current than the OCP threshold level (110% of the requested current I_{REQ}, the requested current after successful negotiation with the source), the AP33771C enables OCP by turning off the nMOS switch to disconnect VBUS from VOUT.

The AP33771C supports the OTP by embedding an internal junction temperature detection. When the temperature goes beyond the internal OTP threshold (+130°C), the associated VOUT MOS switch is turned off to disconnect VBUS from VOUT.

Moisture Detection

The AP33771C supports the moisture detection of the connector. As soon as the Type-C connector is plugged in, the impedance between signal line and ground is evaluated by internal ADC digitization and firmware calculation. If the impedance level is below the pre-determined threshold, the VOUT MOS switch is turned off to disconnect VBUS from VOUT, and the LED is switched to 2-sec flicker mode accordingly.

LED Indication

The user is informed of the system status by the LED blinking patterns. Table 5 summarizes LED indication and VOUT status in each state.

State	LED Indication	VOUT	Comments
INIT	NA	OFF	During VBUS/Rd attachment and AP33771C initialization
CHARGING	4-sec Cycle Breathing (Brightness gradually changes)	ON	Successful negotiation or enter Non-PD Mode and start charging
MISMATCH	Full Light	OFF	Voltage or Current mismatch
MOISTURE	2-sec Cycle Flicker	OFF	Abnormal impedance in connector is detected
FAULT	0.6-sec Cycle Flicker	OFF	OVP, OCP, UVP or OTP occurs.

Table 5. Flash LED Indication for Different Negotiation Results

Functional Description (continued)

Cable Voltage Drop Compensation for PD Mode

After the AP33771C completes the RDO negotiation based on VSEL and ISEL and enables the VOUT MOS switch, the AP33771C monitors the VOUT voltage level. If the VOUT voltage (V_{VOUT}) fails to reach more than 6% below the selected voltage (V_{VSEL}), the AP33771C activates automatic Type-C cable voltage drop compensation scheme, shown as Table 6.

Source PDO	Compensation Criteria	Compensation Manner	Voltage Compensation Upper Limit
Fixed PDO	V_{VOUT} < V_{VSEL} x 0.94 (Note 11)	PDO Position + 1 (Next Higher Voltage PDO)	4.0V (Note 12)
PPS APDO	V_{VOUT} < V_{VSEL} x 0.94 (Note 11)	Voltage + 0.1V Each Voltage Drop Compensation Iteration	1.3V (Note 13)

Notes: 11. Enables voltage drop compensation when V_{VOUT} < V_{VSEL} x (1 - 6%).
12. Upper limit of voltage compensation is set at 4.0V to prevent subsequent circuit from potential damage. For example, PDO 5V can only be raised to next PDO 9V.
13. The Type-C to Type-C compliance cables have typically end-to-end resistance of 250mΩ of any length. The maximum voltage drop compensation allowed is 1.3V - from source-end to sink-end of a Type-C to Type-C cable should be within 1.25V for maximum current of 5A.

Table 6. Cable Voltage Drop Compensation Criteria for PD Mode

The VOUT voltage behavior comparison between Cable drop compensation and non-compensation is shown in Table 7 below. If the voltage drop compensation fails, it means that no suitable PDO is found or voltage compensation exceeds the upper limit.

Source PDO	V_{VSEL}	Before Compensation		After Compensation	
		Original Request Voltage	V_{VOUT}	Adjusted Request Voltage (V_{AREQ})	V_{VOUT}
Fixed_5V	5V	Fixed_5V	< 4.7V	Fixed_5V	< 4.7V
Fixed_5V / Fixed_9V	5V	Fixed_5V	< 4.7V	Fixed_9V	9V-Cable Voltage Drop (1.3V max) (Note 15)
Fixed_5V / Fixed_9V / PPS_3.3 to 11V	5V	PPS_5V	< 4.7V	PPS_5V+Voltage Drop (1.3V max) (Note 14)	≥ 4.7V
Fixed_5V / Fixed_9V / PPS_3.3 to 11V	5V	PPS_5V	< 4.7V	PPS_5V+1.3V	< 4.7V

Notes: 14. If the cable voltage drop from the source-end to the sink-end is 1.0V, adjusted V_{AREQ} would be 5.7V for V_{VOUT} to reach 4.7V
15. If the cable voltage drop from the source-end to the sink-end is 1.0V, adjusted V_{AREQ} would be 9V and V_{VOUT} would be 8V

Table 7. VOUT Voltage Behavior Under PD Mode with Cable Drop Compensation

Legacy Type-A Charger with Type-A to Type-C Cable

When the energy source is from a legacy Type-A charger with Type-A to Type-C cable connection to the TCD, the AP33771C enters the Non-PD mode after PD negotiation fails. Table 8 below shows the Non-PD mode state of AP33771C.

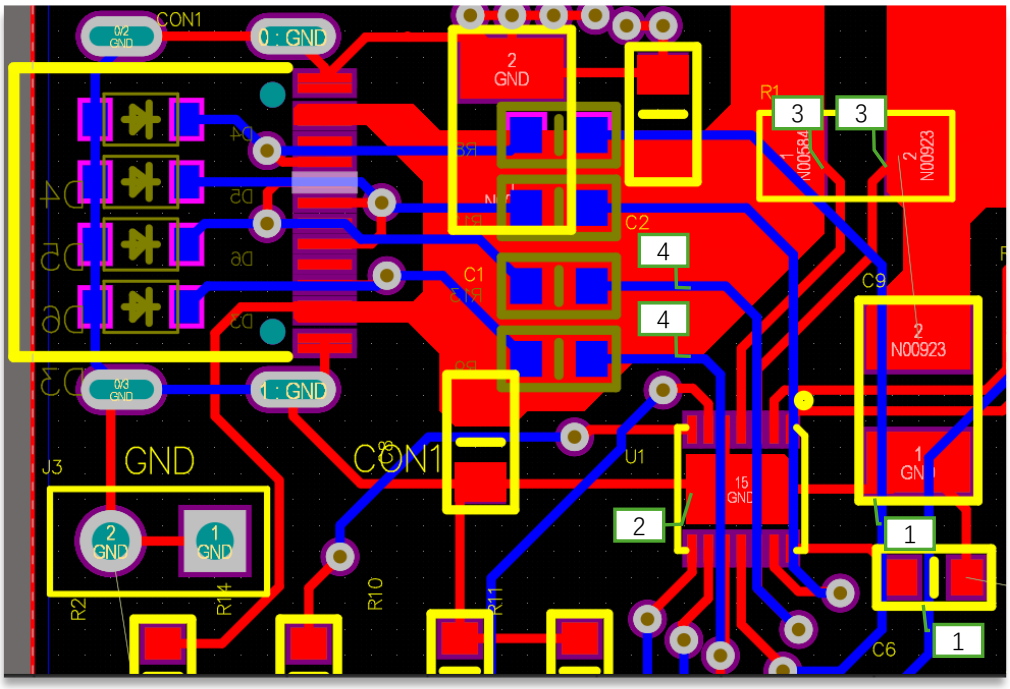
Non-PD Mode State			
V_{VSEL}	$V_{VSELMIN}$	V_{VOUT}	State
V_{VSEL} = 5V	5V	ON	CHARGING
V_{VSEL} ≥ 9V	5V	ON	CHARGING

Table 8. VOUT Voltage Status Under Non-PD Mode

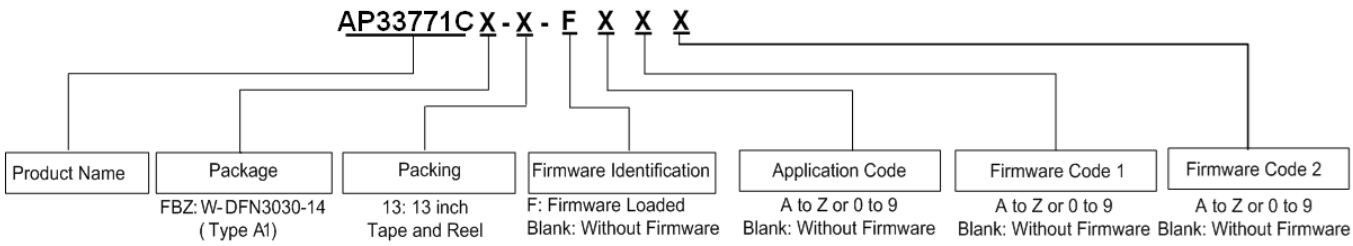
PCB Layout Guideline

Suitable PCB layout is critical for stable operation and better ESD performance. Follow some guidelines as below:

1. Place the VCC/V5V decoupling capacitor as close to the pins as possible.
2. The exposed pad of the IC must be connected to GND. It is better for noise immunity.
3. Current sensing traces must start directly from the footprint pads of current sensing resistor.
4. Use traces to connect CC1/CC2 pins to the USB Type-C receptacle as short as possible.



Ordering Information (Note 16)



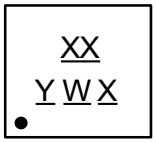
Orderable Part Number (Note 17)	Package	Identification Code	Firmware Inside	Packing	
				Qty.	Carrier
AP33771CFBZ-13-FA01	W-DFN3030-14 (Type A1)	6X	Standard Firmware (Function as Described in Datasheet)	3000	13” Tape & Reel
AP33771CFBZ-13-FA02					
AP33771CFBZ-13-FXXX			Customized Firmware		

Note: 16. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.
17. It is recommended to order Standard Firmware device based on functions described in datasheet. For without firmware and customized options, please contact us or your local Diodes representative.

Marking Information

W-DFN3030-14 (Type A1)

(Top View)

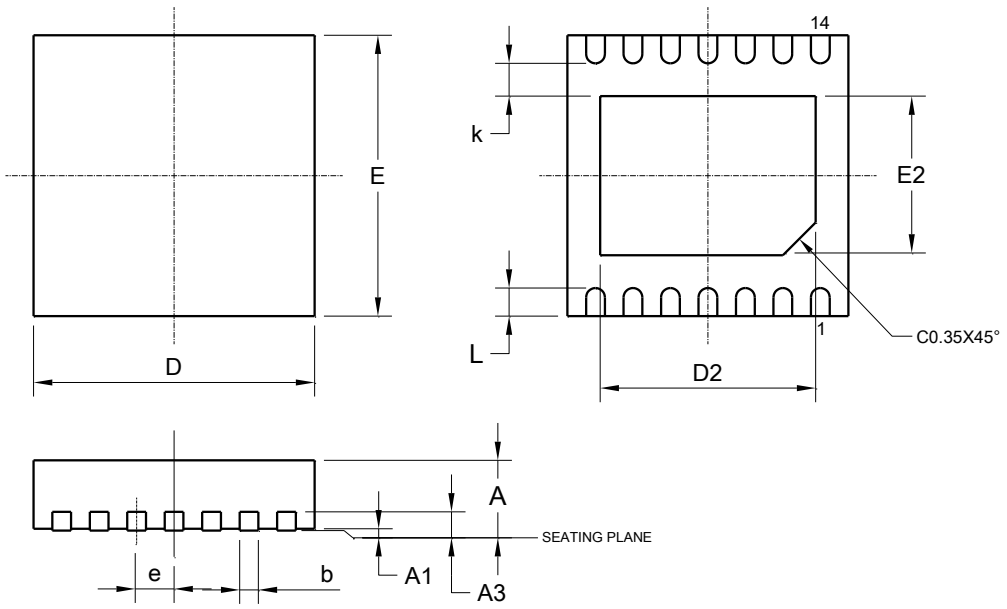


XX : Identification Code
Y : Year : 0 to 9 (ex: 5 = 2025)
W : Week : A to Z : week 1 to 26;
a to z : week 27 to 52; z represents week 52 and 53
X : Internal Code

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-DFN3030-14 (Type A1)

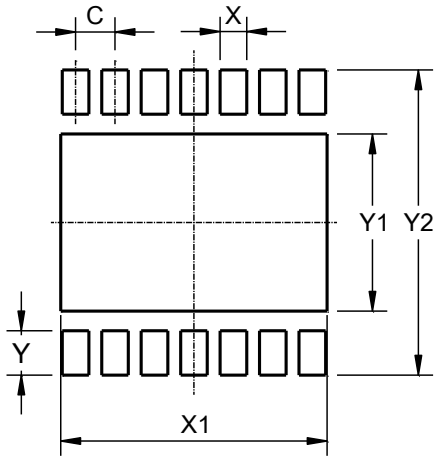


W-DFN3030-14 (Type A1)			
Dim	**Min**	**Max**	**Typ**
A	0.70	0.80	0.75
A1	0.00	0.05	0.02
A3	0.203REF		
b	0.15	0.25	0.20
D	3.00BSC		
D2	2.55	2.65	2.60
e	0.40BSC		
E	3.00BSC		
E2	1.65	1.75	1.70
k	0.20	--	--
L	0.35	0.45	0.40
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-DFN3030-14 (Type A1)



Dimensions	Value (in mm)
C	0.40
X	0.27
X1	2.70
Y	0.45
Y1	1.80
Y2	3.10

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per J-STD-202 e3
- Weight: 0.017 grams (Approximate)

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