



TuffDrive® S51 Series – SD Memory Card

Industrial SD 3.0, SLC

VTDS51PI xxxG- V11

Datasheet - Rev. 1.2



1. Description

Virtium TuffDrive® S51 SD card provide highly reliable storage media in a very small space. The simplicity of the SD and SPI protocols allows easy host design and integration. The TuffDrive S51 SD card support a high security level of copyright protection and an easy to implement interface.

Features

Capacity

- 2GB, 4GB, 8GB, 16GB, 32GB

SLC NAND

Class: Class 10, UHS-I

Sequential Performance⁽¹⁾

- 128kB Sequential Read: 72 MB/s (QD: 32)
- 128kB Sequential Write: 50 MB/s (QD:32)

Voltage Supply: 2.7V – 3.6V

Power Consumption⁽¹⁾

- Sequential Read: 0.25 W
- Sequential Write: 0.30 W
- Idle: 0.15 W

Temperature Ranges

- Industrial: -40°C to 85°C
- Non-Operating: -40°C to 85°C

Reliability

- 40-Bit/1K Hardware BCH ECC
- Number of card insertions/removals up to 10,000
- MTBF: >5M hours

Advanced Flash Management

- ECC Correction
- Static and Dynamic Wear Leveling
- Bad Block Management

Write Protect with mechanical switch

Mechanical Dimensions

- 9-Pin SD Standard
- Length x Width x Height mm (inches)
32.00 (1.259) x 24.00 (0.945) x 2.1 (0.083)
- Weight: 2g ± 0.1g

Compliance

- SD Memory Card Specifications
 - Physical Layer Specification Ver. 3.1 (Part 1)
 - File System Specification Ver. 3.0 (Part 2)
 - Security Specification Ver. 3.0 (Part 3)
- FCC, CE, UL, RoHS, WEEE

Environmental (Non-operating)

- Humidity (non-condensing): 5% to 95%
- Shock: 1500G, half-sine wave, 0.5ms duration
- Vibration: 20G, 20 Hz to 2000 Hz

(1) Based on the 32GB device



Electrostatic Discharge (ESD) can damage this device. When handling the device, always wear a grounded wrist strap and use a static dissipative surface.



Any damage to the unit that occurs after its removal from the shipping package and ESD protective bag is the responsibility of the user.

Part Numbering System

V TD S51 P I XXXG - V11

Where:	
V	= Virtium
TD	= TuffDrive
S51	= Form Factor / Interface: S51 = 9-Pin SD card / SD 3.1 Specification
P	= Product Class: P = PE
I	= Operating Temperature: I = Industrial (-40°C to 85°C)
XXXG	= Capacity (1GB = 1,000,000,000 bytes) 002G = 2 GB 004G = 4 GB 008G = 8 GB 016G = 16 GB 032G = 32 GB
V11	= Virtium Proprietary

Order Information

Capacity (GB)	Part Number
2	VTDS51PI002G-V11
4	VTDS51PI004G-V11
8	VTDS51PI008G-V11
16	VTDS51PI016G-V11
32	VTDS51PI032G-V11

2. Revision History

Date	Revision	Page(s)	Description
08/05/2022	1.0	All	First Release
10/05/2022	1.1	All	Remove SMART section and updated datasheet's format
11/02/2022	1.2	All	Updated the performance, power, and endurance numbers based on final validation testing.

3. Specifications

Capacity

Unformatted Capacity (GB) ⁽¹⁾	User-Addressable LBA ⁽²⁾	User-Addressable Capacity Bytes
2	3,907,672	2,000,728,064
4	7,774,208	3,980,394,496
8	15,542,272	7,957,643,264
16	31,834,112	16,299,065,344
32	62,531,584	32,016,171,008

(1) 1GB = 1,000,000,000 bytes. LBA: Logical Block Address; Logical Block Size = 512 Bytes/1 Sector.
 (2) LBA: Logical Block Address; Logical Block Size = 512 Bytes/1 Sector.

Performance

Capacity (GB)	Sequential Read ⁽¹⁾ MB/s	Sequential Write ⁽¹⁾ MB/s
2	34	26
4	34	26
8	72	50
16	72	50
32	72	50

(1) Product Performance is based on running CrystalDiskMark 8.00

Power Requirements

Parameter	Min	Typ	Max
Voltage supply (3.3V)	2.7V	3.3V	3.6V

Parameter	Sequential Read	Sequential Write	Idle
Power Consumption ⁽¹⁾	0.25 W	0.30 W	0.15 W

(1) Based on the 32GB device. Measured at 3.3V

Temperature and Humidity

Part Number	Operating Temperature	Non-Operating ⁽¹⁾ Temperature	Moisture Sensitivity (Non-Condensing)
VTDS51PI002G-V11			
VTDS51PI004G-V11			
VTDS51PI008G-V11			
VTDS51PI016G-V11			
VTDS51PI032G-V11			

(1) Maximum non-operating temperature assumes data is stored on the SSD. Temperatures above 85°C are beyond NAND specification for data retention. Please see *Temperature Considerations for Industrial Embedded SSDs* whitepaper under the industrial SSD section of Virtium website (Virtium.com)

Shock and Vibration

Reliability	Test Conditions	Reference Standards
Shock	1500G, half-sine wave, 0.5ms duration	JESD22-B110B.01
Vibration	20G, 20 Hz to 2000 Hz	JESD22-B103B.01

Electrostatic Discharge (ESD)

	Test Conditions
Non-operating	Contact discharge: $\pm 4\text{KV}$; 5 times/Pin Air discharge: $\pm 15\text{KV}$; 5 times/Position
Operating	Air discharge: $\pm 8\text{KV}$; 10 times/Position (EN55024-61000-4-2)

4. Reliability

Endurance

Capacity (GB)	JESD218A ⁽¹⁾ & JESD219 Enterprise Workloads		100% Sequential Workloads	
	Total Bytes Written TBW (TB)	Drive Writes per day (5 years)	Total Bytes Written TBW (TB)	Drive Writes per day (5 years)
2	17	4.6	195	53.0
4	38	5.2	387	53.0
8	75	5.2	774	53.0
16	187	6.4	1548	53.0
32	498	8.5	3097	53.0

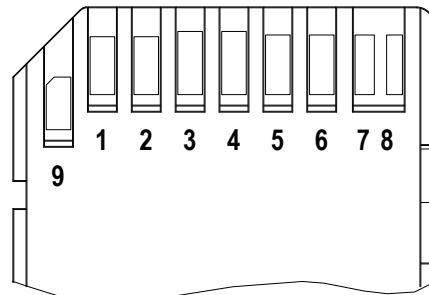
(1) JESD218A assumes an active temperature at 55°C and a retention temperature at 40°C

Mean Time Between Failures (MTBF)

The SSD achieves a MTBF of greater than 5,000,000 hours predicted and is derived from the component reliability data using Telcordia SR-332 methods at 40°C and tested under standard environmental operating conditions.

5. Physical Specifications

Pin Layout / Assignments



SD Memory Card Pin assignment (Back View of the card)

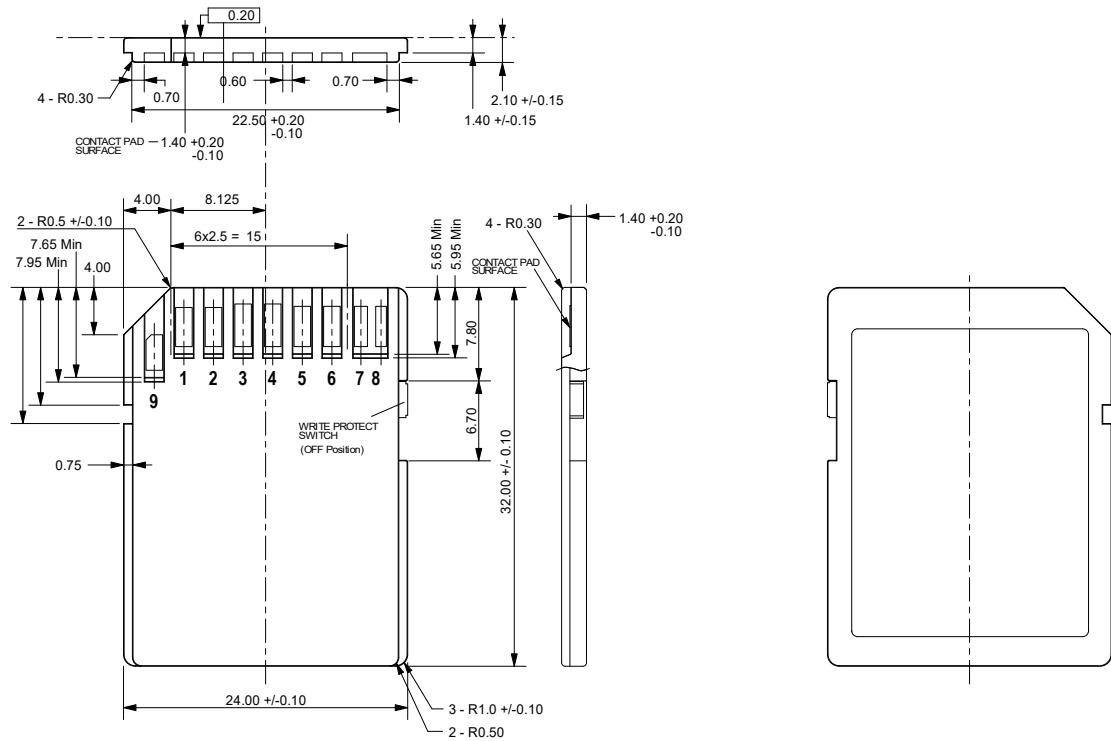
Pin	SD Mode			SPI Mode		
	Name	Type ⁽¹⁾	Description	Name	Type	Description
1	CD/DAT3 ⁽²⁾	I/O/PP ⁽³⁾	Card Detect/ Data Line [bit3]	CS	I ⁽³⁾	Chip Select (neg. true)
2	CMD	PP	Command/Response	DI	I	Data In
3	VSS	S	Supply voltage ground	VSS	S	Supply voltage ground
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	VSS	S	Supply voltage ground	VSS	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line [bit1]	RSV		
9	DAT2	I/O/PP	Data Line [bit2]	RSV		

(1) S: power supply, I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers.

(2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode as well while they are not used. It is defined so in order to keep compatibility to MultiMedia Cards.

(3) At power up, this line has a 50KOhm pull up enabled in the card. This resistor serves two functions: Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode, it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer with SET_CLR_CARD_DETECT (ACMD42) command.

Mechanical Dimensions



Note: 1. All dimensions are in millimeters
2. The dimensional diagram is for reference only

6. Electrical Specifications

DC Characteristic

Bus Operation Conditions for 3.3V Signaling

Parameter	Symbol	Min	Max	Unit	Condition
Supply Voltage	VDD	2.7	3.6	V	
Output High Voltage	VOH	0.75*VDD		V	IOH=-2mA VDD Min
Output Low Voltage	VOL		0.125*VDD	V	IOL=2mA VDD Min
Input High Voltage	VIH	0.625*VDD	VDD+0.3	V	
Input Low Voltage	VIL	VSS-0.3	0.25*VDD	V	
Power Up Time			250	ms	From 0V to VDD min
Peak voltage on all lines		-0.3	VDD+0.3	V	
Input Leakage Current – All Input		-10	10	uA	
Output Leakage Current – All Input		-10	10	uA	

Bus Operation Conditions for 1.8V Signaling

Parameter	Symbol	Min	Max	Unit	Condition
Supply Voltage	VDD	2.7	3.6	V	
Regulator Voltage	VDDIO	1.7	1.95	V	Generated by VDD
Output High Voltage	VOH	1.4	-	V	IOH=-2mA
Output Low Voltage	VOL	-	0.45	V	IOL=2mA
Input High Voltage	VIH	1.27	2.00	V	
Input Low Voltage	VIL	Vss-0.3	0.58	V	
Input Leakage Current – All Input		-2	2	uA	

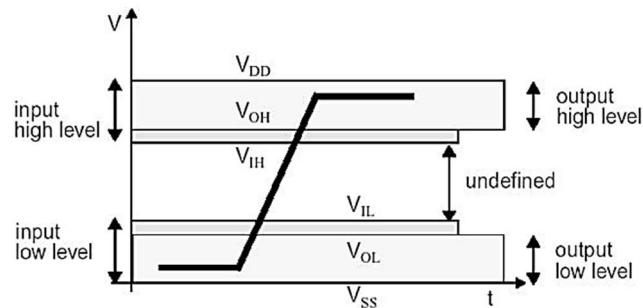
Bus Operation Conditions – Signal Line's Load

Total Bus Capacitance = CHOST + CBUS + N CCARD

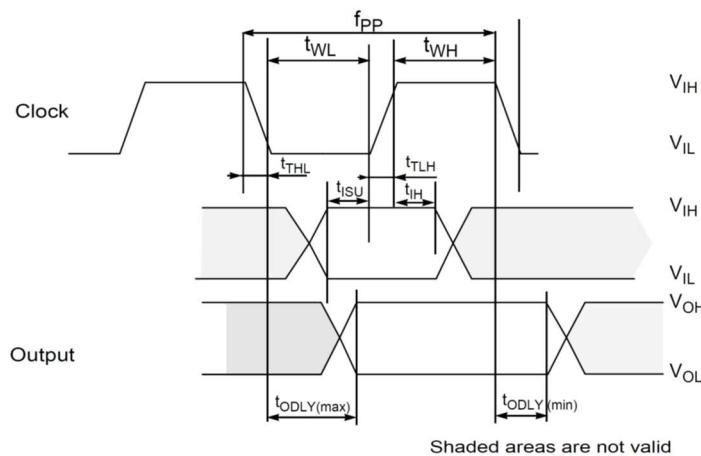
Parameter	Symbol	Min	Max	Unit	Condition
Pull-up resistance	RCMD	10	100	kΩ	to prevent bus floating
Total bus capacitance for each signal line	RDAT		40	pF	1 card CHOST+CBUS shall not exceed 30 pF
Card Capacitance for each signal pin	CL		10	pF	
Maximum signal line inductance	CCARD		16	nH	
Pull-up resistance inside card (pin1)	RDAT3	10	90	kΩ	May be used for card detection
Capacity Connected to Power Line	CC		5	uF	

AC Characteristic

Bus Signal Levels



Bus Timing (Default Mode)

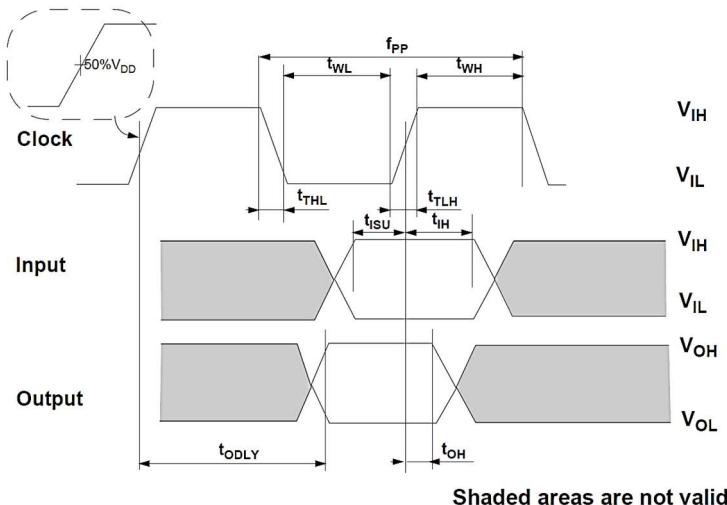


Timing diagram data input/output referenced to clock (Default)

Parameter	Symbol	Min	Max	Unit	Condition
Clock CLK (All values are referred to min. (V_{IH}) and max. (V_{IL}))					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	CCARD ≤ 10 pF (1 card)
Clock frequency Identification Mode	f_{OD}	$0^{(1)}/10$	400	kHz	CCARD ≤ 10 pF (1 card)
Clock low time	t_{WL}	10		ns	CCARD ≤ 10 pF (1 card's)
Clock high time	t_{WH}	10		ns	CCARD ≤ 10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	CCARD ≤ 10 pF (1 card)
Clock fall time	t_{THL}		10	ns	CCARD ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	CCARD ≤ 10 pF (1 card)
Input hold time	t_{IH}	5		ns	CCARD ≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	$CL \leq 40$ pF (1 card)
Output delay time during Identification Mode	t_{ODLY}	0	50	ns	$CL \leq 40$ pF (1 card)

1) 0Hz means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required

Bus Timing (High-speed Mode)



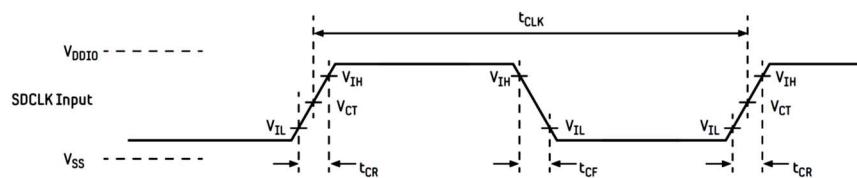
Timing diagram data input/output referenced to clock (High-speed)

Parameter	Symbol	Min	Max	Unit	Condition
Clock CLK (All values are referred to min. (VIH) and max. (VIL))					
Clock frequency Data Transfer Mode	fPP	0	50	MHz	CCARD <= 10 pF (1 card)
Clock low time	tWL	7		ns	CCARD <= 10 pF (1 card)
Clock high time	tWH	7		ns	CCARD <= 10 pF (1 card)
Clock rise time	tTLH		3	ns	CCARD <= 10 pF (1 card)
Clock fall time	tTHL		3	ns	CCARD <= 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	6		ns	CCARD <= 10 pF (1 card)
Input hold time	tIH	2		ns	CCARD <= 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output delay time during Data Transfer Mode	tODLY		14	ns	CL <= 40 pF (1 card)
Output Hold time	tOH	2.5		ns	CL <= 15 pF (1 card)
Total System capacitance for each line ⁽¹⁾	CL		40	pF	CL <= 15 pF (1 card)

1) In order to satisfy severe timing, host shall drive only one card.

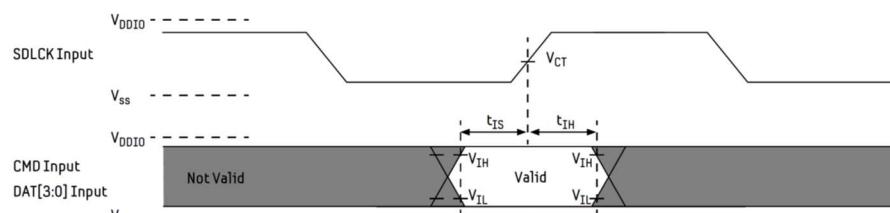
Bus Timing Specification in SDR12, SDR25, SDR50 and SDR104 Modes

Clock Signal Timing				
Symbol	Min	Max	Unit	Remark
tCLK	4.80	-	ns	208MHz (Max.), Between rising edge, VCT= 0.975V
tCR, tCF	-	0.2* tCLK	ns	tCR, tCF < 0.96ns (max.) at 208MHz, CCARD=10pF tCR, tCF < 2.00ns (max.) at 100MHz, CCARD=10pF The maximum value of tCR, tCF is 10ns regardless of clock frequency
Clock Duty	30	70	%	



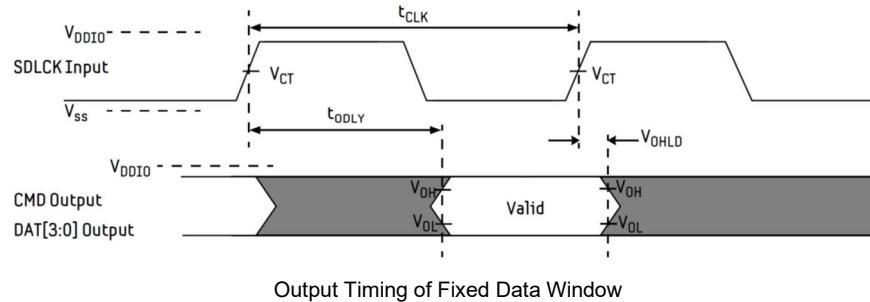
Clock Signal Timing

SDR50 and SDR104 Input Timing				
Symbol	Min	Max	Unit	SDR104 Mode
tIS	1.40	-	ns	CCARD=10pF, VCT= 0.975V
tIH	0.80	-	ns	CCARD=5pF, VCT= 0.975V
Symbol	Min	Max	Unit	SDR50 Mode
tIS	3.00	-	ns	CCARD=10pF, VCT= 0.975V
tIH	0.80	-	ns	CCARD=5pF, VCT= 0.975V



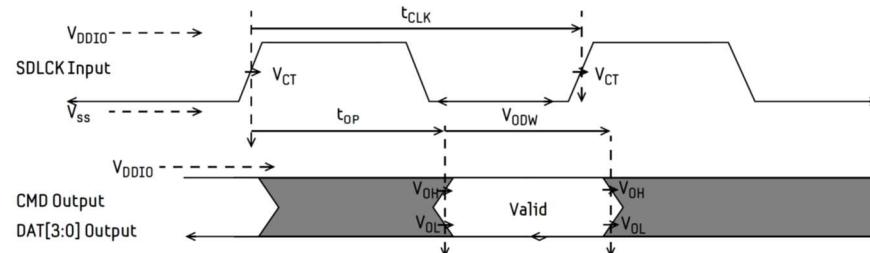
Card Input Timing

Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50)				
Symbol	Min	Max	Unit	Remark
tODLY	-	7.5	ns	tCLK >= 10.0ns, CL = 30pF, using driver Type B. for SDR50
tODLY	-	14	ns	tCLK >= 20.0ns, CL = 40pF, using driver Type B. for SDR25 and SDR12
tOH	1.5	-	ns	Hold time at the tODLY (min.), CL = 15pF



Output Timing of Fixed Data Window

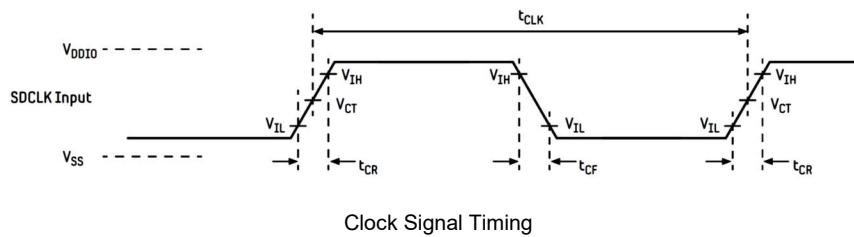
Output Timing of Variable Window (SDR104)				
Symbol	Min	Max	Unit	Remark
tOP	0	2	UI	Card Output Phase
ΔtOP	-350	+1550	ps	Delay variation due to temperature change after tuning
tODW	0.60	-	UI	$tODW = 2.88\text{ns}$ at 208MHz



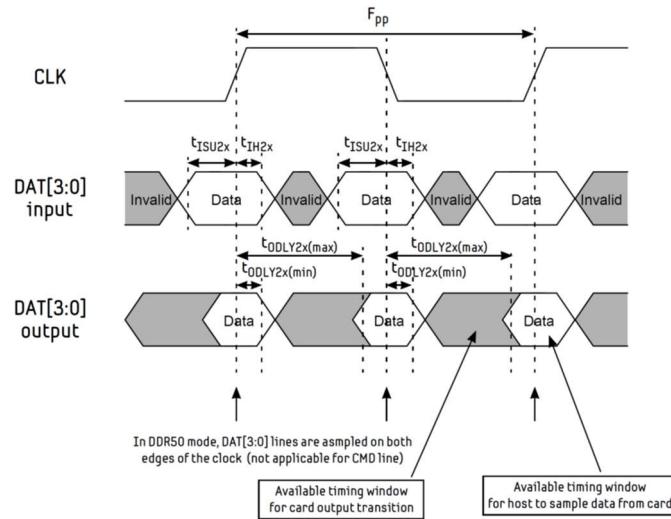
Output Timing of Variable Data Window

Bus Timing Specification in SDR50 Modes

Clock Signal Timing				
Symbol	Min	Max	Unit	Remark
tCLK	20	-	ns	50MHz (Max.), Between rising edge
tCR, tCF	-	0.2* tCLK	ns	tCR, tCF <4.00ns (max.) at 50MHz, CCARD=10pF
Clock Duty	45	70	%	



Bus Timings - Parameters Values (DDR50 mode)					
Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t _{ISU}	6	-	ns	CCARD ≤10pF (1 card)
Input hold time	t _{IH}	0.8	-	ns	CCARD ≤10pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t _{ODLY}	-	13.7	ns	CCARD ≤30pF (1 card)
Output hold time	t _{OH}	1.5	-	ns	CCARD ≤15pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t _{ISU2X}	3	-	ns	CCARD ≤10pF (1 card)
Input hold time	t _{IH2X}	0.8	-	ns	CCARD ≤10pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t _{ODLY2X}	-	7.0	ns	CCARD ≤25pF (1 card)
Output hold time	t _{ODLY2X}	1.5	-	ns	CCARD ≤15pF (1 card)



Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

7. Card Registers

SD Card Registers

Name	Width	Description
CID	128bit	Card Identification information
RCA ⁽¹⁾	16bit	Relative card address
DSR	16bit	Driver Stage Register
CSD	128bit	Card Specific Data
SCR	64bit	SD Configuration Register
OCR	32bit	Operation conditions register
SSR	512bit	SD Status
OCR	32bit	Operation Condition Register

(1) RCA register is not used (or available) in SPI mode.

8. SD Card Bus Topology

The SD Memory Card supports two alternative communication protocols: SD and SPI Bus mode. The host system can choose either one of the modes. The same data on the SD Card can be read and written by both modes.

SD mode allows 4-bit high-performance data transfer. SPI mode supports the easy and common interface for SPI channel. The disadvantage of this mode is the loss of performance relative to the SD mode.

Please see the SD Memory Card Specifications Part 1 - Physical Layer Specification, Version 6.10 for details.

9. Certifications and Compliance

Compliance / Certification	Description
CE and FCC Compliant	Class: FCC Part 15 Subpart B Class B:2011 Declaration of Conformity registration No. STE120607699
RoHS Compliant	Restriction of Hazardous Substance Directive
UL Certified	Underwriters Laboratories, Inc. 94V-0
WEEE Certified	Waste, Electrical and Electronic Equipment Directive

10. Contact Information

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