Product Specifications		
PART NO.:	VL51A1H63F-N7SC	REV: 1.1

General Information

8GB 1Gx72 DDR4 SDRAM ULP ECC UNBUFFERED Mini-UDIMM 288-PIN

Description

The VL51A1H63F is a 1Gx72 DDR4 SDRAM high density Mini-UDIMM. This single rank memory module consists of nine CMOS 1Gx8 bits with 16 internal banks DDR4 Synchronous DRAMs in BGA packages, and a 4K EEPROM with thermal sensor in an 8-pin MLF package. This module is a 288-pin mini dual in-line memory module and is intended for mounting into an edge connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR4 SDRAM.

Features

- 288-pin, unbuffered mini dual in-line memory module (Mini-UDIMM)
- Supports ECC error detection and correction
- Fast data transfer rate: 2400MT/s
- VDD = VDDQ = 1.2V +/-0.060V
- VPP = 2.5V (2.375 min, 2.75 max)
- VDDSPD = 2.5V or 3.3V +/-10%
- 16 internal banks; 4 groups of 4 banks each
- Nominal and dynamic on-die termination (ODT)
- Low-power auto self refresh
- Programmable CAS# latency: 17 (DDR4-2400)
- Programmable burst length (8)
- Asynchronous reset
- On-die VREFDQ generation and calibration
- Fly-by topology
- On board terminated command, address, and control bus
- Serial presence detect (SPD) EEPROM with thermal sensor
- Thermal sensor range: -40ºC to +125ºC (Max +/-3% accuracy)
- Lead-free, RoHS compliant
- JEDEC pinout
- Gold edge contacts
- PCB: Height 17.78mm (0.700”), double sided component
- Operating temperature (TOPER)[1]: - Commercial (0ºC to +95ºC)
  - Industrial (-40ºC to +95ºC)

Notes: (1) Double refresh rate is required when 85ºC < TOPER <= 95ºC.
TOPER is DRAM case temperature.

Order Information:

VL51A1H63F - N7 S C - X

- X: OPERATING TEMPERATURE
  None: Commercial
  S1: Industrial screening
- C: DRAM DIE: C
- S: DRAM MANUFACTURER
  S - SAMSUNG
- N7: MODULE SPEED
  N7: DDR4-2400 @ CL17
- VL: Lead-free/RoHS

DRAM component: K4A8G085WC-BCTD

Pin Description

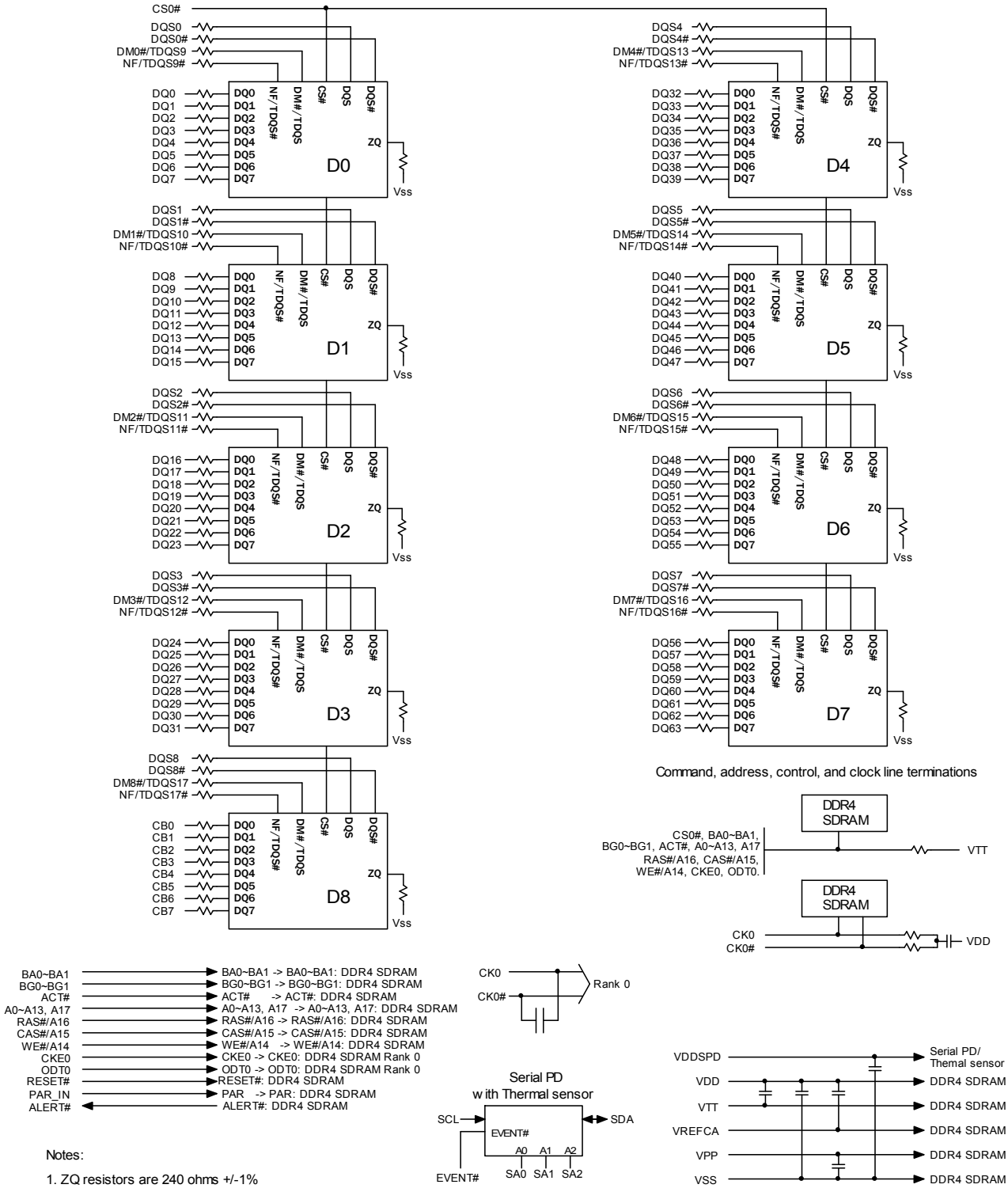
Pin Name	Function
A0~A15	Row Address Inputs
A0~A9	Column Address Inputs
A10/AP	Address Input/ Autoprecharge
A12/BC#	Address Input/ Burst Chop
ACT#	Activate input
RAS#/A16	Row Address Strobes/ Address Input
CAS#/A15	Column Address Strobes/ Address Input
WE#/A14	Write Enable/Address Input
BA0~BA1	Bank Address Inputs
BG0~BG1	Bank group address inputs
DQ0~DQ63	Data Input/Output
DQS0~DQS8	Data Strobes
DQS0#~DQS8#	Data Strobes Complement
DM0#~DM8#	Data Mask Input
TDQS9~TDQS17 TDQS9#~TDQS17#	Termination data strobe
CB0~CB7	Data Check Bits I/O
PAR_IN	Parity Input
ALERT#	Alert output
CK0, CK0#	Clock Inputs
ODT0	On-die Termination Controls
CKE0	Clock Enables
CS0#	Chip Selects
RESET#	Register and SDRAM Control
VDD	Voltage Supply
VPP	DRAM Activating Voltage Supply
VSS	Ground
SA0~SA2	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
EVENT#	Temperature Event Output
VREFCA	Reference Voltage for CA
VDDSPD	SPD Voltage Supply
VTT	Termination Voltage
NC	No Connect

Pin Configuration

288-PIN DDR4 Mini-UDIMM FRONT SIDE								288-PIN DDR4 Mini-UDIMM BACK SIDE							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	12V, NC	37	VSS	73	A1	109	DQ41	145	VREFCA	181	VSS	217	RFU	253	DQ45
2	12V,NC	38	DQ24	74	VDD	110	VSS	146	SAVE#,NC	182	DQ28	218	VDD	254	VSS
3	RFU	39	VSS	75	CK0	111	DQS5#	147	RFU	183	VSS	219	CK1*	255	DM5#/ TDQS14
4	VSS	40	DQ25	76	CK0#	112	DQS5	148	VSS	184	DQ29	220	CK1#*	256	NF/TDQS14#
5	DQ0	41	VSS	77	VDD	113	VSS	149	DQ4	185	VSS	221	VDD	257	VSS
6	VSS	42	DQS3#	78	RFU	114	DQ42	150	VSS	186	DM3#/ TDQS12	222	RFU	258	DQ46
7	DQ1	43	DQS3	79	VTT	115	VSS	151	DQ5	187	NF/TDQS12#	223	VTT	259	VSS
8	VSS	44	VSS	80	EVENT#	116	DQ43	152	VSS	188	VSS	224	PAR_IN	260	DQ47
9	DQS0#	45	DQ26	81	VDD	117	VSS	153	DM0#/ TDQS9	189	DQ30	225	VDD	261	VSS
10	DQS0	46	VSS	82	A0	118	DQ48	154	NF/TDQS9#	190	VSS	226	BA1	262	DQ52
11	VSS	47	DQ27	83	BA0	119	VSS	155	VSS	191	DQ31	227	A10/AP	263	VSS
12	DQ2	48	VSS	84	VDD	120	DQ49	156	DQ6	192	VSS	228	VDD	264	DQ53
13	VSS	49	CB0	85	RAS#/A16	121	VSS	157	VSS	193	CB4	229	WE#/ A14	265	VSS
14	DQ3	50	VSS	86	CS0#	122	DQS6#	158	DQ7	194	VSS	230	CAS#/ A15	266	DM6#/ TDQS15
15	VSS	51	CB1	87	VDD	123	DQS6	159	VSS	195	CB5	231	VDD	267	NF/TDQS15#
16	DQ8	52	VSS	88	ODT0	124	VSS	160	DQ12	196	VSS	232	A13	268	VSS
17	VSS	53	DQS8#	89	CS1#*	125	DQ50	161	VSS	197	DM8#/ TDQS17	233	A17*	269	DQ54
18	DQ9	54	DQS8	90	VDD	126	VSS	162	DQ13	198	NF/TDQS17#	234	VDD	270	VSS
19	VSS	55	VSS	91	ODT1*	127	DQ51	163	VSS	199	VSS	235	C1*	271	DQ55
20	DQS1#	56	CB2	92	C0*	128	VSS	164	DM1#/ TDQS10	200	CB6	236	C2*	272	VSS
21	DQS1	57	VSS	93	VDD	129	DQ56	165	NF/TDQS10#	201	VSS	237	VDD	273	DQ60
22	VSS	58	CB3	94	RFU	130	VSS	166	VSS	202	CB7	238	RFU	274	VSS
23	DQ10	59	VSS	95	VSS	131	DQ57	167	DQ14	203	VSS	239	VSS	275	DQ61
24	VSS	60	ALERT#	96	DQ32	132	VSS	168	VSS	204	RESET#	240	DQ36	276	VSS
25	DQ11	61	CKE0	97	VSS	133	DQS7#	169	DQ15	205	RFU	241	VSS	277	DM7#/ TDQS16
26	VSS	62	VDD	98	DQ33	134	DQS7	170	VSS	206	VDD	242	DQ37	278	NF/TDQS16#
27	DQ16	63	ACT#	99	VSS	135	VSS	171	DQ20	207	CKE1*	243	VSS	279	VSS
28	VSS	64	BG0	100	DQS4#	136	DQ58	172	VSS	208	BG1	244	DM4#/ TDQS13	280	DQ62
29	DQ17	65	VDD	101	DQS4	137	VSS	173	DQ21	209	VDD	245	NF/TDQS13#	281	VSS
30	VSS	66	A12/BC#	102	VSS	138	DQ59	174	VSS	210	A11	246	VSS	282	DQ63
31	DQS2#	67	A9	103	DQ34	139	VSS	175	DM2#/ TDQS11	211	A7	247	DQ38	283	VSS
32	DQS2	68	VDD	104	VSS	140	SA0	176	NF/TDQS11#	212	VDD	248	VSS	284	SA1
33	VSS	69	A8	105	DQ35	141	VDDSPD	177	VSS	213	A5	249	DQ39	285	SA2
34	DQ18	70	A6	106	VSS	142	SDA	178	DQ22	214	A4	250	VSS	286	SCL
35	VSS	71	VDD	107	DQ40	143	VPP	179	VSS	215	VDD	251	DQ44	287	VPP
36	DQ19	72	A3	108	VSS	144	VPP	180	DQ23	216	A2	252	VSS	288	VPP

*: These pins are not used in this module.

Function Block Diagram



Notes:

1. ZQ resistors are 240 ohms +/-1%

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
VDD	Voltage on VDD pin relative to VSS	-0.4	1.5	V	1
VDDQ	Voltage on VDDQ pin relative to VSS	-0.4	1.5	V	1
VPP	Voltage on VPP pin relative to VSS	-0.4	3.0	V	2
VIN, VOUT	Voltage on any pin relative to VSS	-0.4	1.5	V	
TSTG	Storage temperature	-55	100	^{0}C	

Notes:
1. VDDQ balls on DRAM are tied to VDD.
2. VPP must be greater than or equal to VDD at all times.

DC Operating Conditions

Symbol	Parameter		Min	Typical	Max	Unit	Notes
VDD	VDD Supply Voltage		1.14	1.2	1.26	V	1
VDDQ	VDDQ Supply Voltage for Input/Output		1.14	1.2	1.26	V	1
VPP	DRAM Activating Power Supply		2.375	2.5	2.750	V	2
VREFCA (DC)	Input reference voltage CMD/ADD bus		0.49 x VDD	0.5 x VDD	0.51 x VDD	V	3
VTT	Termination Reference Voltage (DC) - command/address bus		0.49 × VDD - 20mV	0.5 x VDDQ	0.51 × VDD + 20mV	V	4
I_{VTT}	Termination reference current from VTT		-750	-	750	mA	
I_I	Input leakage current; any input excluding ZQ; 0V < VIN < 1.1V	Address inputs, RAS#, CAS#, WE#, CS#, CKE, ODT, BA, BG, PAR_IN	-18	-	18	uA	
		CK, CK#	-18	-	18	uA	
		DM#	-2	-	2	uA	
I_I	Input leakage current; ZQ		-27	-	27	uA	5
$I_{I/O}$	DQ leakage; 0V < Vin < VDD		-36	-	36	uA	
IOZpd	Output leakage current; VOUT=VDD; DQ is disabled		-	-	5	uA	
IOZpu	Output leakage current; VOUT = VSS; DQ and ODT are disabled; ODT is disabled with ODT input HIGH		-	-	50	uA	
IVREFCA	VREFCA leakage; VREFCA = VDD/2 (after DRAM is initialized)		-18	-	18	uA	

Notes:
1. VDDQ tracks with VDD; VDDQ and VDD are tied together.
2. DC bandwidth is limited to 20 MHz.
3. VREFCA must not be greater than 0.6 x VDD. When VDD is less than 500mV, VREF may be less than or equal to 300mV.
4. VTT termination voltages in excess of specification limit will adversely affect command and address signals' voltage margins, and reduce timing margins.
5. Tied to ground. Not connected to edge connector.

Operating Temperature Condition

Symbol	Parameter		Rating	Units	Notes
TOPER	Operating temperature	Commercial	0 to 95	^{0}C	1,2
		Industrial	-40 to +95		

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51-2.
2. At -40^{o}C to +85^{o}C, operation temperature range, all DRAM specifications will be supported. The refresh rate is required to double when 85^{o}C < TOPER <= 95^{o}C.

Speed Bins

Symbol	N7 DDR4-2400 (17-17-17)[1]	N6 DDR4-2133 (15-15-15)[1]	M4 DDR4-1866 (13-13-13)[1]	K2 DDR4-1600 (11-11-11)[1]	Unit
tCK(min)	0.833	0.938	1.071	1.25	ns
CAS Latency	17	15	13	11	nCK
tRCD(min)	14.16	14.06	13.92	13.75	ns
tRP(min)	14.16	14.06	13.92	13.75	ns
tRAS(min)	32	33	34	35	ns
tRC(min)	46.16	47.06	47.92	48.75	ns

Note: 1. Speed bin is in order of CL-tRCD-tRP

Command/Address Input Levels

Symbol	Parameter	N7/N6/M4/K2 DDR4-2133/2400/1866/1600		Unit	Note
		Min	Max		
VIH(DC)	DC Input High (Logic 1) Voltage	VREF + 0.075	VDD	V	1,2,3
VIL(DC)	DC Input Low (Logic 0) Voltage	VSS	VREF - 0.075	V	1,2
VIH(AC)	AC Input High (Logic 1) Voltage	VREF + 0.100	VDD	V	1,2
VIL(AC)	AC Input Low (Logic 0) Voltage	VSS	VREF - 0.100	V	1,2,3

Notes:
1. For input except RESET#. VREF = VREFCA(DC).
2. VREF = VREFCA(DC).
3. Input signal must meet VIL/VIH(AC) to meet tIS/tIH timings.

AC & DC Output Levels

Symbol	Parameter	Value	Unit	Note
VOH(DC)	DC output high measurement level (for IV curve linearity)	1.1 x VDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.8 x VDDQ	V	
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.5 x VDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	(0.7 + 0.15) x VDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) x VDDQ	V	1
VOHdiff(AC)	AC differential output high measurement level (for output SR)	+0.3 x VDDQ	V	2
VOLdiff(AC)	AC differential output low measurement level (for output SR)	-0.3 x VDDQ	V	2

Notes:
1. The swing of ± 0.15 × VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT = VDDQ.
2. The swing of ± 0.3 × VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT = VDDQ.

Input/Output Capacitance

TA=25^{0}C, f=100MHz

Parameter	Symbol	N7 (DDR4-2400)		Unit
		Min	Max	
Input capacitance (BA0~BA1, BG0~BG1, A0~A13, RAS#/A16, CAS#/A15, WE#/A14, ACT#)	CIN1	5.8	10.3	pF
Input capacitance (CKE0, ODT0, CS0#)	CIN2	5.8	10.3	pF
Input capacitance (CK0, CK0#)	CIN3	5.8	10.3	pF
Input/Output capacitance (DQ, DQS, DQS#, DM#, CB)	CIO	4.6	5.2	pF

IDD & IPP Specifications

Parameter	Symbol	N7 (DDR4-2400)	Unit
One bank ACTIVATE-PRECHARGE current	IDD0	243	mA
One bank ACTIVATE-PRECHARGE, word line boost, IPP current	IPP0	36	mA
One bank ACTIVATE-READ-PRECHARGE current	IDD1	288	mA
Precharge standby current	IDD2N	162	mA
Precharge standby ODT current	IDD2NT	162	mA
Precharge power-down current	IDD2P	99	mA
Precharge quiet standby current	IDD2Q	153	mA
Active standby current	IDD3N	243	mA
Active standby IPP current	IPP3N	27	mA
Active power-down current	IDD3P	171	mA
Burst read current	IDD4R	738	mA
Burst write current	IDD4W	720	mA
Burst refresh current (1 x REF)	IDD5B	1665	mA
Burst refresh IPP current (1 x REF)	IPP5B	162	mA
Self refresh current: Normal temperature range (0°C to +85°C)	IDD6N	189	mA
Self refresh current: Extended temperature range (0°C to +95°C)	IDD6E	306	mA
Self refresh current: Reduced temperature range (0°C to +45°C)	IDD6R	135	mA
Auto self refresh current	IDD6A	189	mA
Bank interleave read current	IDD7	1215	mA
Bank interleave read IPP current	IPP7	90	mA
Maximum power-down current	IDD8	81	mA

Note:
IDD specification is based on Samsung C-die components.

AC TIMING PARAMETERS & SPECIFICATIONS

Speed		N7 DDR4-2400		N6 DDR4-2133		M4 DDR4-1866		K2 DDR4-1600		Units
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
Clock Timing										
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	8	20	ns
Average Clock Period	tCK(avg)	0.833	<0.937	0.937	<1.071	1.071	<1.25	1.25	<1.5	ns
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)
Absolute Clock Period	tCK(abs)	MIN : tCK(avg)min + tJIT(per)min_tot MAX : tCK(avg)max + tJIT(per)max_tot								tCK(avg)
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)
Clock Period Jitter- total	JIT(per)_tot	-42	42	-47	47	-54	54	-63	63	ps
Clock Period Jitter- deterministic	JIT(per)_dj	-21	21	-23	23	-27	27	-31	31	ps
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-33	33	-38	38	-43	43	-50	50	ps
Cycle to Cycle Period Jitter	tJIT(cc)	-	83	-	94	-	107	-	125	ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	-	67	-	75	-	86	-	100	ps
Cumulative error across 2 cycles	tERR(2per)	-61	61	-69	69	-79	79	-92	92	ps
Cumulative error across 3 cycles	tERR(3per)	-73	73	-82	82	-94	94	-109	109	ps
Cumulative error across 4 cycles	tERR(4per)	-81	81	-91	91	-104	104	-121	121	ps
Cumulative error across 5 cycles	tERR(5per)	-87	87	-98	98	-112	112	-131	131	ps
Cumulative error across 6 cycles	tERR(6per)	-92	92	-104	104	-119	119	-139	139	ps
Cumulative error across 7 cycles	tERR(7per)	-97	97	-109	109	-124	124	-145	145	ps
Cumulative error across 8 cycles	tERR(8per)	-101	101	-113	113	-129	129	-151	151	ps
Cumulative error across 9 cycles	tERR(9per)	-104	104	-117	117	-134	134	-156	156	ps
Cumulative error across 10 cy- cles	tERR (10per)	-107	107	-120	120	-137	137	-160	160	ps
Cumulative error across 11 cy- cles	tERR (11per)	-110	110	-123	123	-141	141	-164	164	ps
Cumulative error across 12 cy- cles	tERR (12per)	-112	112	-126	126	-144	144	-168	168	ps
Cumulative error across 13 cy- cles	tERR (13per)	-114	114	-129	129	-147	147	-172	172	ps
Cumulative error across 14 cy- cles	tERR (14per)	-116	116	-131	131	-150	150	-175	175	ps
Cumulative error across 15 cy- cles	tERR (15per)	-118	118	-133	133	-152	152	-178	178	ps
Cumulative error across 16 cy- cles	tERR (16per)	-120	120	-135	135	-155	155	-180	189	ps
Cumulative error across 17 cy- cles	tERR (17per)	-122	122	-137	137	-157	157	-183	183	ps
Cumulative error across 18 cy- cles	tERR (18per)	-124	124	-139	139	-159	159	-185	185	ps
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	MIN : tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) MAX : tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)								ps
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base)	62	-	80	-	100	-	115	-	ps
Command and Address setup time to CK, CK# referenced to Vref levels	tIS(Vref)	162	-	180	-	200	-	215	-	ps
Command and Address hold time to CK, CK# referenced to Vih(dc) / Vil(dc) levels	tIH(base)	87	-	105	-	125	-	140	-	ps
Command and Address hold time to CK, CK# referenced to Vref levels	tIH(Vref)	162	-	180	-	200	-	215	-	ps
Control and Address Input pulse width for each input	tIPW	410	-	460	-	525	-	600	-	ps

AC TIMING PARAMETERS & SPECIFICATIONS

Speed		N7 DDR4-2400		N6 DDR4-2133		M4 DDR4-1866		K2 DDR4-1600		Units
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Command and Address Timing										
CAS# to CAS# command de- lay for same bank group	tCCD_L	max(5 nCK, 5 ns)	-	max(5 nCK, 5.355 ns)	-	max(5 nCK, 5.355 ns)	-	max(5 nCK, 6.250 ns)	-	nCK
CAS# to CAS# command de- lay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	nCK
ACTIVATE to ACTIVATE Com- mand delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nC K,5.3ns)	-	Max(4nC K,5.3ns)	-	Max(4nC K,5.3ns)	-	Max(4nC K,6ns)	-	nCK
ACTIVATE to ACTIVATE Com- mand delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nC K,3.3ns)	-	Max(4nC K,3.7ns)		Max(4nC K,4.2ns)		Max(4nC K,5ns)		nCK
ACTIVATE to ACTIVATE Com- mand delay to different bank group for 1/2KB page size	tRRD_S(1/ 2K)	Max(4nC K,3.3ns)	-	Max(4nC K,3.7ns)		Max(4nC K,4.2ns)		Max(4nC K,5ns)		nCK
ACTIVATE to ACTIVATE Com- mand delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nC K,6.4ns)	-	Max(4nC K,6.4ns)		Max(4nC K,6.4ns)		Max(4nC K,7.5ns)		nCK
ACTIVATE to ACTIVATE Com- mand delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nC K,4.9ns)	-	Max(4nC K,5.3ns)		Max(4nC K,5.3ns)		Max(4nC K,6ns)		nCK
ACTIVATE to ACTIVATE Com- mand delay to same bank group for 1/2KB page size	tRRD_L(1/ 2K)	Max(4nC K,4.9ns)	-	Max(4nC K,5.3ns)		Max(4nC K,5.3ns)		Max(4nC K,6ns)		nCK
Four activate window for 2KB page size	tFAW_2K	Max(28n CK,30ns)	-	Max(28n CK,30ns)		Max(28n CK,30ns)		Max(28n CK,35ns)		ns
Four activate window for 1KB page size	tFAW_1K	Max(20n CK,21ns)	-	Max(20n CK,21ns)		Max(20n CK,23ns)		Max(20n CK,25ns)		ns
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16n CK,13ns)	-	Max(16n CK,15ns)		Max(16n CK,17ns)		Max(16n CK,20ns)		ns
Delay from start of internal write transaction to internal read com- mand for different bank group	tWTR_S	Max (2nCK, 2.5ns)	-	max(2nC K,2.5ns)	-	max(2nC K,2.5ns)	-	max(2nC K,2.5ns)	-	ns
Delay from start of internal write transaction to internal read com- mand for same bank group	tWTR_L	max (4nCK,7.5 ns)	-	max(4nC K,7.5ns)	-	max(4nC K,7.5ns)	-	max(4nC K,7.5ns)	-	
Internal READ Command to PRECHARGE Command delay	tRTP	max (4nCK,7.5 ns)	-	max(4nC K,7.5ns)	-	max(4nC K,7.5ns)	-	max(4nC K,7.5ns)	-	
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	ns
Write recovery time when CRC and DM are enabled	tWR_CRC _DM	tWR+max (5nCK,3.7 5ns)	-	tWR+max (5nCK,3.7 5ns)	-	tWR+max (5nCK,3.7 5ns)	-	tWR+max (4nCK,3.7 5ns)	-	ns
Delay from start of internal write transaction to internal read com- mand for different bank group with both CRC and DM enabled	tWTR_S_C RC_DM	tWTR_S+ max (5nCK,3.7 5ns)	-	tWTR_S+ max (5nCK,3.7 5ns)	-	tWTR_S+ max (5nCK,3.7 5ns)	-	tWTR_S+ max (4nCK,3.7 5ns)	-	ns
Delay from start of internal write transaction to internal read com- mand for same bank group with both CRC and DM enabled	tWTR_L_C RC_DM	tWTR_L+ max (5nCK,3.7 5ns)	-	tWTR_L+ max (5nCK,3.7 5ns)	-	tWTR_L+ max (5nCK,3.7 5ns)	-	tWTR_L+ max (4nCK,3.7 5ns)	-	ns
DLL locking time	tDLLK	768	-	768	-	597	-	597	-	nCK
Mode Register Set command cy- cle time	tMRD	8	-	8	-	8	-	8	-	nCK
Mode Register Set command up- date delay	tMOD	max(24n CK,15ns)	-	max(24n CK,15ns)	-	max(24n CK,15ns)	-	max(24n CK,15ns)	-	nCK
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	nCK
Multi Purpose Register Write Re- covery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))								nCK
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	0.5	-	UI
DQ0 or DQL0 driven to 0 hold time from last DQS falling edge	tPDA_H	0.5	-	0.5	-	0.5	-	0.5	-	UI

AC TIMING PARAMETERS & SPECIFICATIONS

Speed		N7 DDR4-2400		N6 DDR4-2133		M4 DDR4-1866		K2 DDR4-1600		Units
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
CS# to Command Address Latency										
CS# to Command Address La- tency	tCAL	max(3 nCK, 3.748 ns)	-	max(3 nCK, 3.748 ns)	-	max(3 nCK, 3.748 ns)	-	max(3 nCK, 3.748 ns)	-	nCK
Mode Register Set command cy- cle time in CAL mode	tMRD_tCAL	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	nCK
Mode Register Set update delay in CAL mode	tMOD_tCAL	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	nCK
DRAM Data Timing										
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	0.17	-	0.16	-	0.16	-	0.16	tCK(avg) /2
DQ output hold time per group, per access from DQS, DQS#	tQH	0.74	-	0.76	-	0.76	-	0.76	-	tCK(avg) /2
Data Valid Window per device, per UI: (tQH - tDQSQ) of each UI on a given DRAM	tDVWd	0.64	-	0.64	-	0.63	-	0.63	-	UI
Data Valid Window, per pin, per UI: (tQH - tDQSQ) each UI on a pin of a given DRAM	tDVWp	0.72	-	0.69	-	0.66	-	0.66	-	UI
DQ low impedance time from CK, CK#	tLZ(DQ)	-330	175	-360	180	-390	195	-450	225	ps
DQ high impedance time from CK, CK#	tHZ(DQ)	-	175	-	180	-	195	-	225	ps
Data Strobe Timing										
DQS, DQS# differential READ Pre-amble (1 clock preamble)	tRPRE	0.9	NOTE 1	0.9	NOTE 1	0.9	NOTE 1	0.9	NOTE 1	tCK
DQS, DQS# differential READ Preamble (2 clock preamble)	tRPRE2	1.8	NOTE 1	NA	NA	NA	NA	NA	NA	tCK
DQS, DQS# differential READ Postamble	tRPST	0.33	NOTE 2	0.33	NOTE 2	0.33	NOTE 2	0.33	NOTE 2	tCK
DQS, DQS# differential output high time	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	tCK
DQS, DQS# differential output low time	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	tCK
DQS, DQS# differential WRITE Preamble (1 clock pream- ble)	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK
DQS, DQS# differential WRITE Preamble (2 clock pream- ble)	tWPRE2	1.8	-	NA		NA		NA		tCK
DQS, DQS# differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	0.33	-	tCK
DQS and DQS# low-imped- ance time (Referenced from RL- 1)	tLZ(DQS)	-330	175	-360	180	-390	195	-450	225	ps
DQS and DQS# high-imped- ance time (Referenced from RL+BL/2)	tHZ(DQS)	-	175	-	180	-	195	-	225	ps
DQS, DQS# differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK
DQS, DQS# differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK
DQS, DQS# rising edge to CK, CK# rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK
DQS, DQS# rising edge to CK, CK# rising edge (2 clock preamble)	tDQSS2	-0.5	0.5	N/A	N/A	N/A	N/A	N/A	N/A	tCK
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	tCK
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	tCK
DQS, DQS# rising edge out- put timing location from rising CK, CK# with DLL On mode	tDQSCK (DLL On)	-175	175	-180	180	-195	195	-225	225	ps
DQS, DQS# rising edge out- put variance window per DRAM	tDQSCKI (DLL On)	-	290	-	310	-	330	-	370	ps

AC TIMING PARAMETERS & SPECIFICATIONS

Speed		N7 DDR4-2400		N6 DDR4-2133		M4 DDR4-1866		K2 DDR4-1600		Units
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
MPSM Timing										
Command path disable delay upon MPSM entry	tMPED	$t_{MOD(min)} + t_{CP-DED(min)}$	-	$t_{MOD(min)} + t_{CP-DED(min)}$	-	$t_{MOD(min)} + t_{CP-DED(min)}$	-	$t_{MOD(min)} + t_{CP-DED(min)}$	-	
Valid clock requirement after MPSM entry	tCKMPE	$t_{MOD(min)} + t_{CP-DED(min)}$	-	$t_{MOD(min)} + t_{CP-DED(min)}$	-	$t_{MOD(min)} + t_{CP-DED(min)}$	-	$t_{MOD(min)} + t_{CP-DED(min)}$	-	
Valid clock requirement before MPSM exit	tCKMPX	$t_{CKSRX(min)}$	-	$t_{CKSRX(min)}$	-	$t_{CKSRX(min)}$	-	$t_{CKSRX(min)}$	-	
Exit MPSM to commands not requiring a locked DLL	tXMP	$t_{XS(min)}$	-	$t_{XS(min)}$	-	$t_{XS(min)}$	-	$t_{XS(min)}$	-	
Exit MPSM to commands requir- ing a locked DLL	tXMPDLL	$t_{XMP(min)} + t_{XS-DLL(min)}$	-	$t_{XMP(min)} + t_{XS-DLL(min)}$	-	$t_{XMP(min)} + t_{XS-DLL(min)}$	-	$t_{XMP(min)} + t_{XS-DLL(min)}$	-	
CS setup time to CKE	tMPX_S	$t_{IS(min)} + t$	-	$t_{IS(min)} + t$	-	$t_{IS(min)} + t$	-	$t_{IS(min)} + t$	-	
CS# High hold time to CKE ris- ing edge	tMPX_HH	$t_{XP(min)}$	-	$t_{XP(min)}$	-	$t_{XP(min)}$	-	$t_{XP(min)}$	-	
CS# Low hold time to CKE ris- ing edge	tMPX_LH	12	t_{XMP} + 10ns	12	t_{XMP} + 10ns	12	t_{XMP} + 10ns	12	t_{XMP} + 10ns	ns
Calibration Timing										
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	nCK
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	nCK
Normal operation Short calibra- tion time	tZQCS	128	-	128	-	128	-	128	-	nCK
Reset/Self Refresh Timing										
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-	nCK
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	nCK
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tX-S_ABORT(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	nCK
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	nCK
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	nCK
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	nCK
Valid Clock Requirement after Self Refresh Entry (SRE) or Pow- er-Down Entry (PDE)	tCKSRE	max (5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	nCK
Valid Clock Requirement after Self Refresh Entry (SRE) or Pow- er-Down when CA Parity is en- abled	tCKS-RE_PAR	max (5nCK,10ns)+PL	-	max (5nCK,10ns)+PL	-	max (5nCK,10ns)+PL	-	max (5nCK,10ns)+PL	-	nCK
Valid Clock Requirement before Self Refresh Exit (SRX) or Pow- er-Down Exit (PDX) or Reset Exit	tCKSRX	max (5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	nCK
Power Down Timing										
Exit Power Down with DLL on to any valid command; Exit Pre- charge Power Down with DLL fro- zen to commands not requiring a locked DLL	tXP	max (4nCK, 6ns)	-	max (4nCK, 6ns)	-	max (4nCK, 6ns)	-	max (4nCK, 6ns)	-	nCK
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	nCK
Command pass disable delay	tCPDED	4	-	4	-	4	-	4	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	nCK

AC TIMING PARAMETERS & SPECIFICATIONS

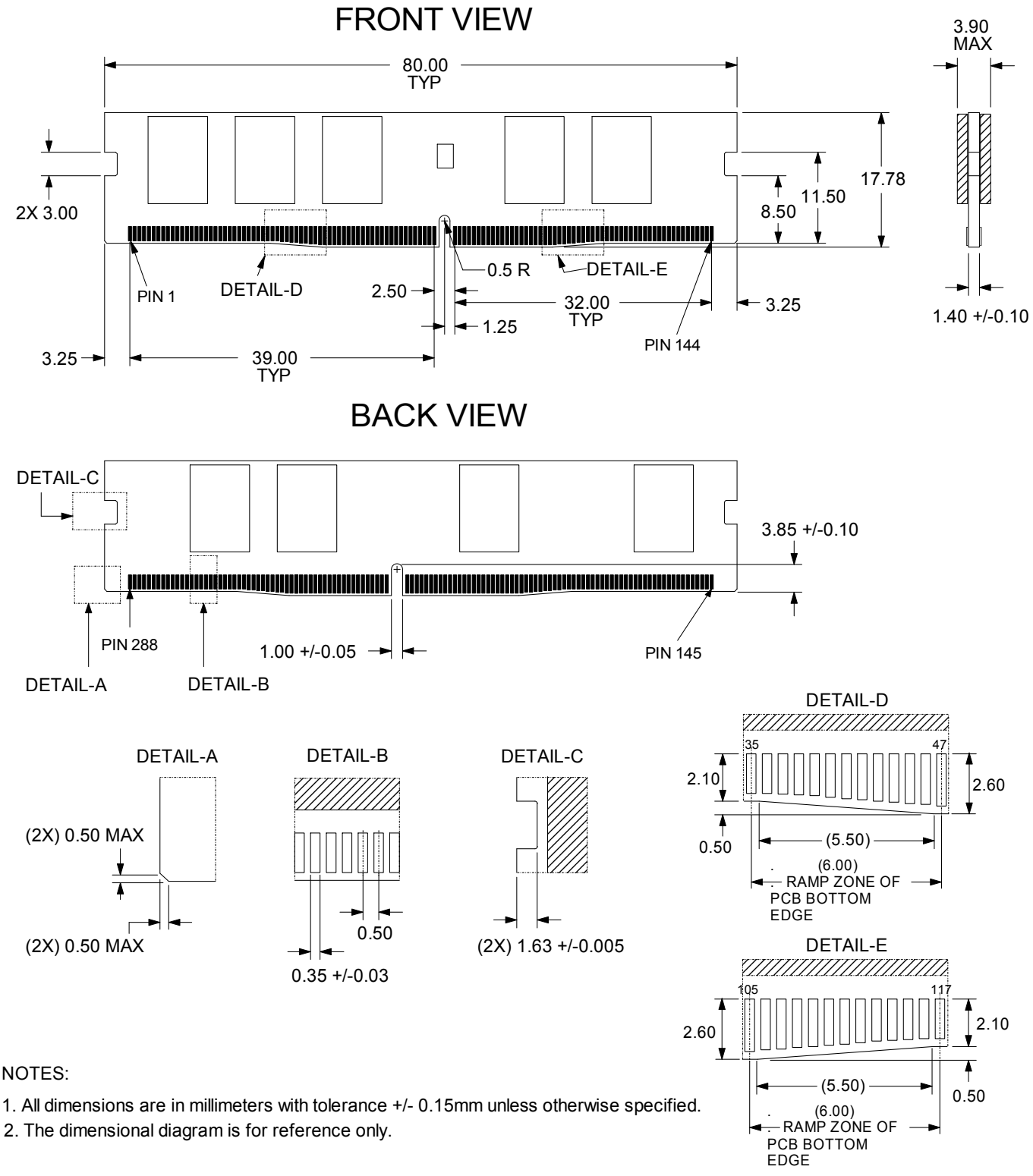
Speed		N7 DDR4-2400		N6 DDR4-2133		M4 DDR4-1866		K2 DDR4-1600		Units
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Timing of ACT command to Pow- er Down entry	tACTPDEN	2	-	2	-	1	-	1	-	nCK
Timing of PRE or PREA com- mand to Power Down entry	tPRPDEN	2	-	2	-	1	-	1	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(t WR/ tCK(avg))	-	WL+4+(t WR/ tCK(avg))	-	WL+4+(t WR/ tCK(avg))	-	WL+4+(t WR/ tCK(avg))	-	nCK
Timing of WRA command to Pow- er Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+W R+1	-	WL+4+W R+1	-	WL+4+W R+1	-	WL+4+W R+1	-	nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRP- BC4DEN	WL+2+(t WR/ tCK(avg))	-	WL+2+(t WR/ tCK(avg))	-	WL+2+(t WR/ tCK(avg))	-	WL+2+(t WR/ tCK(avg))	-	nCK
Timing of WRA command to Pow- er Down entry (BC4MRS)	tWRAP- BC4DEN	WL+2+W R+1	-	WL+2+W R+1	-	WL+2+W R+1	-	WL+2+W R+1	-	nCK
Timing of REF command to Pow- er Down entry	tREFPDEN	2	-	2	-	1	-	1	-	nCK
Timing of MRS command to Pow- er Down entry	tMRSPDEN	tMOD(mi n)	-	tMOD(mi n)	-	tMOD(mi n)	-	tMOD(mi n)	-	
PDA Timing										
Mode Register Set command cy- cle time in PDA mode	tMRD_PDA	max(16n CK,10ns)	-	max(16n CK,10ns)	-	max(16n CK,10ns)	-	max(16n CK,10ns)	-	nCK
Mode Register Set command up- date delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		tMOD		
ODT Timing										
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)
Write Leveling Timing										
First DQS/DQS# rising edge after write leveling mode is pro- grammed	tWLMRD	40	-	40	-	40	-	40	-	nCK
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	nCK
Write leveling setup time from ris- ing CK, CK# crossing to rising DQS/DQS# crossing	tWLS	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)
Write leveling hold time from ris- ing DQS/DQS# crossing to ris- ing CK, CK# crossing	tWLH	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	ns
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	ns
CA Parity Timing										
Commands not guaranteed to be executed during this time	tPAR_UN- KNOWN	-	PL	-	PL	-	PL	-	PL	
Delay from errant command to ALERT# assertion	tPAR_ALER T_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	
Pulse width of ALERT# signal when asserted	tPAR_ALER T_PW	72	144	64	128	56	112	48	96	nCK
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALER T_RSP	-	64	-	57	-	50	-	43	nCK
Parity Latency	PL	5		4		4		4		nCK
CRC Error Reporting										
CRC error to ALERT# latency	tCRC_ALE RT	3	13	3	13	3	13	3	13	ns
CRC ALERT# pulse width	CRC_ALER T_PW	6	10	6	10	6	10	6	10	nCK

AC TIMING PARAMETERS & SPECIFICATIONS

Speed		N7 DDR4-2400		N6 DDR4-2133		M4 DDR4-1866		K2 DDR4-1600		Units
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
Geardown timing										
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	tX-PR_GEAR	-	-	-	-	-	-	-	-	
CKE High Assert to Gear Down Enable time(T2/CKE)	tXS_GEAR	-	-	-	-	-	-	-	-	
MRS command to Sync pulse time(T3)	tSYN-C_GEAR	-	-	-	-	-	-	-	-	
Sync pulse to First valid com- mand(T4)	tCM-D_GEAR	-	-	-	-	-	-	-	-	
Geardown setup time	tGEAR_set- up	-	-	-	-	-	-	-	-	nCK
Geardown hold time	tGEAR_hold	-	-	-	-	-	-	-	-	nCK
tREFI										
tRFC1 (min) 550ns setting (NOTE 3,4)	2Gb	160	-	160	-	160	-	160	-	ns
	4Gb	260	-	260	-	260	-	260	-	ns
	8Gb	350	-	350	-	350	-	350	-	ns
	16Gb	550	-	550	-	550	-	550	-	ns
tRFC1 (min)_350ns setting	16Gb	350	-	350	-	350	-	350	-	ns
tRFC2 (min) 550ns setting (NOTE 3,4)	2Gb	110	-	110	-	110	-	110	-	ns
	4Gb	160	-	160	-	160	-	160	-	ns
	8Gb	260	-	260	-	260	-	260	-	ns
	16Gb	350	-	350	-	350	-	350	-	ns
tRFC2 (min)_350ns setting	16Gb	260	-	260	-	260	-	260	-	ns
tRFC4 (min) 550ns setting (NOTE 3,4)	2Gb	90	-	90	-	90	-	90	-	ns
	4Gb	110	-	110	-	110	-	110	-	ns
	8Gb	160	-	160	-	160	-	160	-	ns
	16Gb	260	-	260	-	260	-	260	-	ns
tRFC4 (min)_350ns setting	16Gb	160	-	160	-	160	-	160	-	ns

Note:
1. The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. Boundary of DQS Low-Z occur one cycle earlier in 2tCK toggle mode.
2. DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point.
3. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
4. 16Gb A-die 2Gx8 product supports both tRFC1 550ns and 350ns setting. It depends on customer's preference. tRFC2 and tRFC4 needs to be set corresponding to each setting values.

Package Dimensions



NOTES:

1. All dimensions are in millimeters with tolerance +/- 0.15mm unless otherwise specified.
2. The dimensional diagram is for reference only.

Revision History:

Date	Rev.	Page	Changes
03/04/2019	1.0	All	Spec release
08/06/2019	1.1	1	Typo correction