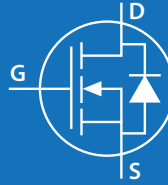


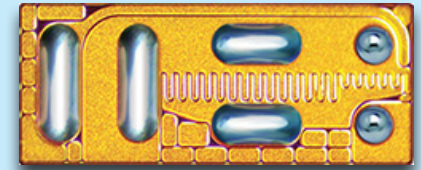
## EPC8010 – Enhancement Mode Power Transistor

 $V_{DS}$ , 100 V $R_{DS(on)}$ , 160 mΩ $I_D$ , 4 A

Revised July 5, 2023

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low  $R_{DS(on)}$ , while its lateral device structure and majority carrier diode provide exceptionally low  $Q_G$  and zero  $Q_{RR}$ . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Questions:  
Ask a GaN  
Expert



Die size: 2.1 x 0.85 mm

EPC8010 eGaN FETs are supplied only in passivated die form with solder bars.

**Applications**

- Ultra high speed DC-DC conversion
- RF envelope tracking
- Wireless power transfer
- Game console and industrial movement sensing (lidar)

**Benefits**

- Ultra high efficiency
- Ultra low  $R_{DS(on)}$
- Ultra low  $Q_G$
- Ultra small footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC8010>

**Maximum Ratings**

PARAMETER		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage (Continuous)	100	V
$I_D$	Continuous ( $T_A = 25^\circ\text{C}$ , $R_{\theta JA} = 27^\circ\text{C/W}$ )	4	A
	Pulsed ( $25^\circ\text{C}$ , $T_{PULSE} = 300 \mu\text{s}$ )	7.5	
$V_{GS}$	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
$T_J$	Operating Temperature	-40 to 150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature	-40 to 150	

**Thermal Characteristics**

PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	8.2	$^\circ\text{C/W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	16	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	82	

Note 1:  $R_{\theta JA}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See [https://epc-co.com/epc/documents/product-training/Appnote\\_Thermal\\_Performance\\_of\\_eGaN\\_FETs.pdf](https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf) for details

**Static Characteristics ( $T_J = 25^\circ\text{C}$  unless otherwise stated)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V}$ , $I_D = 125 \mu\text{A}$	100		V	
$I_{DSS}$	Drain-Source Leakage	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 80 \text{ V}$	20	100	$\mu\text{A}$	
$I_{GSS}$	Gate-to-Source Forward Leakage	$V_{GS} = 5 \text{ V}$	0.1	0.5	$\text{mA}$	
	Gate-to-Source Reverse Leakage	$V_{GS} = -4 \text{ V}$	20	100	$\mu\text{A}$	
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 0.25 \text{ mA}$	80	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5 \text{ V}$ , $I_D = 0.5 \text{ A}$	120	160	$\text{m}\Omega$	
$V_{SD}$	Source-Drain Forward Voltage <sup>#</sup>	$V_{GS} = 0 \text{ V}$ , $I_S = 0.5 \text{ A}$	2.5		V	

<sup>#</sup> Defined by design. Not subject to production test.

All measurements were done with substrate connected to source.

Specifications are with substrate connected to source where applicable.

Dynamic Characteristics ( $T_J = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{ISS}$	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}$		43	55	pF
$C_{OSS}$	Output Capacitance			25	36	
$C_{RSS}$	Reverse Transfer Capacitance			0.3	0.5	
$R_G$	Gate Resistance			0.3		$\Omega$
$Q_G$	Total Gate Charge	$V_{GS} = 5\text{ V}, V_{DS} = 50\text{ V}, I_D = 1\text{ A}$		360	480	pC
$Q_{GS}$	Gate-to-Source Charge			130		
$Q_{GD}$	Gate-to-Drain Charge	$V_{DS} = 50\text{ V}, I_D = 1\text{ A}$		60	100	
$Q_{G(TH)}$	Gate Charge at Threshold			100		
$Q_{OSS}$	Output Charge	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}$		2200	3300	
$Q_{RR}$	Source-Drain Recovery Charge			0		

# Defined by design. Not subject to production test.  
 All measurements were done with substrate connected to source.  
 Specifications are with substrate connected to source where applicable.

Figure 1: Typical Output Characteristics at 25°C

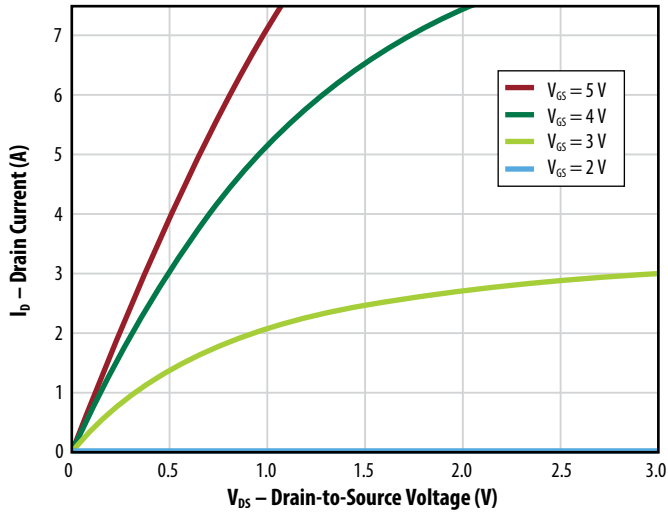


Figure 2: Typical Transfer Characteristics

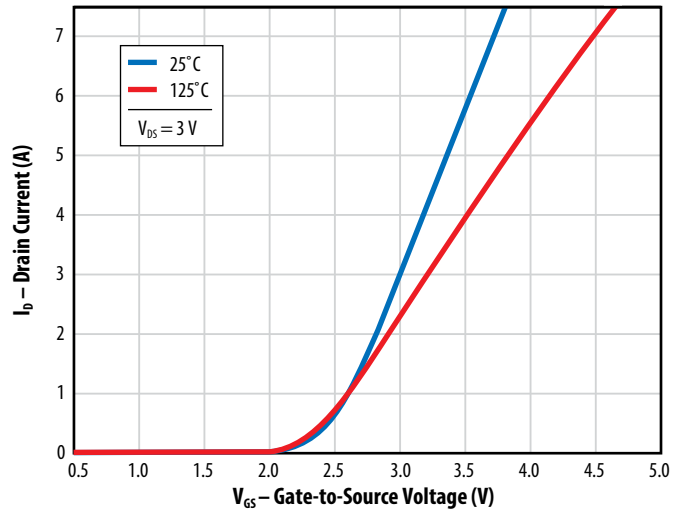


Figure 3: Typical  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Drain Currents

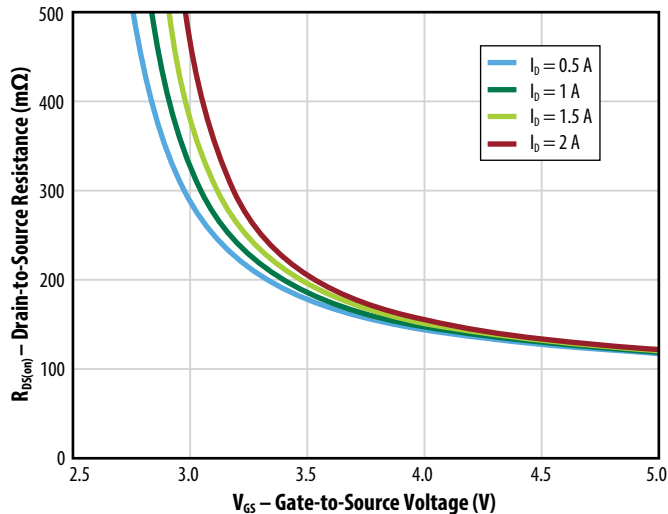


Figure 4: Typical  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Temperatures

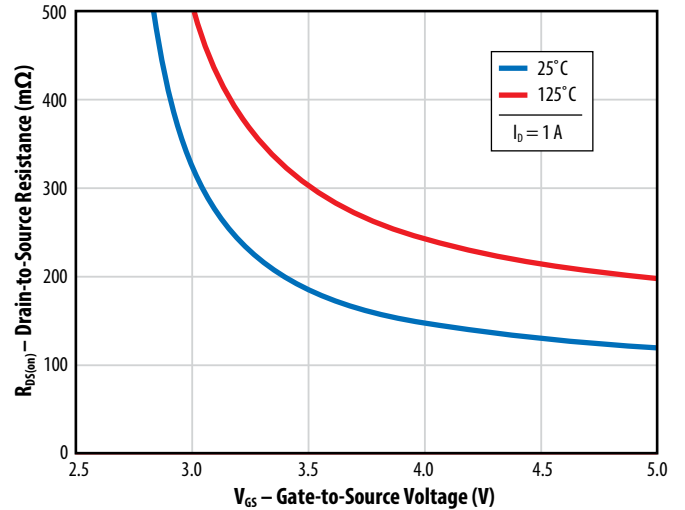


Figure 5a: Typical Capacitance (Linear Scale)

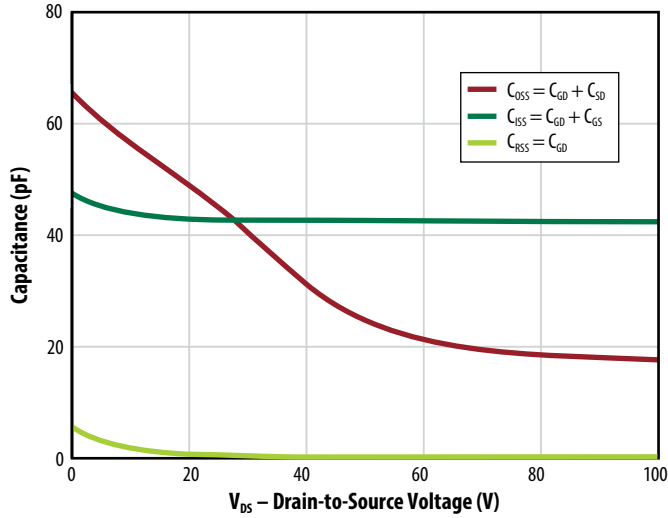


Figure 5b: Typical Capacitance (Log Scale)

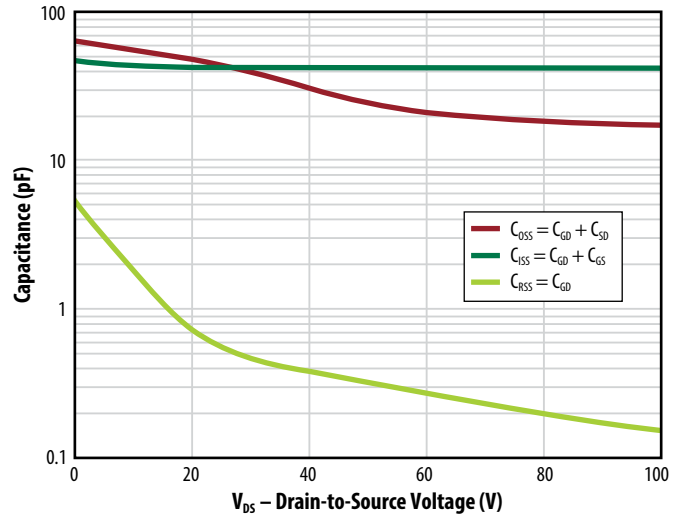


Figure 6: Typical Gate Charge

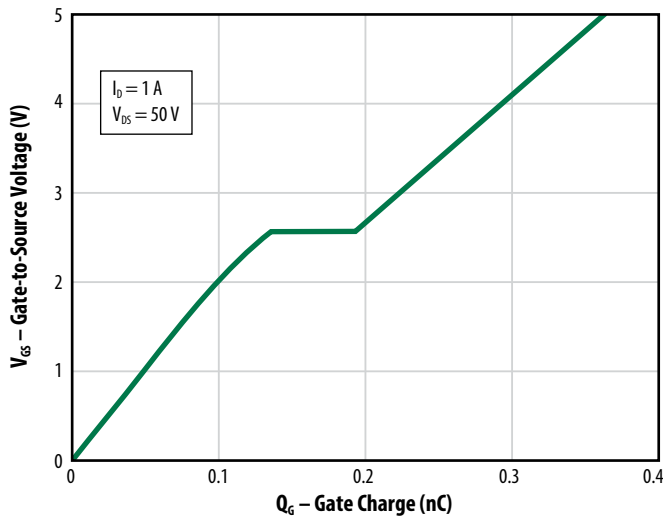
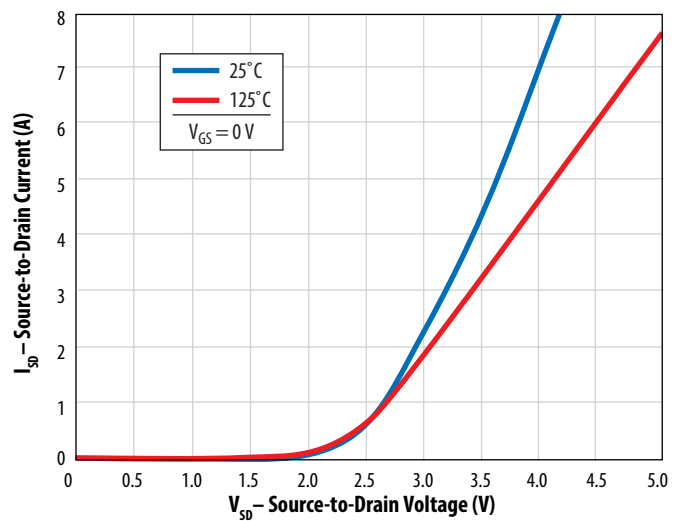


Figure 7: Typical Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

Figure 8: Typical Normalized On-State Resistance vs. Temp.

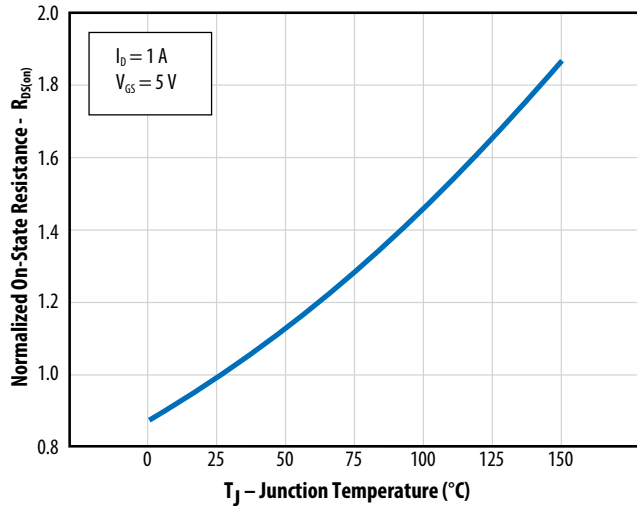


Figure 9: Typical Normalized Threshold Voltage vs. Temp.

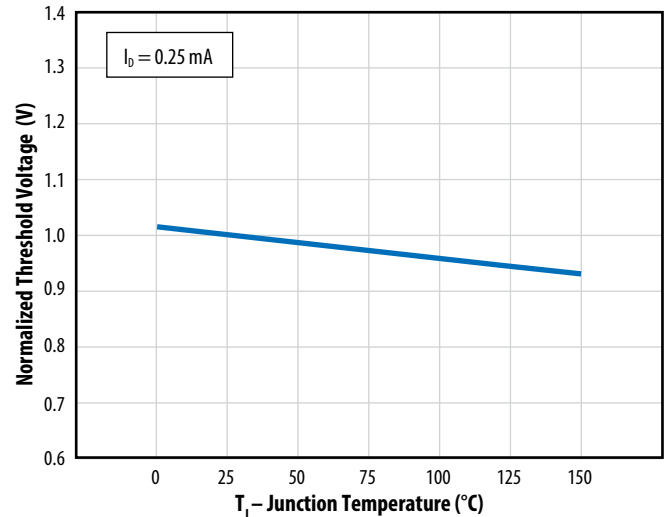


Figure 10: Typical Gate Leakage Current

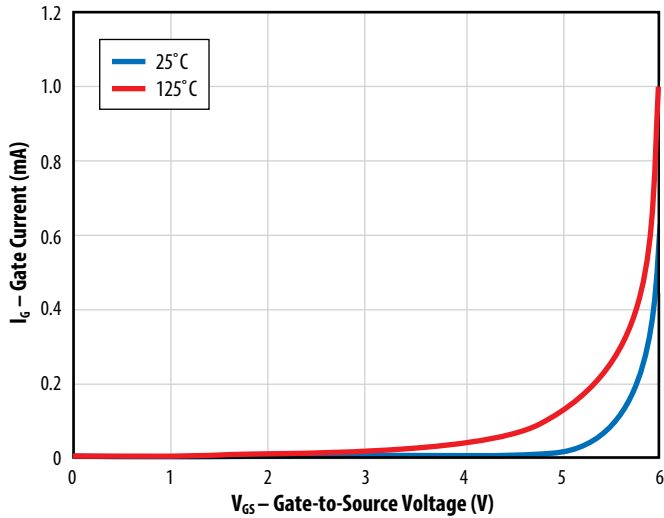


Figure 11: Smith Chart

S-Parameter Characteristics  
 $V_{GSQ} = 1.34\text{ V}$ ,  $V_{DSQ} = 50\text{ V}$ ,  $I_{DQ} = 0.50\text{ A}$   
 Pulsed Measurement, Heat-Sink Installed,  $Z_0 = 50\ \Omega$

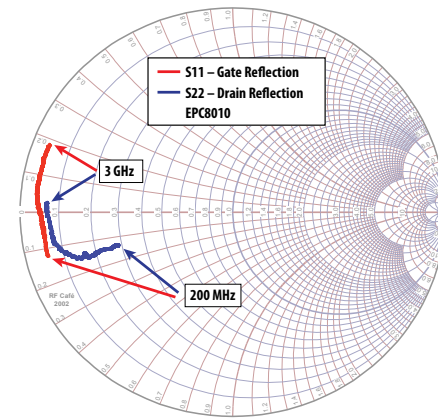


Figure 12: Gain Chart

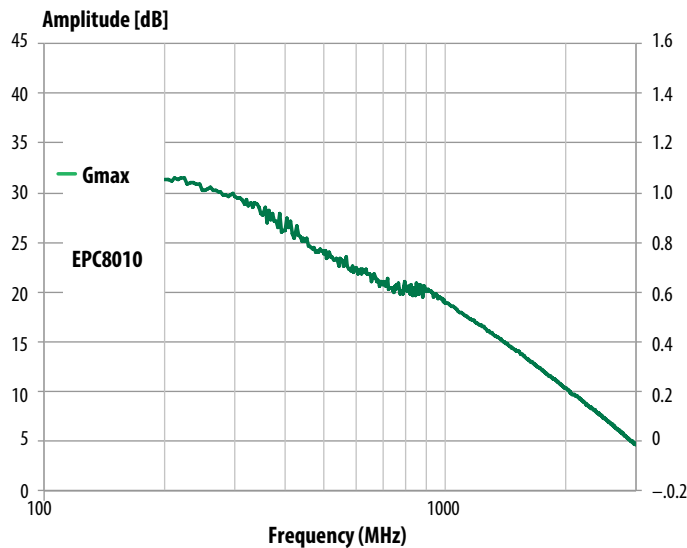


Figure 13: Device Reflection

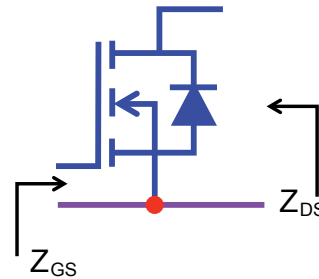
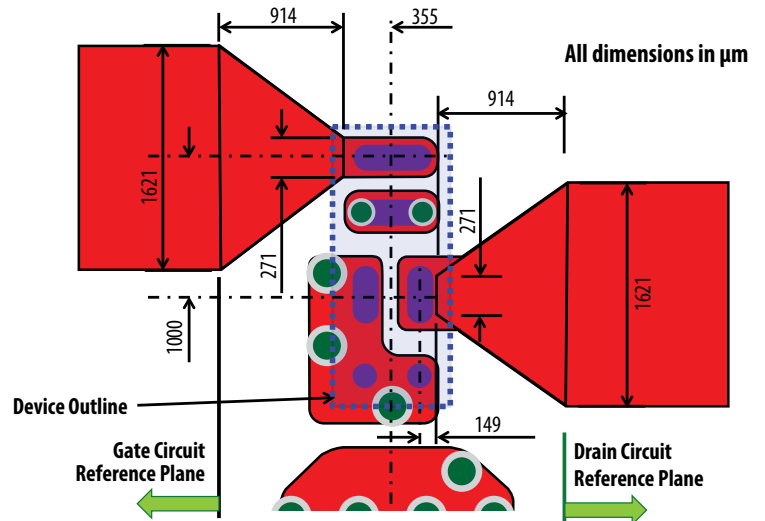


Figure 14: Taper and Reference Plane details – Device Connection

Micro-Strip design: 2-layer  
 1/2 oz (17.5 μm) thick copper  
 30 mil thick R04350 substrate



Frequency [MHz]	Gate ( $Z_{GS}$ ) [Ω]	Drain ( $Z_{DS}$ ) [Ω]
200	2.54 - j11.18	22.54 - j23.91
500	1.57 - j4.20	6.01 - j15.53
1000	0.94 - j0.23	1.85 - j6.89
1200	0.97 + j0.89	1.47 - j4.87
1500	0.97 + j2.38	1.51 - j2.52
2000	1.08 + j4.80	2.09 + j0.41
2400	1.21 + j6.74	2.50 + j2.25
3000	1.62 + j10.34	3.05 + j5.00

S-Parameter Table - Download S-parameter files at [www.epc-co.com](http://www.epc-co.com)

Figure 15: Typical Transient Thermal Response Curves

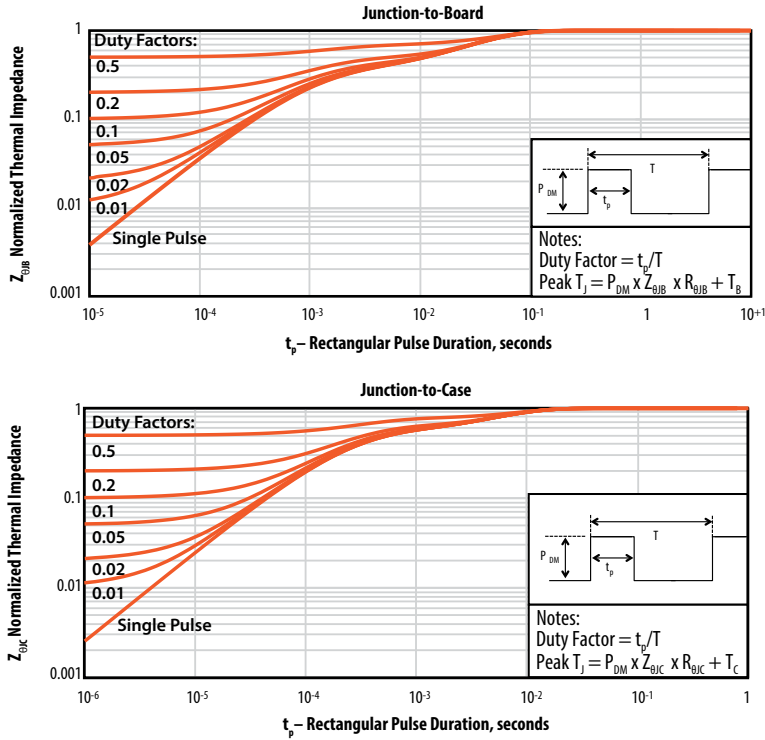
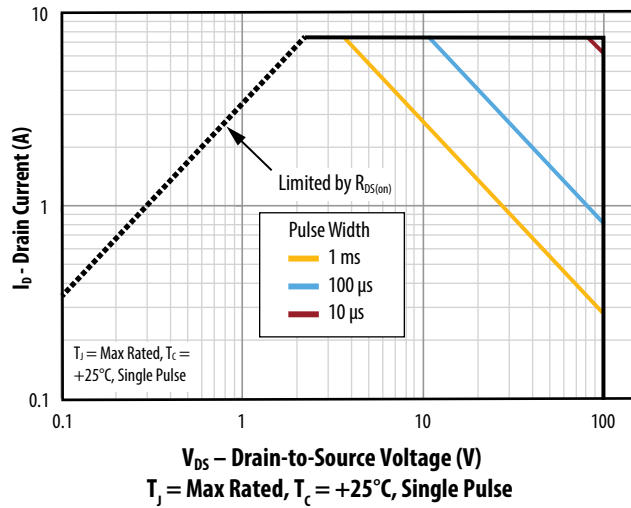
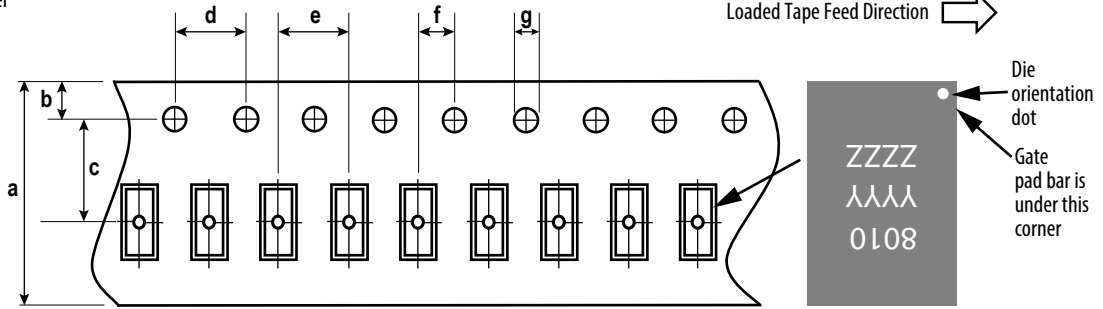
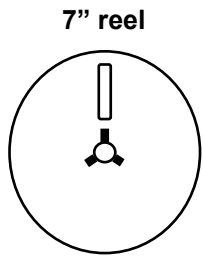


Figure 16: Safe Operating Area



**TAPE AND REEL CONFIGURATION**

4mm pitch, 8mm wide tape on 7" reel

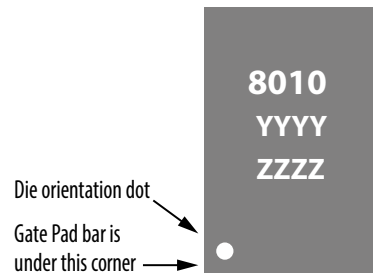


Dimension (mm)	EPC8010 (note 1)		
	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Die is placed into pocket solder bar side down (face side down)

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.  
 Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

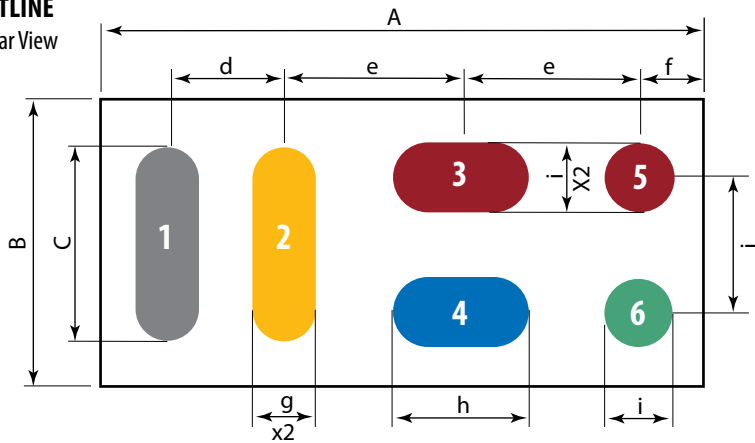
**DIE MARKINGS**



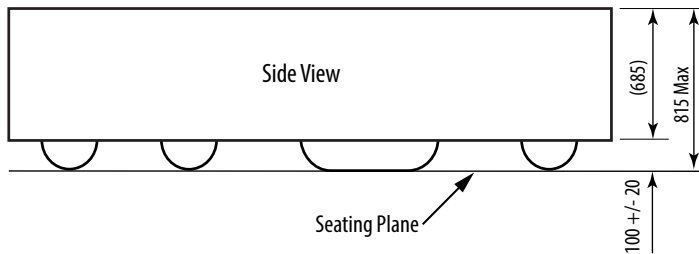
Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC8010	8010	YYYY	ZZZZ

**DIE OUTLINE**

Solder Bar View



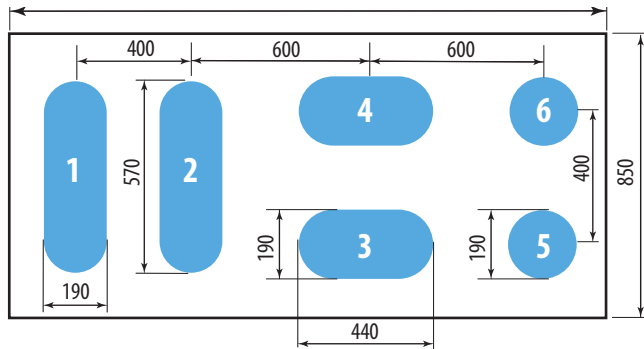
Dim	Micrometers		
	Min	Nominal	Max
A	2020	2050	2080
B	820	850	880
C	555	580	605
d	400	400	400
e	600	600	600
f	200	225	250
g	175	200	225
h	425	450	475
i	175	200	225
j	400	400	400



- Pad no. 1 is Gate
- Pad no. 2 is Source Return for Gate Driver
- Pad no. 3 and 5 are Source
- Pad no. 4 is Drain
- Pad no. 6 is Substrate\*

\*Substrate pin should be connected to Source

**RECOMMENDED LAND PATTERN** (measurements in  $\mu\text{m}$ )

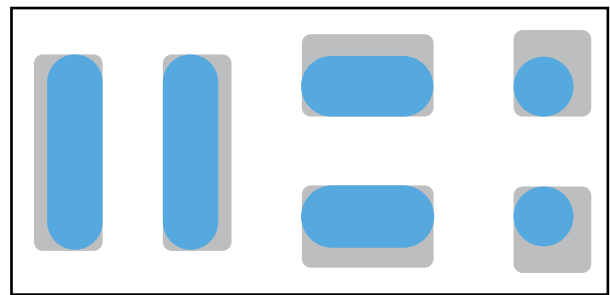
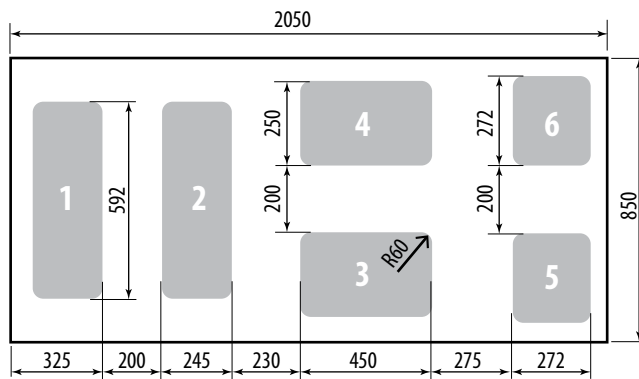


The land pattern is solder mask defined.

- Pad no. 1 is Gate
- Pad no. 2 is Source Return for Gate Driver
- Pad no. 3 and 5 are Source
- Pad no. 4 is Drain
- Pad no. 6 is Substrate\*

\*Substrate pin should be connected to Source

**RECOMMENDED STENCIL DRAWING** (measurements in  $\mu\text{m}$ )



Blue = bump, Gray = stencil

Recommended stencil should be 4 mil (100  $\mu\text{m}$ ) thick, must be laser cut, openings per drawing. Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at: <https://epc-co.com/epc/design-support>

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