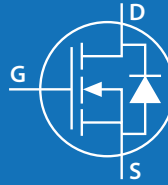


EPC2069 – Enhancement Mode Power Transistor

 V_{DS} , 40 V $R_{DS(on)}$, 2.25 mΩ I_D , 80 A

Revised October 26, 2024

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Questions:
Ask a GaN
Expert



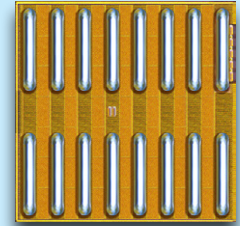
Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	40	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	48	
I_D	Continuous ($T_A = 25^\circ\text{C}$)	80	A
	Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$)	422	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.35	$^\circ\text{C}/\text{W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	1.1	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	46	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V}$, $I_D = 0.7 \text{ mA}$	40			V
I_{DSS}	Drain-Source Leakage	$V_{GS} = 0 \text{ V}$, $V_{DS} = 32 \text{ V}$		0.01	0.7	mA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5 \text{ V}$		0.01	4	
	Gate-to-Source Forward Leakage [#]	$V_{GS} = 5 \text{ V}$, $T_J = 125^\circ\text{C}$		0.05	9	
	Gate-to-Source Reverse Leakage	$V_{GS} = -4 \text{ V}$		0.01	0.8	
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 14 \text{ mA}$	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5 \text{ V}$, $I_D = 30 \text{ A}$		1.6	2.25	mΩ
V_{SD}	Source-Drain Forward Voltage [#]	$I_S = 0.5 \text{ A}$, $V_{GS} = 0 \text{ V}$		1.6		V

[#]Defined by design. Not subject to production test.



Die Size: 3.25 x 3.25 mm

EPC2069 eGaN® FETs are supplied only in passivated die form with solder bars.

Applications

- High frequency DC-DC converters
- BLDC motor drives
- Sync rectification for AC-DC and DC-DC

Benefits

- High power density
- High efficiency
- No reverse recovery
- Ultra low Q_G
- Small footprint
- High frequency capability

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://lead.me/EPC2069>

Dynamic Characteristics[#] ($T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$		1351	2027	pF
C_{RSS}	Reverse Transfer Capacitance			32		
C_{OSS}	Output Capacitance			1044	1566	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{DS} = 0\text{ to }20\text{ V}, V_{GS} = 0\text{ V}$		1465		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			1647		
R_G	Gate Resistance			0.4		Ω
Q_G	Total Gate Charge	$V_{DS} = 20\text{ V}, V_{GS} = 5\text{ V}, I_D = 30\text{ A}$		12.5	16.2	nC
Q_{GS}	Gate-to-Source Charge	$V_{DS} = 20\text{ V}, I_D = 30\text{ A}$		3.9		
Q_{GD}	Gate-to-Drain Charge			2.4		
$Q_{G(TH)}$	Gate Charge at Threshold			2.9		
Q_{OSS}	Output Charge	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$		32	48	
Q_{RR}	Source-Drain Recovery Charge			0		

[#]Defined by design. Not subject to production test.

All measurements were done with substrate connected to source.

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

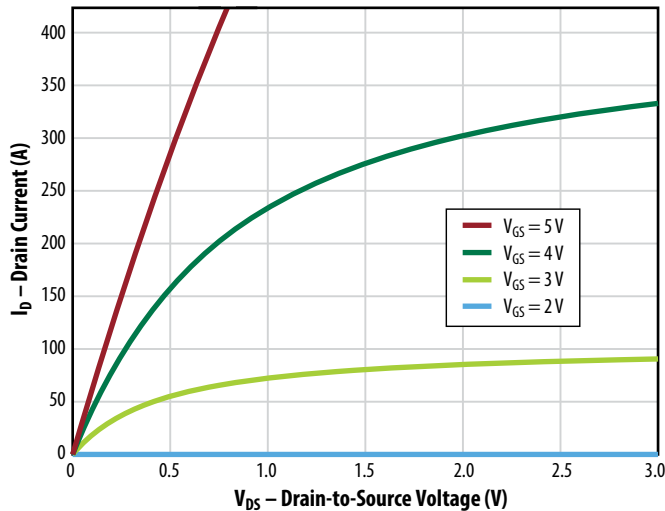
Figure 1: Typical Output Characteristics at 25°C 

Figure 2: Typical Transfer Characteristics

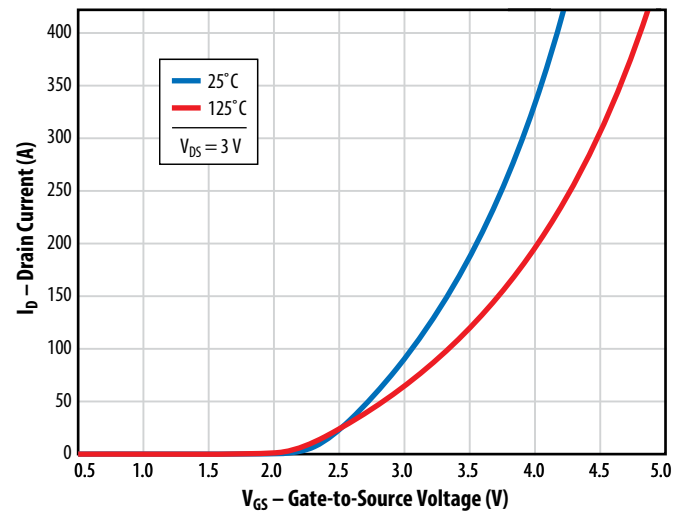
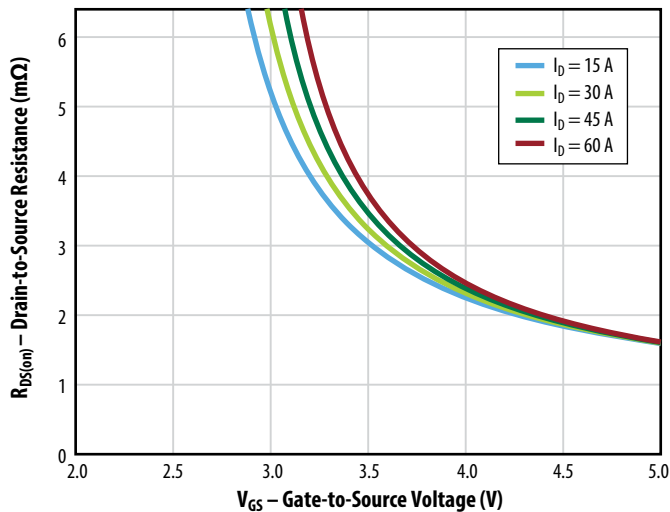
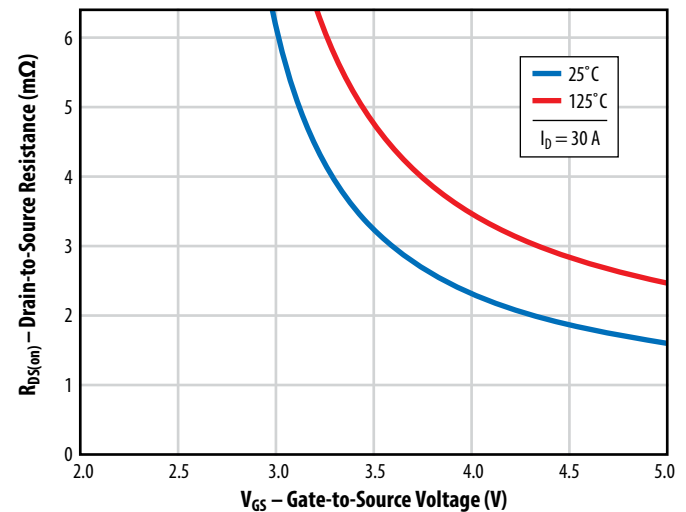
Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain CurrentsFigure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

Figure 5a: Typical Capacitance (Linear Scale)

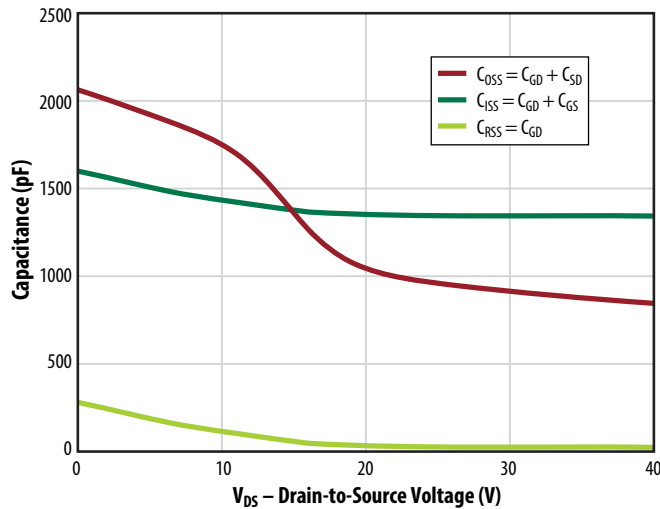


Figure 5b: Typical Capacitance (Log Scale)

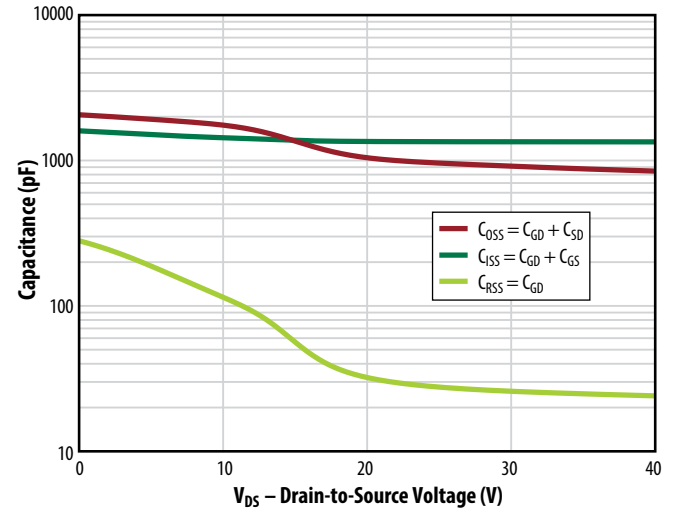
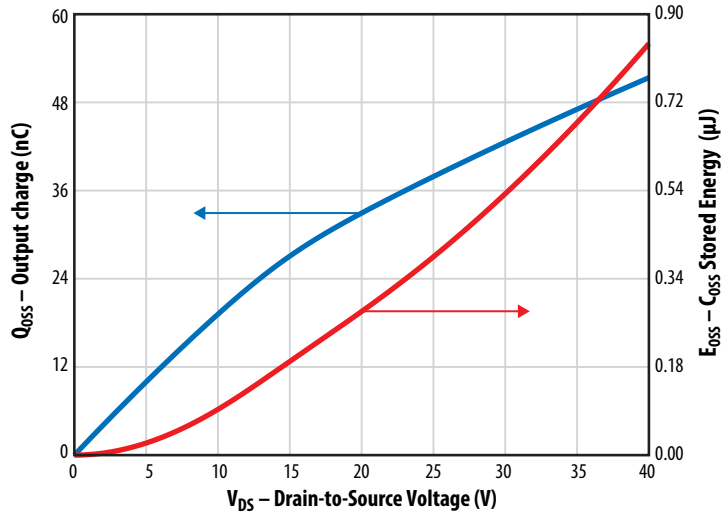
Figure 6: Typical Output Charge and C_{OSS} Stored Energy

Figure 7: Typical Gate Charge

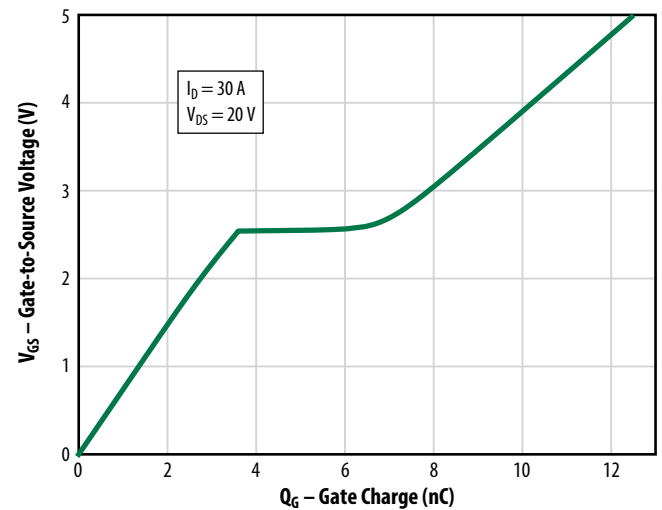


Figure 8: Typical Reverse Drain-Source Characteristics

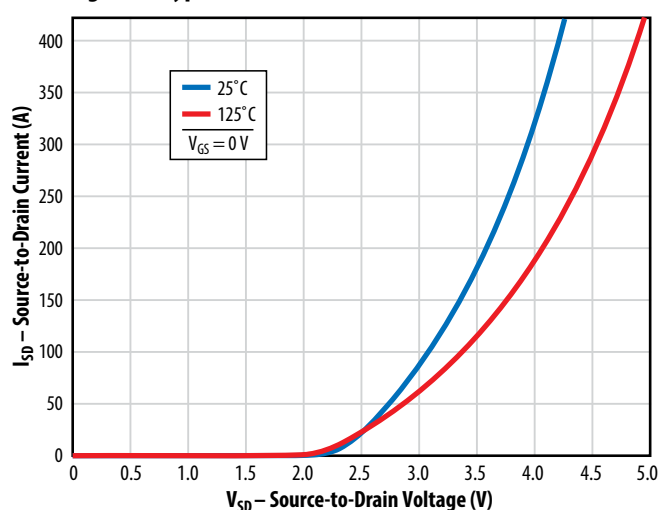
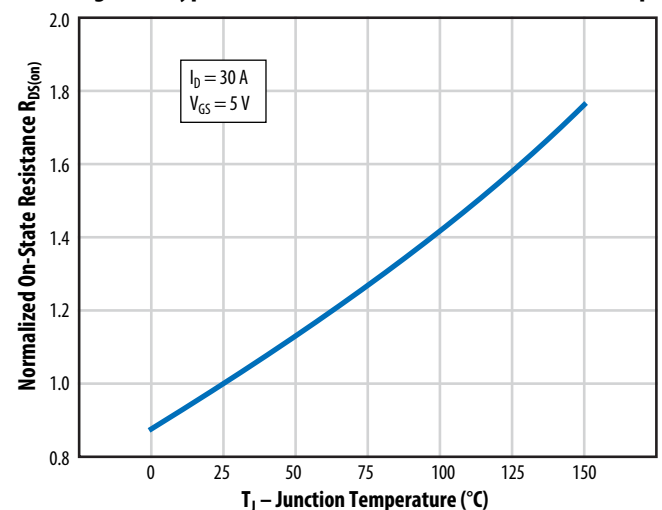


Figure 9: Typical Normalized On-State Resistance vs. Temp.



Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF.

Figure 10: Typical Normalized Threshold Voltage vs. Temperature

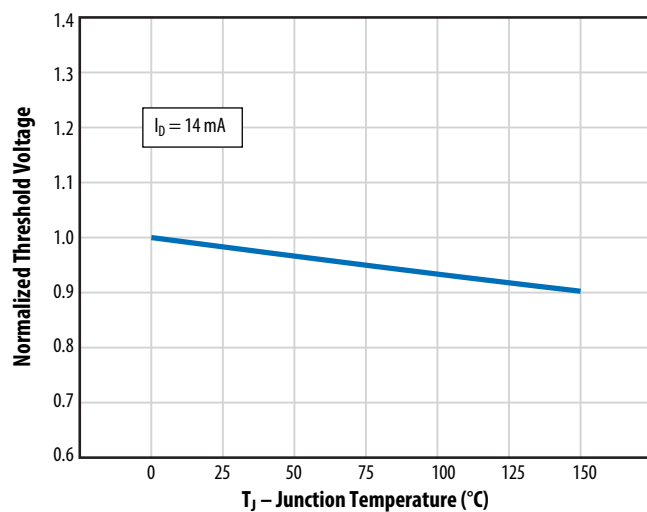


Figure 10: Typical Transient Thermal Response Curves

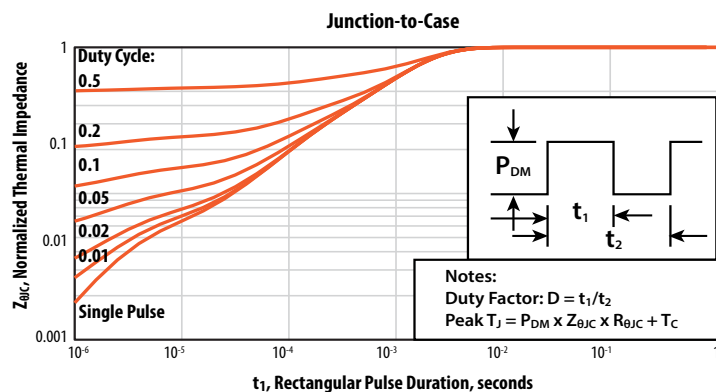
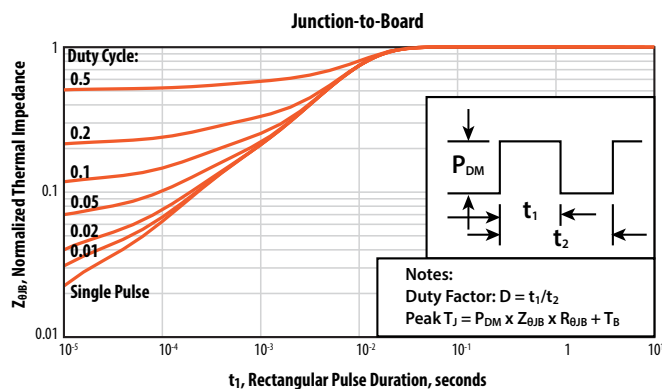
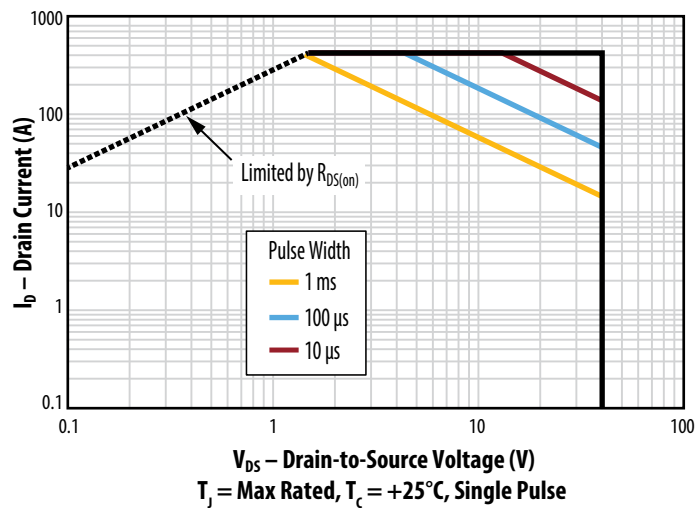
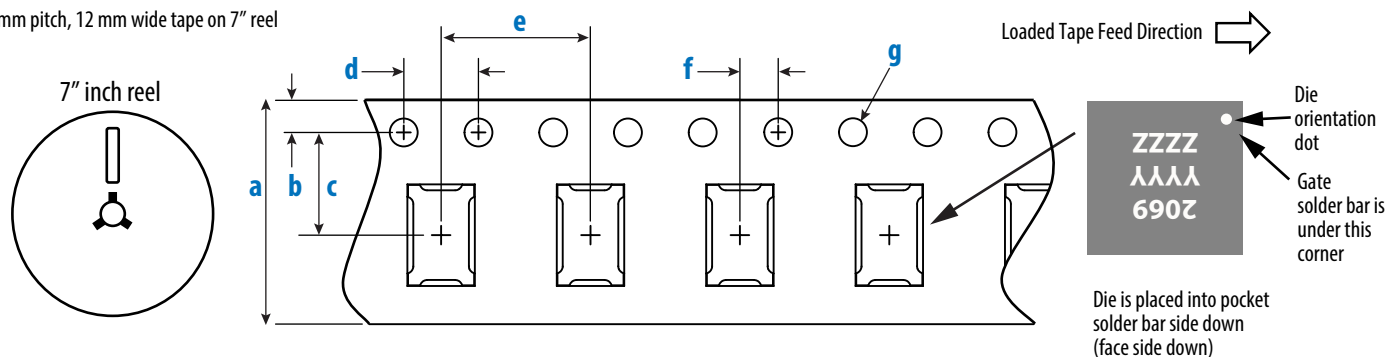


Figure 11: Safe Operating Area



TAPE AND REEL CONFIGURATION

8 mm pitch, 12 mm wide tape on 7" reel

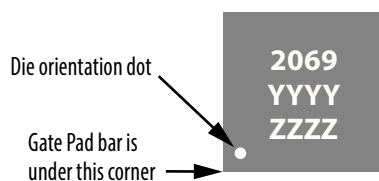


EPC2069 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	8.00	7.90	8.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

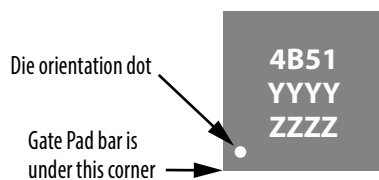
Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

DIE MARKINGS



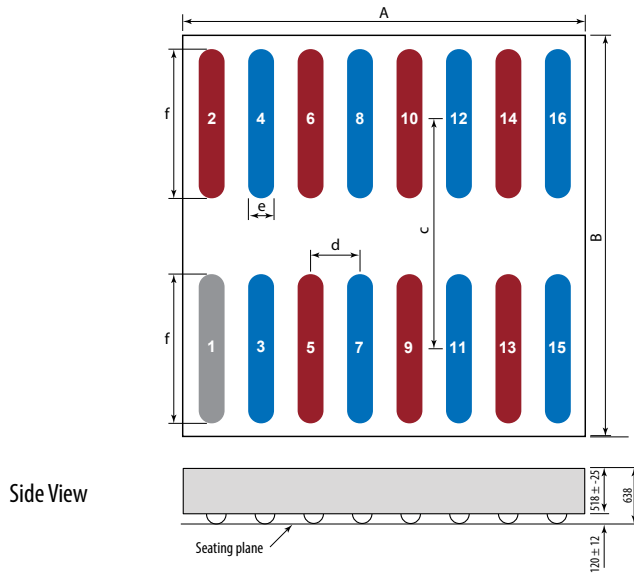
Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2069	2069	YYYY	ZZZZ



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2069	4B51	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View

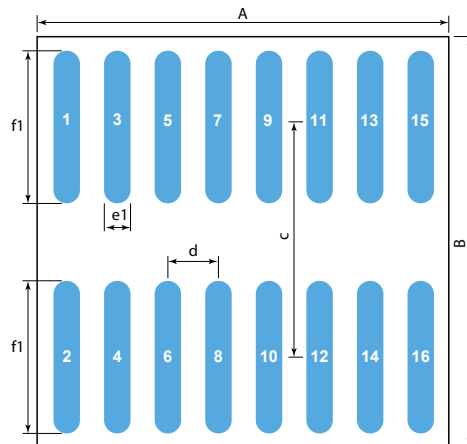


DIM	Micrometers		
	MIN	Nominal	MAX
A	3220	3250	3280
B	3220	3250	3280
c		1805	
d		400	
e	180	200	220
f	1175	1195	1215

Pad 1 is Gate;

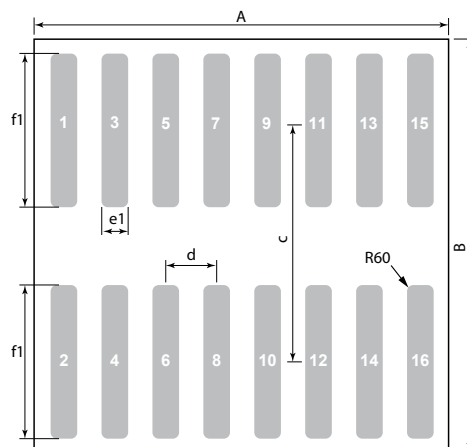
Pads 2,5,6,9,10,13,14 are Source;

Pads 3,4,7,8,11,12,15,16 are Drain

**RECOMMENDED
LAND PATTERN**(units in μm)

Land pattern is solder mask defined

DIM	Micrometers
A	3250
B	3250
c	1805
d	400
e1	180
f1	1175

**RECOMMENDED
STENCIL DRAWING**(units in μm)

DIM	Micrometers
A	3250
B	3250
c	1805
d	400
e1	180
f1	1175

Recommended stencil should be 4 mil (100 μm) thick, must be laser cut, openings per drawing

The corner has a radius of R60

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content

Additional assembly resources available at:

<https://epc-co.com/epc/design-support>

Efficient Power Conversion Corporation (EPC) reserves the right to make changes without further notice to any products herein to improve reliability, function or design. EPC does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights, nor the rights of others.

eGaN® is a registered trademark of Efficient Power Conversion Corporation.

EPC Patent Listing: <https://epc-co.com/epc/about-epc/patents>

Information subject to change without notice.