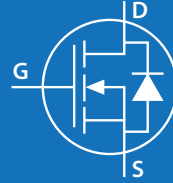


## EPC2057 – Enhancement Mode Power Transistor

 $V_{DS}$ , 50 V $R_{DS(on)}$ , 8.5 mΩ max $I_D$ , 9.6 A

Revised April 8, 2025

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low  $R_{DS(on)}$ , while its lateral device structure and majority carrier diode provide exceptionally low  $Q_G$  and zero  $Q_{RR}$ . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

**Application Notes:**

- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

**Questions:**  
Ask a GaN  
Expert



| Maximum Ratings |                                                               |            |                  |
|-----------------|---------------------------------------------------------------|------------|------------------|
| PARAMETER       |                                                               | VALUE      | UNIT             |
| $V_{DS}$        | Drain-to-Source Voltage (Continuous)                          | 50         | V                |
|                 | Drain-to-Source Voltage (Repetitive Transient) <sup>(1)</sup> | 60         |                  |
| $I_D$           | Continuous ( $T_A = 25^\circ\text{C}$ )                       | 9.6        | A                |
|                 | Pulsed ( $25^\circ\text{C}$ , $T_{PULSE} = 300 \mu\text{s}$ ) | 66         |                  |
| $V_{GS}$        | Gate-to-Source Voltage                                        | 6          | V                |
|                 | Gate-to-Source Voltage                                        | -4         |                  |
| $T_J$           | Operating Temperature                                         | -40 to 150 | $^\circ\text{C}$ |
| $T_{STG}$       | Storage Temperature                                           | -40 to 150 |                  |

<sup>(1)</sup> Pulsed repetitively, duty cycle factor ( $DC_{Factor}$ )  $\leq 1\%$ ; See Figure 13.

| Thermal Characteristics |                                                                              |      |                           |
|-------------------------|------------------------------------------------------------------------------|------|---------------------------|
| PARAMETER               |                                                                              | TYP  | UNIT                      |
| $R_{\theta JC}$         | Thermal Resistance, Junction-to-Case                                         | 2.3  | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JB}$         | Thermal Resistance, Junction-to-Board                                        | 7    |                           |
| $R_{\theta JA}$         | Thermal Resistance, Junction-to-Ambient <sup>(2)</sup>                       | 72.5 |                           |
| $R_{\theta JA\_JEDEC}$  | Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB)               | 82   |                           |
| $R_{\theta JA\_EVB}$    | Thermal Resistance, Junction-to-Ambient (using EPC90155 EVB <sup>(3)</sup> ) | 68.5 |                           |

<sup>(2)</sup>  $R_{\theta JA}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

See [https://epc-co.com/epc/documents/product-training/Appnote\\_Thermal\\_Performance\\_of\\_eGaN\\_FETs.pdf](https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf) for details.

<sup>(3)</sup> Determined with devices mounted on EVB in half-bridge configuration

| Static Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise stated) |                                             |                                                    |     |       |       |      |
|----------------------------------------------------------------------------|---------------------------------------------|----------------------------------------------------|-----|-------|-------|------|
| PARAMETER                                                                  |                                             | TEST CONDITIONS                                    | MIN | TYP   | MAX   | UNIT |
| $BV_{DSS}$                                                                 | Drain-to-Source Voltage                     | $V_{GS} = 0 \text{ V}$ , $I_D = 0.031 \text{ mA}$  | 50  |       |       | V    |
| $I_{DSS}$                                                                  | Drain-Source Leakage                        | $V_{GS} = 0 \text{ V}$ , $V_{DS} = 40 \text{ V}$   |     | 0.004 | 0.031 | mA   |
| $I_{GSS}$                                                                  | Gate-to-Source Forward Leakage              | $V_{GS} = 5 \text{ V}$                             |     | 0.004 | 0.8   |      |
|                                                                            | Gate-to-Source Forward Leakage <sup>#</sup> | $V_{GS} = 5 \text{ V}$ , $T_J = 125^\circ\text{C}$ |     | 0.04  | 1.7   |      |
|                                                                            | Gate-to-Source Reverse Leakage              | $V_{GS} = -4 \text{ V}$                            |     | 0.004 | 0.026 |      |
| $V_{GS(TH)}$                                                               | Gate Threshold Voltage                      | $V_{DS} = V_{GS}$ , $I_D = 2 \text{ mA}$           | 0.7 | 1.1   | 2.5   | V    |
| $R_{DS(on)}$                                                               | Drain-Source On Resistance                  | $V_{GS} = 5 \text{ V}$ , $I_D = 6 \text{ A}$       |     | 6     | 8.5   | mΩ   |
| $V_{SD}$                                                                   | Source-Drain Forward Voltage <sup>#</sup>   | $V_{GS} = 0 \text{ V}$ , $I_S = 0.5 \text{ A}$     |     | 1.4   |       | V    |

<sup>#</sup> Defined by design. Not subject to production test.



Die Size: 1.5 x 1.2 mm

**EPC2057** eGaN® FETs are supplied only in passivated die form with solder bars.

**Applications**

- DC-DC converters
- Isolated DC-DC converters
- USB-C battery chargers
- LED lighting
- 12 V–24 V input motor drives

**Benefits**

- Ultra high efficiency
- No reverse recovery
- Ultra low  $Q_G$
- Small footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC2057>

Dynamic Characteristics<sup>#</sup> ( $T_J = 25^\circ\text{C}$  unless otherwise stated)

| PARAMETER     |                                                       | TEST CONDITIONS                                               | MIN | TYP | MAX | UNIT     |
|---------------|-------------------------------------------------------|---------------------------------------------------------------|-----|-----|-----|----------|
| $C_{ISS}$     | Input Capacitance                                     | $V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$                   |     | 383 | 444 | pF       |
| $C_{RSS}$     | Reverse Transfer Capacitance                          |                                                               |     | 3   |     |          |
| $C_{OSS}$     | Output Capacitance                                    |                                                               |     | 172 | 218 |          |
| $C_{OSS(ER)}$ | Effective Output Capacitance, Energy Related (Note 1) | $V_{DS} = 0\text{ to }25\text{ V}, V_{GS} = 0\text{ V}$       |     | 220 |     |          |
| $C_{OSS(TR)}$ | Effective Output Capacitance, Time Related (Note 2)   |                                                               |     | 265 |     |          |
| $R_G$         | Gate Resistance                                       |                                                               |     | 0.8 |     | $\Omega$ |
| $Q_G$         | Total Gate Charge                                     | $V_{DS} = 25\text{ V}, V_{GS} = 5\text{ V}, I_D = 6\text{ A}$ |     | 3.0 | 3.5 | nC       |
| $Q_{GS}$      | Gate-to-Source Charge                                 | $V_{DS} = 25\text{ V}, I_D = 6\text{ A}$                      |     | 1.2 |     |          |
| $Q_{GD}$      | Gate-to-Drain Charge                                  |                                                               |     | 0.5 |     |          |
| $Q_{G(TH)}$   | Gate Charge at Threshold                              |                                                               |     | 0.8 |     |          |
| $Q_{OSS}$     | Output Charge                                         | $V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$                   |     | 7.9 | 10  |          |
| $Q_{RR}$      | Source-Drain Recovery Charge                          |                                                               |     | 0   |     |          |

<sup>#</sup> Defined by design. Not subject to production test.

All measurements were done with substrate connected to source.

Note 1:  $C_{OSS(ER)}$  is a fixed capacitance that gives the same stored energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50%  $BV_{DSS}$ .

Note 2:  $C_{OSS(TR)}$  is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50%  $BV_{DSS}$ .

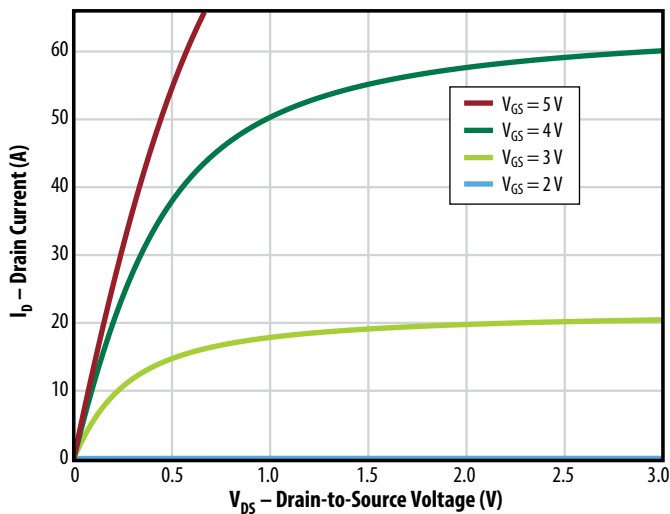
Figure 1: Typical Output Characteristics at  $25^\circ\text{C}$ 

Figure 2: Typical Transfer Characteristics

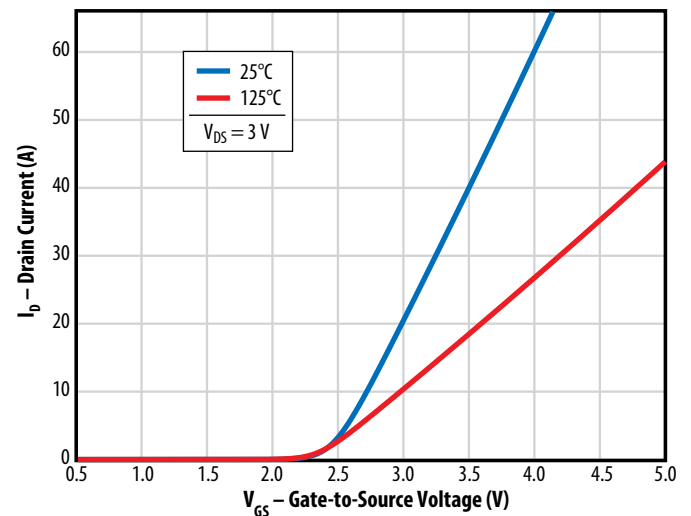
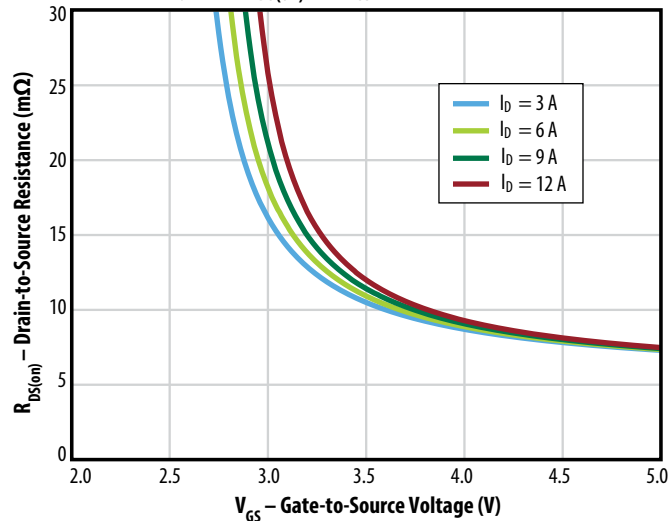
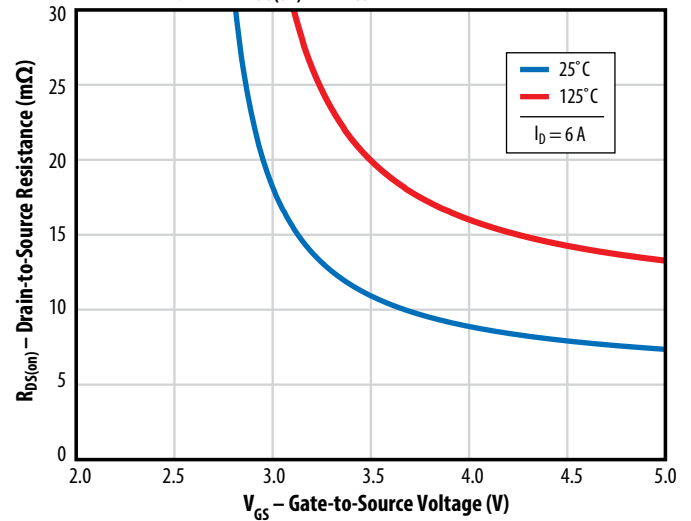
Figure 3: Typical  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Drain CurrentsFigure 4: Typical  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Temperatures

Figure 5a: Typical Capacitance (Linear Scale)

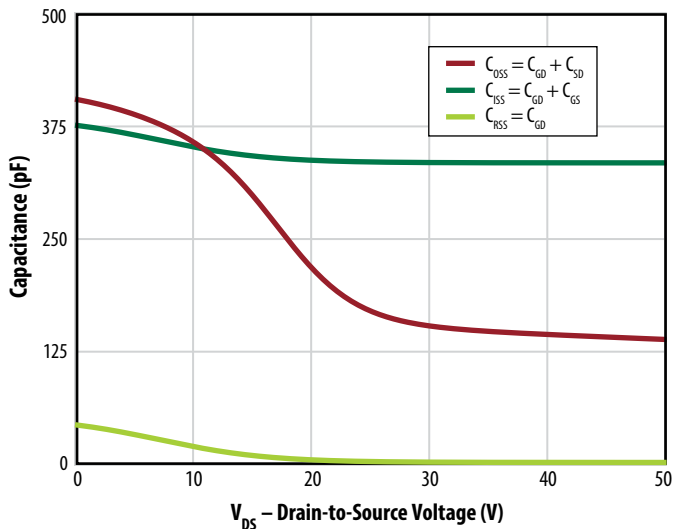


Figure 5b: Typical Capacitance (Log Scale)

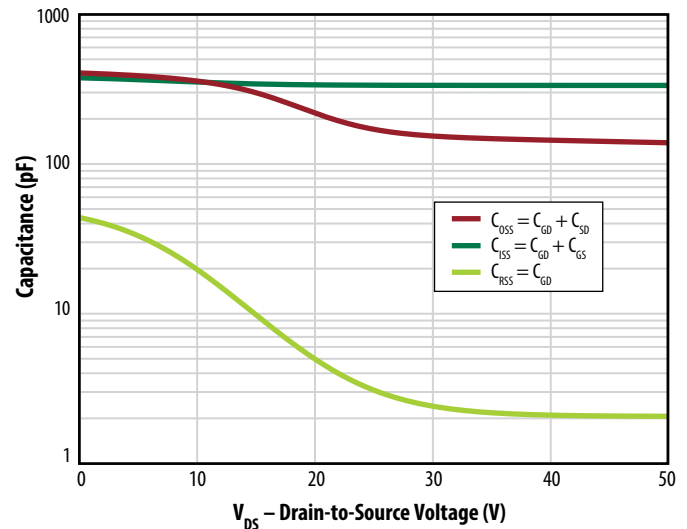
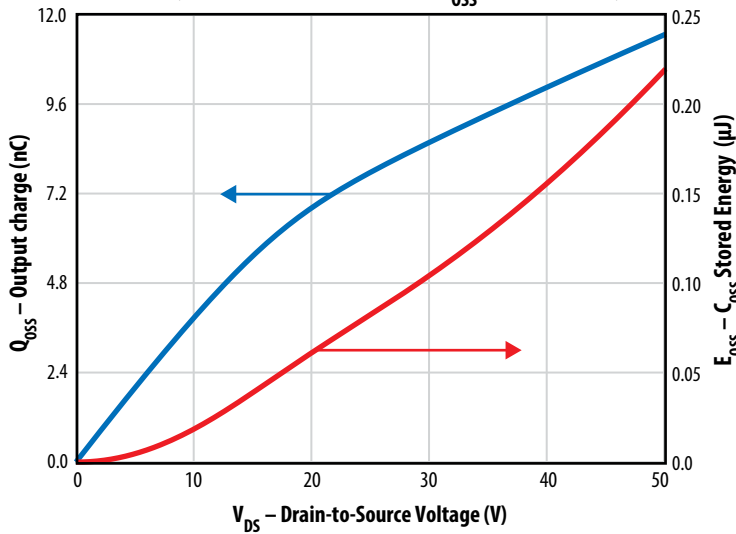
Figure 6: Typical Output Charge and  $C_{OSS}$  Stored Energy

Figure 7: Typical Gate Charge

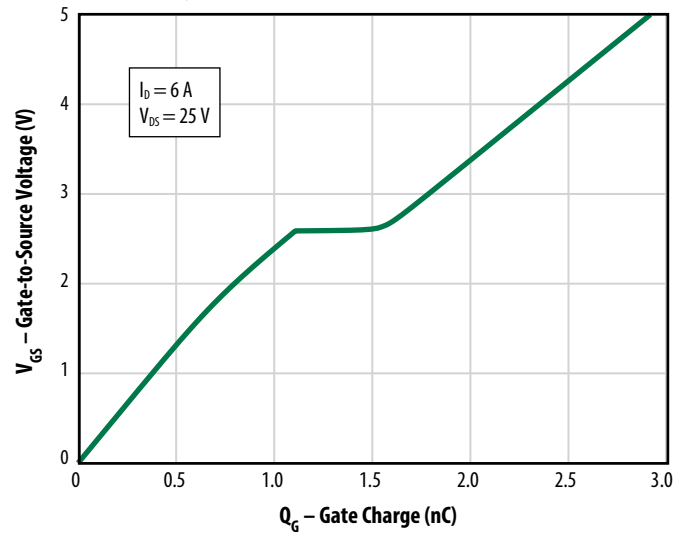
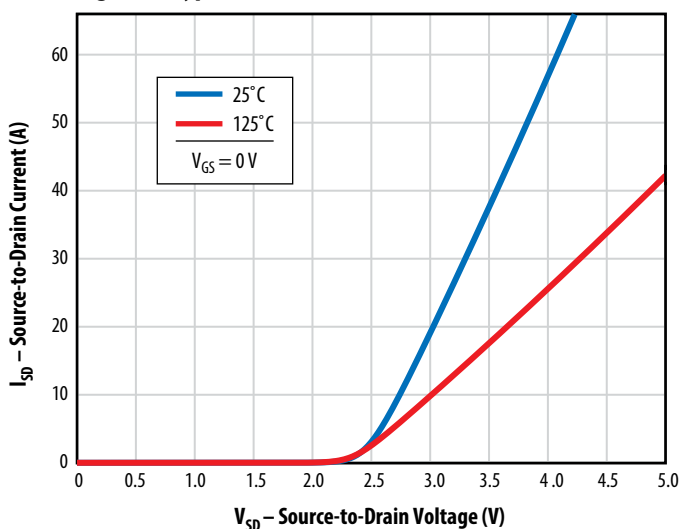


Figure 8: Typical Reverse Drain-Source Characteristics



**Note:** Negative gate drive voltage increases the reverse drain-source voltage.  
EPC recommends 0 V for OFF.

Figure 9: Typical Normalized On-State Resistance vs. Temp.

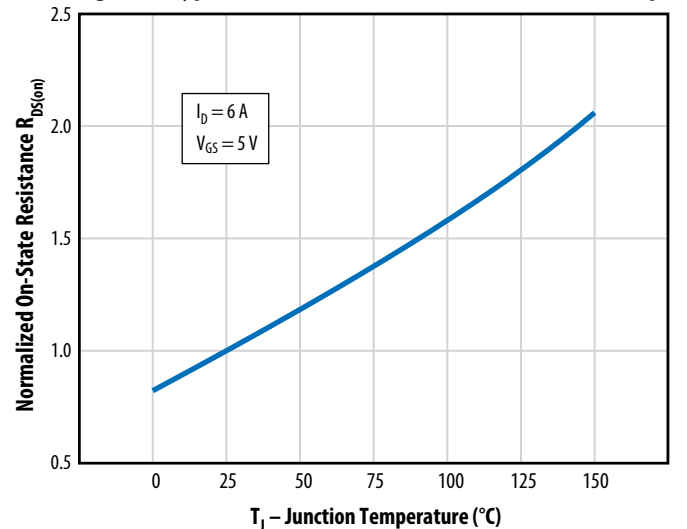


Figure 10: Typical Normalized Threshold Voltage vs. Temp.

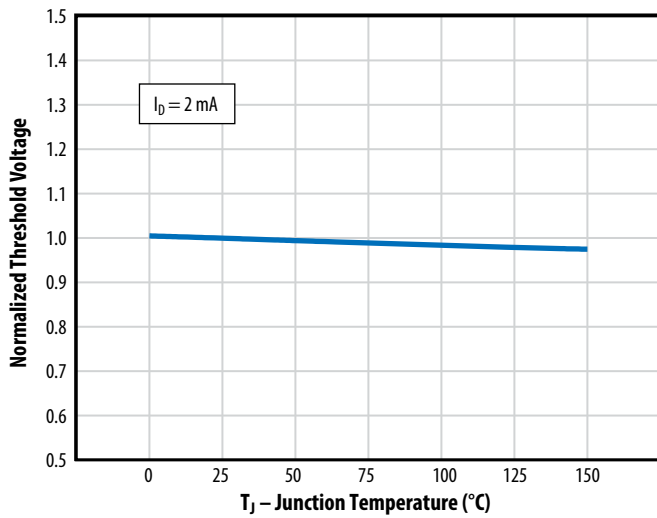


Figure 11: Safe Operating Area

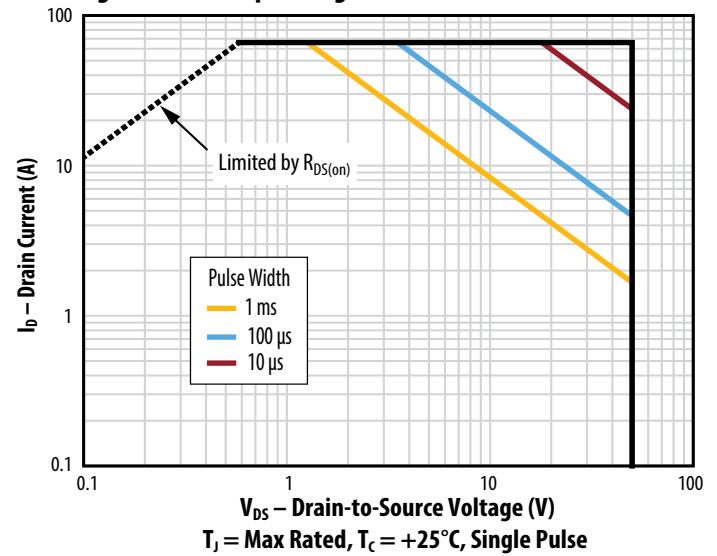
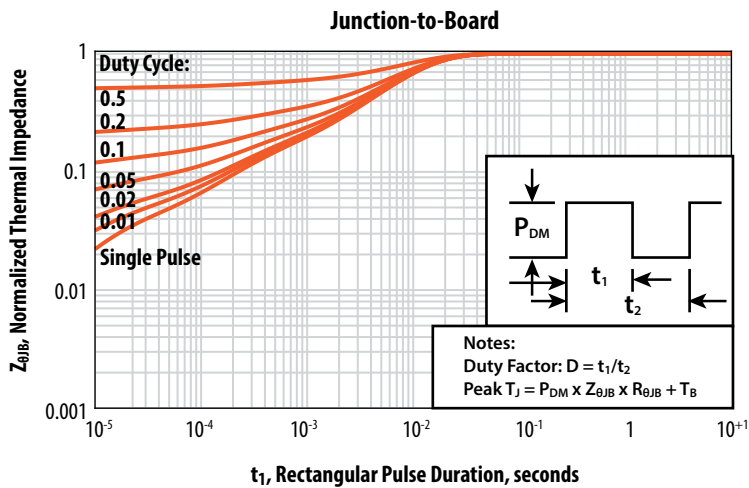
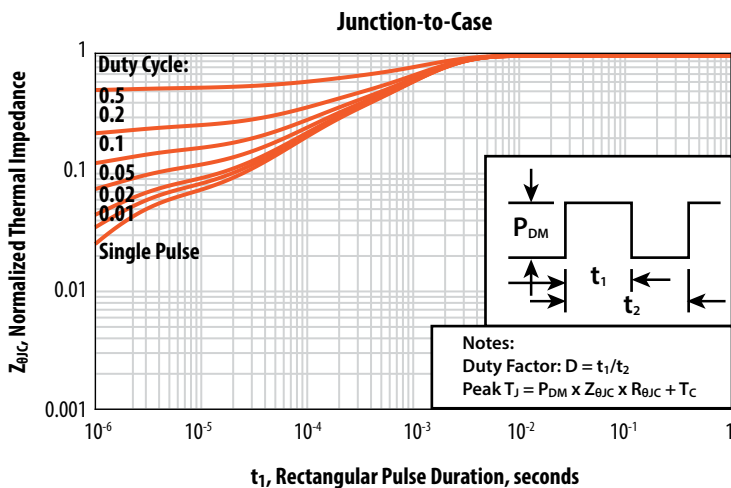
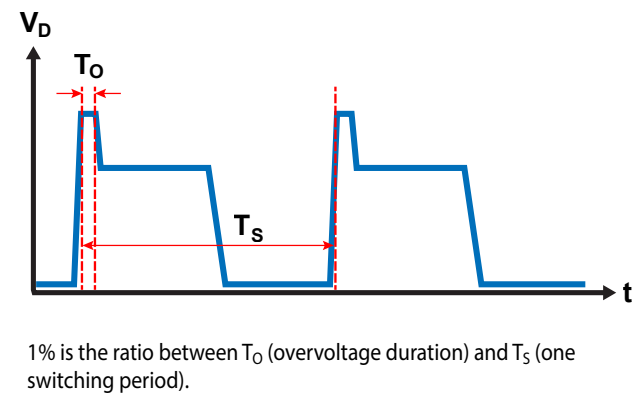


Figure 12: Typical Transient Thermal Response Curves

Figure 13: Duty Cycle Factor ( $DC_{\text{Factor}}$ ) Illustration for Repetitive Overvoltage Specification

## LAYOUT CONSIDERATIONS

GaN transistors generally behave like power MOSFETs, but at much higher switching speeds and power densities, therefore layout considerations are very important, and care must be taken to minimize layout parasitic inductances. The recommended design utilizes the first inner layer as a power loop return path. This return path is located directly beneath the top layer's power loop allowing for the smallest physical loop size. This method is also commonly referred to as flux cancellation. Variations of this concept can be implemented by placing the bus capacitors either next to the high side device, next to the low side device, or between the low and high side devices, but in all cases the loop is closed using the first inner layer right beneath the devices.

A similar concept is also used for the gate loop, with the first inner layer used as a reference for the gate loop under the gate resistors and the relative pins of the gate driver: ground for the bottom FET and switch node for the top FET.

Furthermore, to minimize the common source inductance between power and gate loops, the power and gate loops are laid out perpendicular to each other, and a via next to the source pad closest to the gate pad is used as Kelvin connection for the gate driver return path.

The [EPC90155 40 V Half-bridge with Gate Drive using EPC2057](#) implements our recommended vertical inner layout.

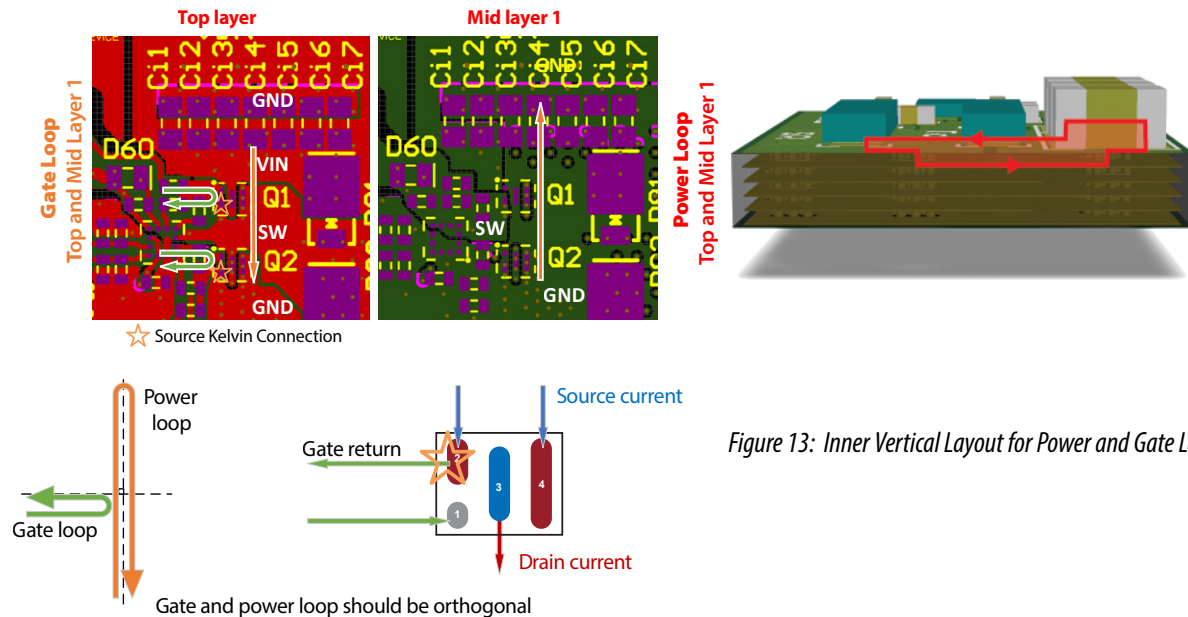


Figure 13: Inner Vertical Layout for Power and Gate Loops

Detailed recommendations on layout can be found on EPC's website: [Optimizing PCB Layout with eGaN FETs.pdf](#)

## TYPICAL SWITCHING BEHAVIOR

The following typical switching waveforms are captured in these conditions:

- [EPC90155 40 V Half-bridge with Gate Drive using EPC2057](#)
- Gate driver: uP1966E with 0.4  $\Omega$ /0.7  $\Omega$  pull-down/pull-up resistance
- External  $R_G(\text{ON}) = 4.7 \Omega$ ,  $R_G(\text{OFF}) = 1 \Omega$
- $V_{IN} = 40 \text{ V}$ ,  $I_L = 7 \text{ A}$

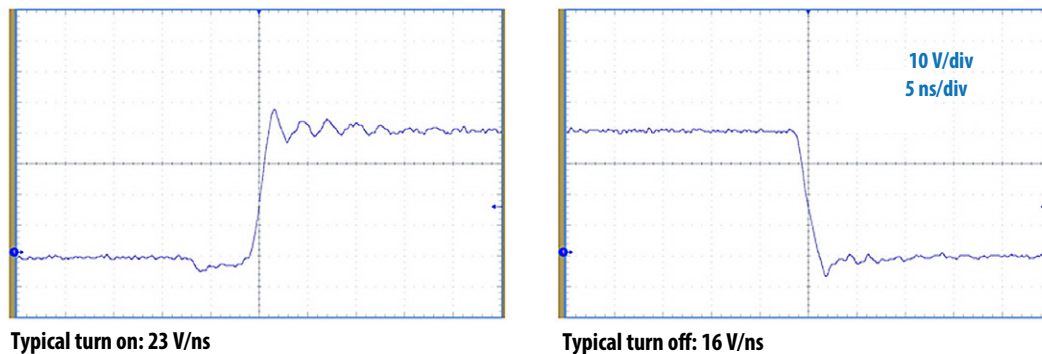


Figure 14: Typical half-bridge voltage switching waveforms

See the [EPC90155 40 V Half-bridge with Gate Drive using EPC2057 Quick Start Guide](#) for more information.

## TYPICAL THERMAL CONCEPT

The EPC2057 can take advantage of dual sided cooling to maximize its heat dissipation capabilities in high power density designs.

**Note that the top of EPC FETs are connected to source potential, so for half-bridge topologies the Thermal Interface Material (TIM) needs to provide electrical isolation to the heatsink.**

Recommended best practice thermal solutions are covered in detail in [How2AppNote012 - How to Get More Power Out of an eGaN Converter.pdf](#).

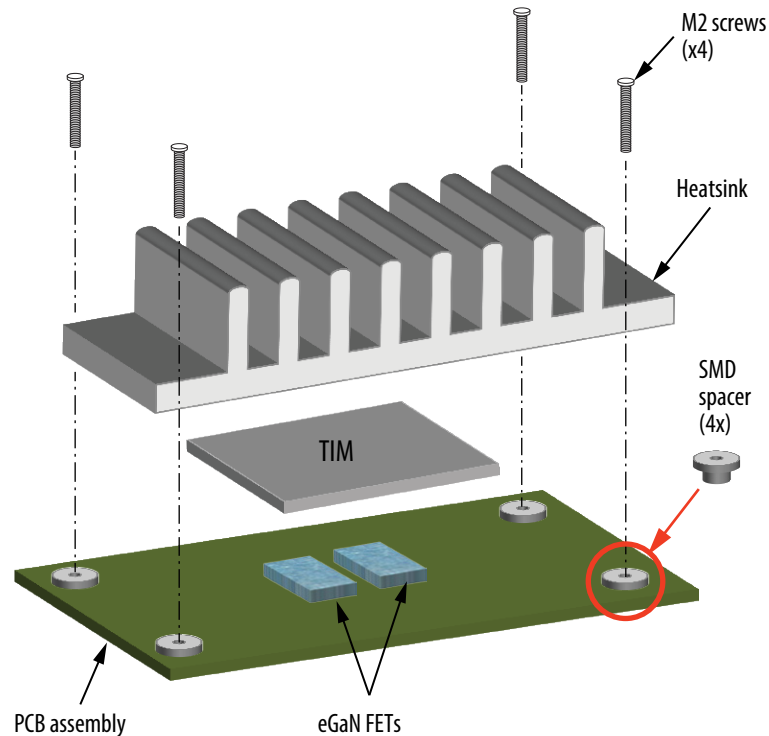


Figure 15: Exploded view of heatsink assembly using screws

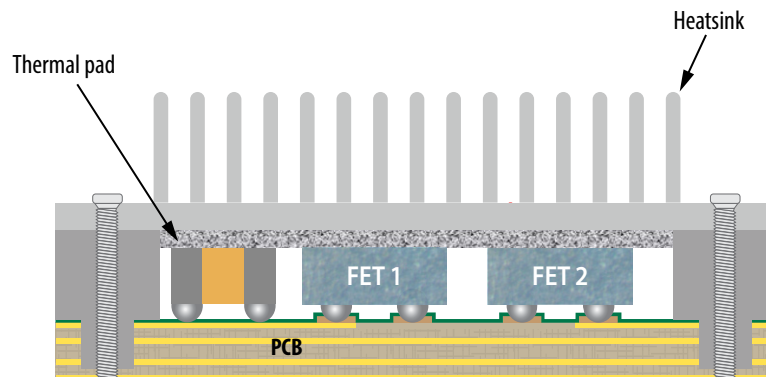


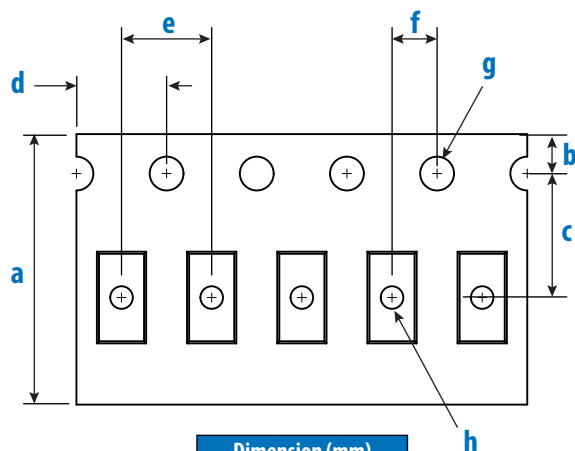
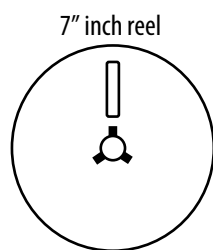
Figure 16: A cross-section image of dual sided thermal solution

**Note: Connecting the heatsink to ground is recommended and can significantly improve radiated EMI**

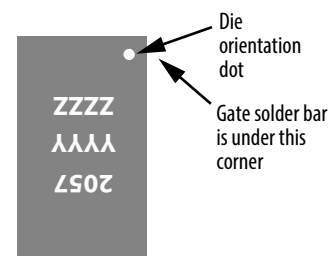
The thermal design can be optimized by using the [GaN FET Thermal Calculator](#) on EPC's website.

## TAPE AND REEL CONFIGURATION

4 mm pitch, 8 mm wide tape on 7" reel



Loaded Tape Feed Direction →



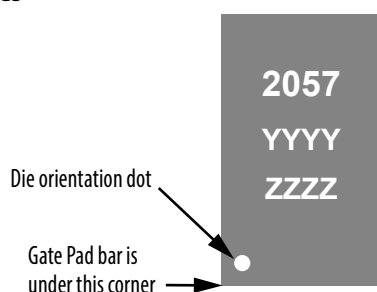
Die is placed into pocket solder bar side down (face side down)

| EPC2057 (Note 1)  | Dimension (mm) |      |      |
|-------------------|----------------|------|------|
|                   | Target         | MIN  | MAX  |
| <b>a</b>          | 8.00           | 7.90 | 8.30 |
| <b>b</b>          | 1.75           | 1.65 | 1.85 |
| <b>c</b> (Note 2) | 3.50           | 3.45 | 3.55 |
| <b>d</b>          | 4.00           | 3.90 | 4.10 |
| <b>e</b>          | 4.00           | 3.90 | 4.10 |
| <b>f</b> (Note 2) | 2.00           | 1.95 | 2.05 |
| <b>g</b>          | 1.50           | 1.50 | 1.60 |
| <b>h</b>          | 0.50           | 0.45 | 0.55 |

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

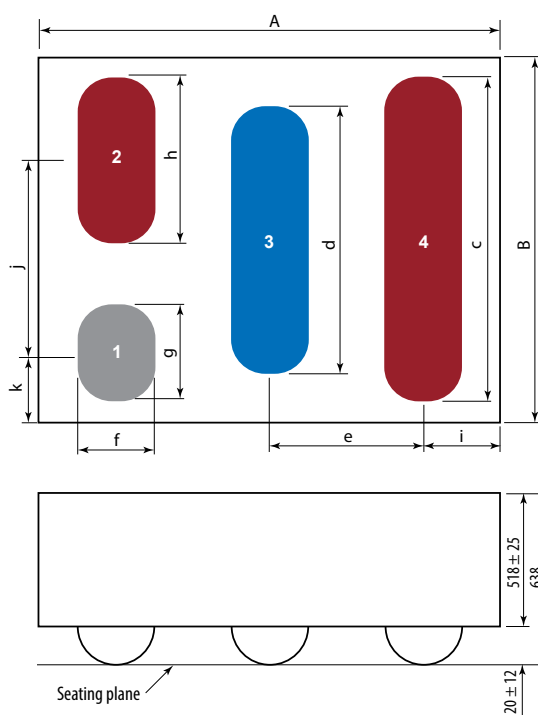
## DIE MARKINGS



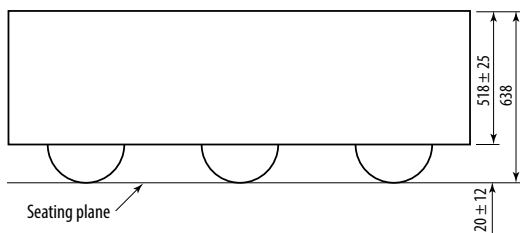
| Part Number | Laser Markings        |                               |                               |
|-------------|-----------------------|-------------------------------|-------------------------------|
|             | Part # Marking Line 1 | Lot _Date Code Marking Line 2 | Lot _Date Code Marking Line 3 |
| EPC2057     | 2057                  | YYYY                          | ZZZZ                          |

## DIE OUTLINE

Solder Bump View



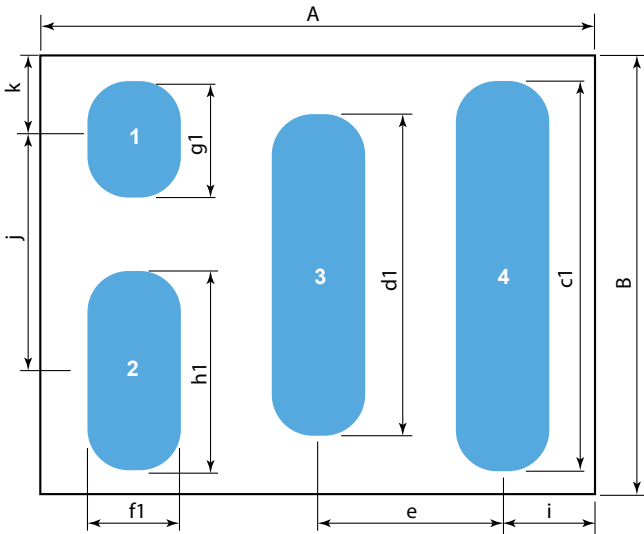
Side View



| DIM      | Micrometers |         |      |
|----------|-------------|---------|------|
|          | MIN         | Nominal | MAX  |
| <b>A</b> | 1470        | 1500    | 1530 |
| <b>B</b> | 1170        | 1200    | 1230 |
| <b>c</b> |             | 1050    |      |
| <b>d</b> |             | 875     |      |
| <b>e</b> |             | 500     |      |
| <b>f</b> |             | 250     |      |
| <b>g</b> |             | 300     |      |
| <b>h</b> |             | 525     |      |
| <b>i</b> |             | 250     |      |
| <b>j</b> |             | 637.5   |      |
| <b>k</b> |             | 225     |      |

Pad 1 is Gate;  
 Pads 2 and 4 are Source;  
 Pad 3 is Drain

RECOMMENDED  
LAND PATTERN  
(units in μm)

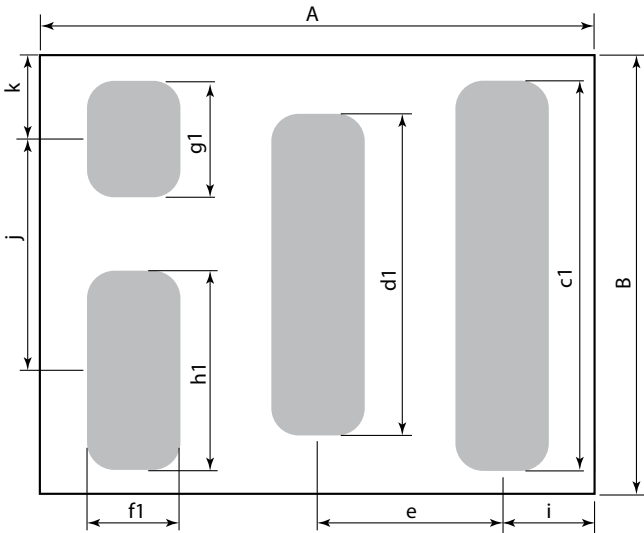


Land pattern is solder mask defined.

| DIM | Micrometers |
|-----|-------------|
| A   | 1500        |
| B   | 1200        |
| c1  | 1030        |
| d1  | 855         |
| e   | 500         |
| f1  | 230         |
| g1  | 280         |
| h1  | 505         |
| i   | 250         |
| j   | 637.5       |
| k   | 225         |

Pad 1 is Gate;  
Pads 2 and 4 are Source;  
Pad 3 is Drain

RECOMMENDED  
STENCIL DRAWING  
(units in μm)



| DIM | Micrometers |
|-----|-------------|
| A   | 1500        |
| B   | 1200        |
| c1  | 1030        |
| d1  | 855         |
| e   | 500         |
| f1  | 230         |
| g1  | 280         |
| h1  | 505         |
| i   | 250         |
| j   | 637.5       |
| k   | 225         |

Recommended stencil should be 4 mil (100 μm) thick, must be laser cut, openings per drawing.

The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Split stencil design can be provided upon request, but EPC has tested this stencil design and not found any scooping issues.

Additional assembly resources available at <https://epc-co.com/epc/design-support/assemblybasics>

## ADDITIONAL RESOURCES AVAILABLE

Solder mask defined pads are recommended for best reliability.

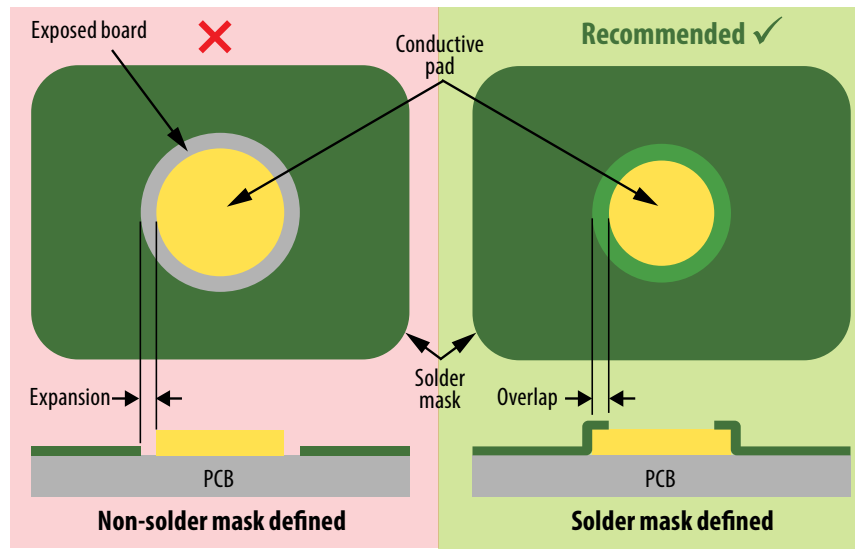


Figure 17: Solder mask defined versus non-solder mask defined pad

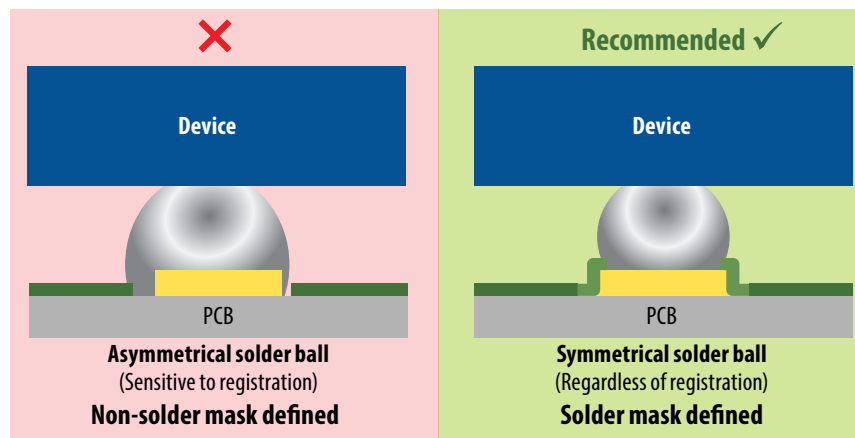


Figure 18: Effect of solder mask design on the solder ball symmetry

- Assembly resources – [https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote\\_GaNassembly.pdf](https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf)
- Library of Altium footprints for production FETs and ICs – <https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip> (for preliminary device Altium footprints, contact EPC)

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EPC Patent Listing: <https://epc-co.com/epc/about-epc/patents>

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