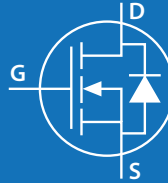


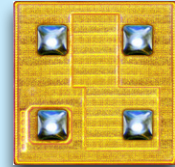
EPC2054 – Enhancement Mode Power Transistor

 V_{DS} , 200 V $R_{DS(on)}$, 43 mΩ I_D , 3 A

Revised June 11, 2021

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Questions:
Ask a GaN
Expert



Die Size: 1.3 x 1.3 mm

EPC2054 eGaN® FETs are supplied only in passivated die form with solder bumps

Maximum Ratings

PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	200	V
I_D	Continuous ($T_A = 25^\circ\text{C}$)	3	A
	Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$)	32	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics

PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.9	$^\circ\text{C}/\text{W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	14	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	83	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V}$, $I_D = 0.12 \text{ mA}$	200			V
I_{DSS}	Drain-Source Leakage	$V_{GS} = 0 \text{ V}$, $V_{DS} = 160 \text{ V}$		0.001	0.1	mA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5 \text{ V}$		0.003	0.5	
	Gate-to-Source Forward Leakage [#]	$V_{GS} = 5 \text{ V}$, $T_J = 125^\circ\text{C}$		0.1	1	
	Gate-to-Source Reverse Leakage	$V_{GS} = -4 \text{ V}$		0.001	0.1	
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 1 \text{ mA}$	0.8	1.2	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5 \text{ V}$, $I_D = 1 \text{ A}$		32	43	mΩ
V_{SD}	Source-Drain Forward Voltage [#]	$I_S = 0.5 \text{ A}$, $V_{GS} = 0 \text{ V}$		1.5		V

[#] Defined by design. Not subject to production test.

Applications

- High Speed DC-DC conversion
- Wireless power transfer
- High frequency hard-switching and soft-switching circuits
- Lidar/time of flight (ToF)
- Automation
- Solar
- Class-D audio

Benefits

- Ultra high efficiency
- Ultra low $R_{DS(on)}$
- Ultra low Q_G
- Ultra small footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC2054>

Dynamic Characteristics[#] ($T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$		358	573	pF
C_{RSS}	Reverse Transfer Capacitance			0.3		
C_{OSS}	Output Capacitance			89	134	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{DS} = 0\text{ to }100\text{ V}, V_{GS} = 0\text{ V}$		120		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			152		
R_G	Gate Resistance			0.8		Ω
Q_G	Total Gate Charge	$V_{DS} = 100\text{ V}, V_{GS} = 5\text{ V}, I_D = 1\text{ A}$		2.9	4.3	nC
Q_{GS}	Gate-to-Source Charge	$V_{DS} = 100\text{ V}, I_D = 1\text{ A}$		0.9		
Q_{GD}	Gate-to-Drain Charge			0.3		
$Q_{G(TH)}$	Gate Charge at Threshold			0.7		
Q_{OSS}	Output Charge	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$		15	23	
Q_{RR}	Source-Drain Recovery Charge			0		

[#] Defined by design. Not subject to production test.

All measurements were done with substrate connected to source.

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

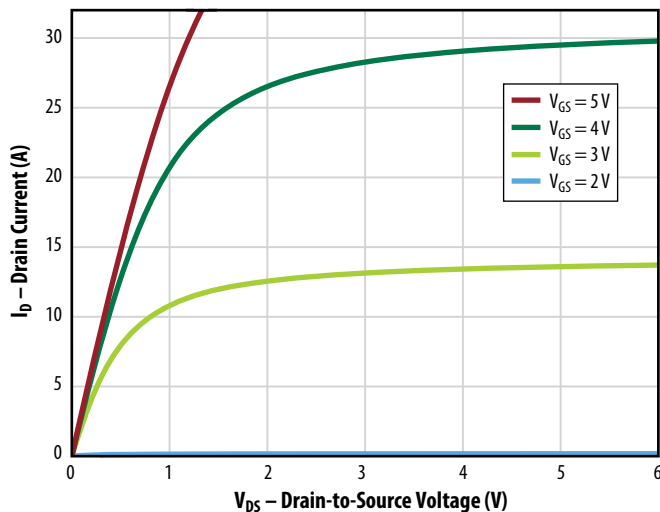
Figure 1: Typical Output Characteristics 25°C 

Figure 2: Typical Transfer Characteristics

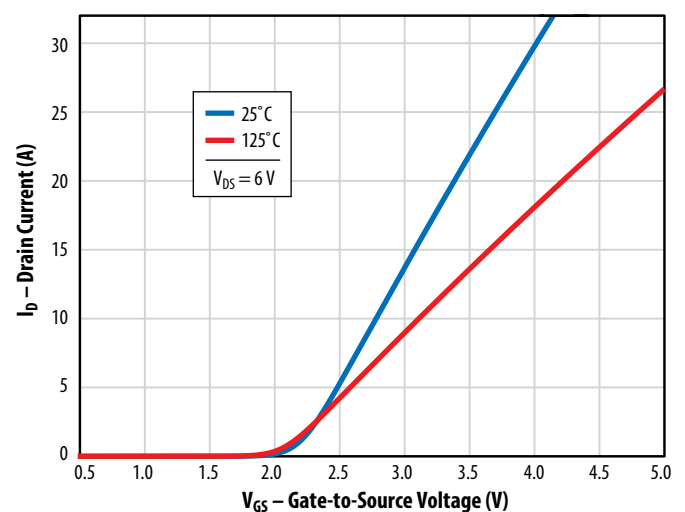
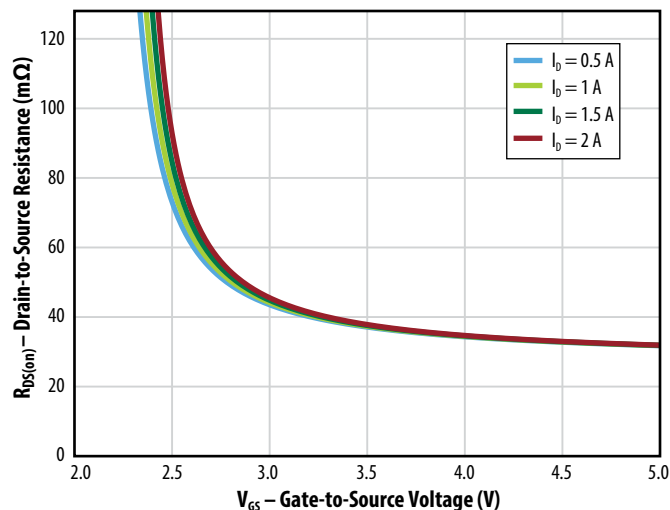
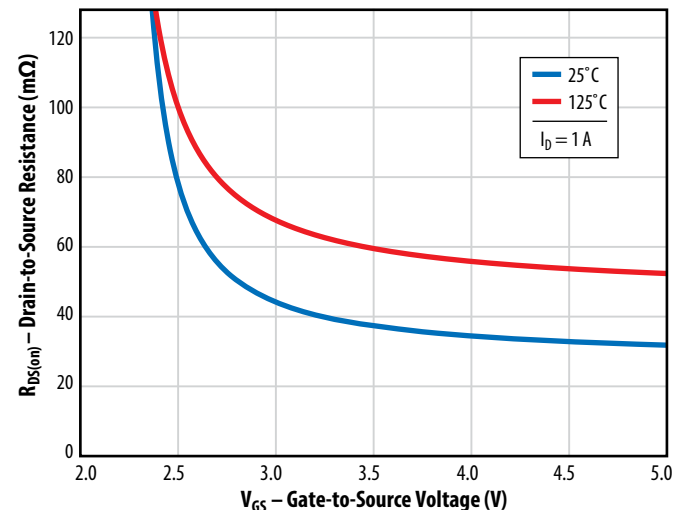
Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain CurrentsFigure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

Figure 5a: Typical Capacitance (Linear Scale)

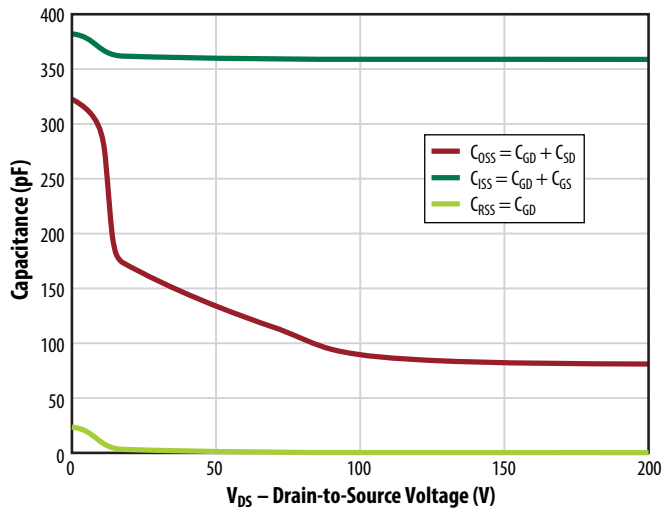


Figure 5b: Typical Capacitance (Log Scale)

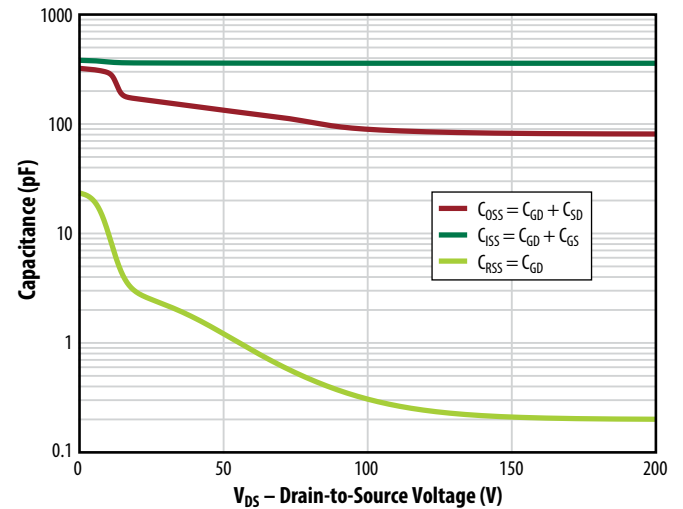
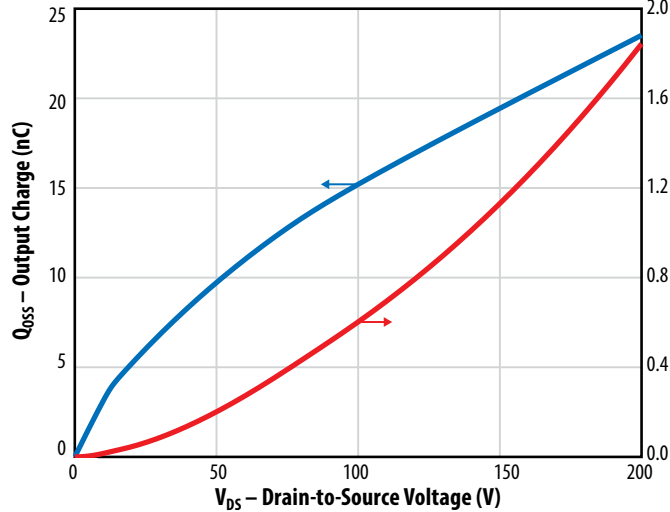
Figure 6: Typical Output Charge and C_{OSS} Stored Energy

Figure 7: Typical Gate Charge

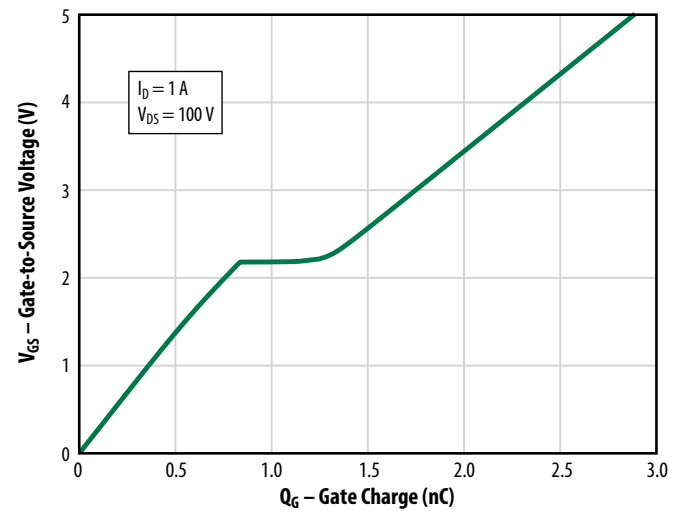


Figure 8: Typical Reverse Drain-Source Characteristics

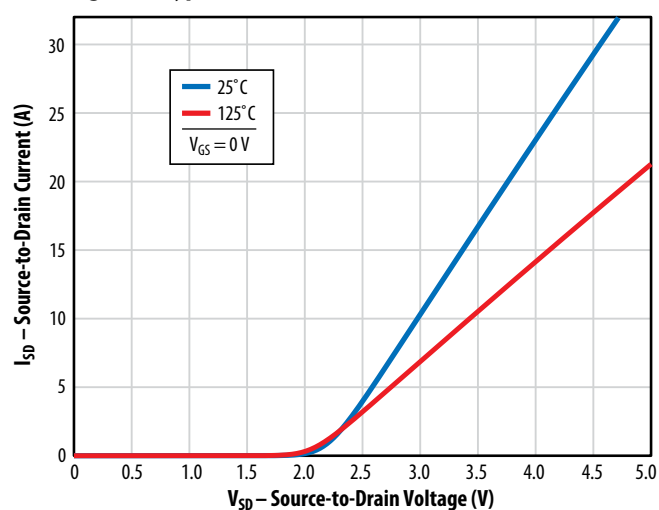
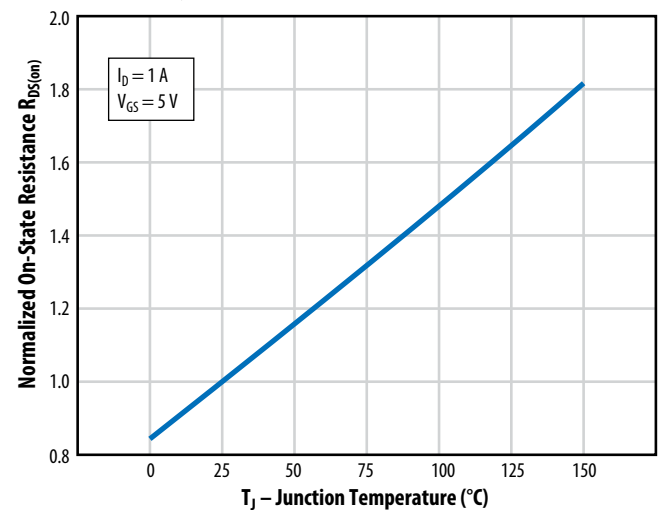


Figure 9: Typical Normalized On Resistance vs. Temperature



Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF.

All measurements were done with substrate shorted to source.

Figure 10: Typical Normalized Threshold Voltage vs. Temp.

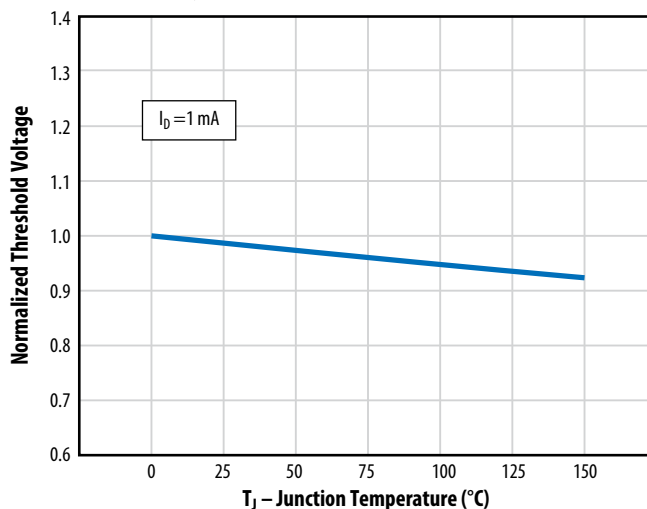


Figure 11: Typical Transient Thermal Response Curves

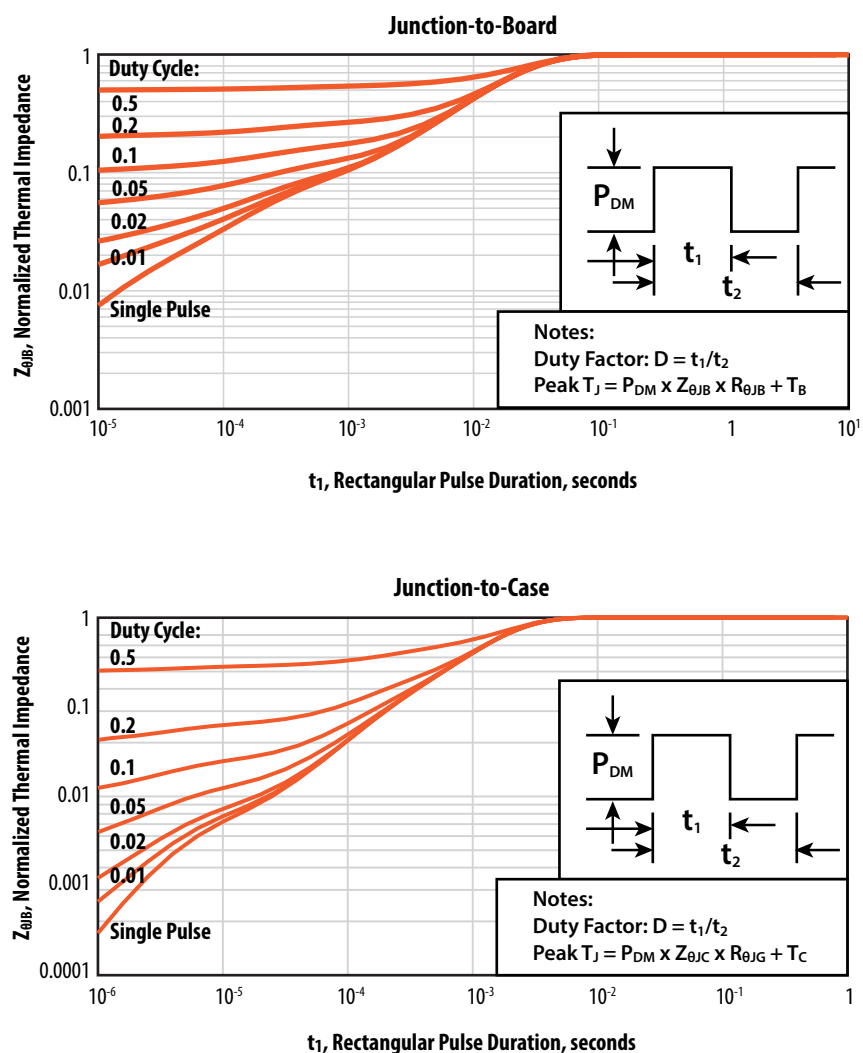
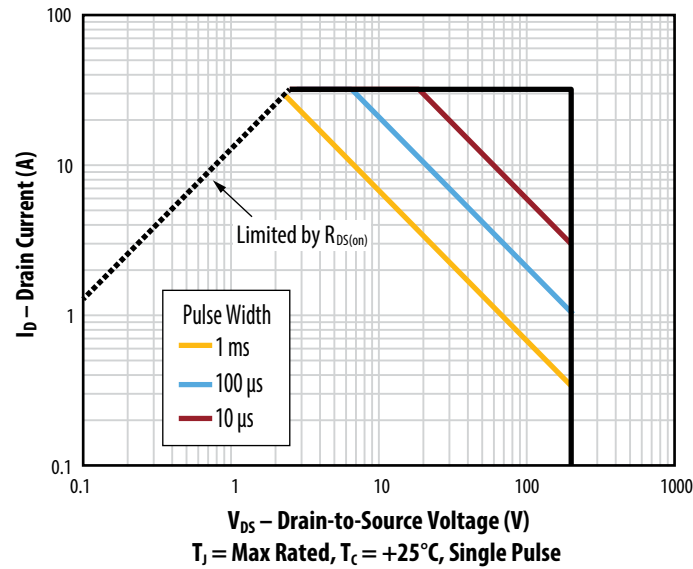
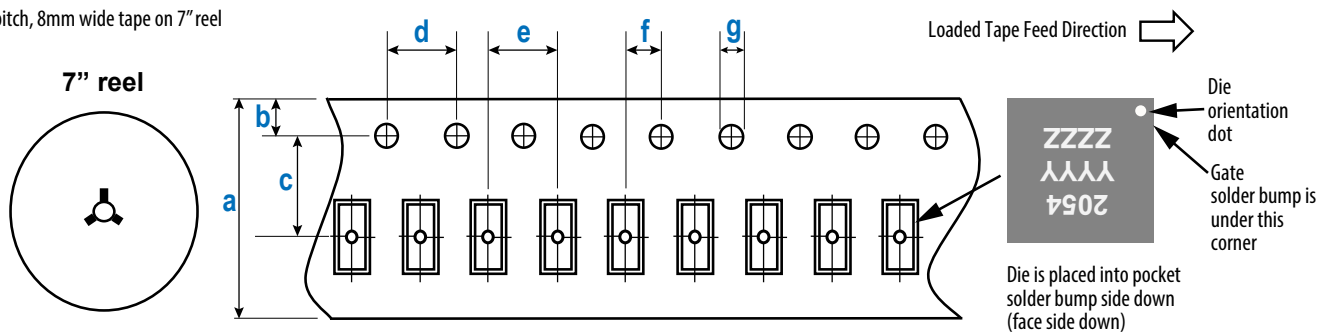


Figure 12: Safe Operating Area



TAPE AND REEL CONFIGURATION

4mm pitch, 8mm wide tape on 7" reel

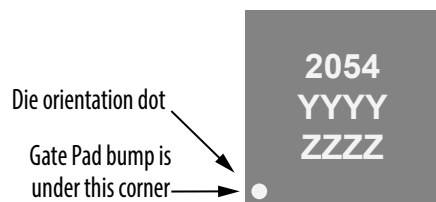


EPC2054 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

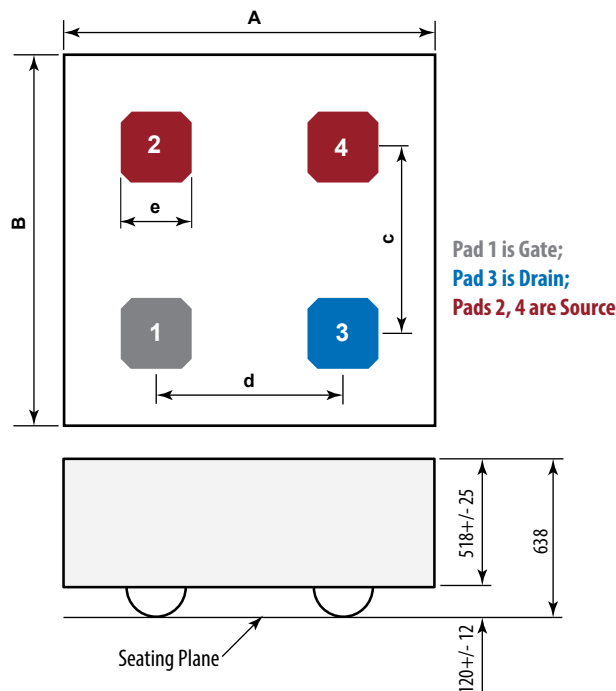
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2054	2054	YYYY	ZZZZ

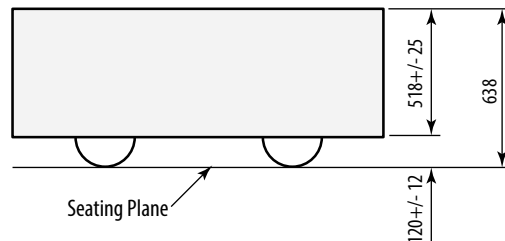
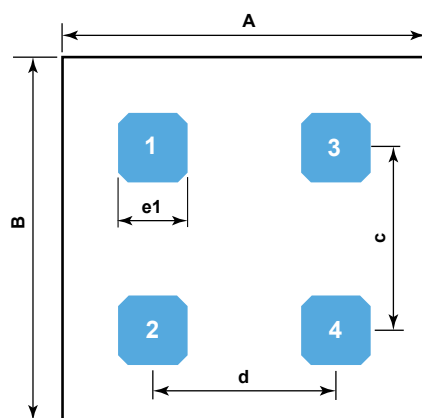
DIE OUTLINE

Solder Bump View



DIM	Micrometers		
	MIN	Nominal	MAX
A	1270	1300	1330
B	1270	1300	1330
c		650	
d		650	
e		250	

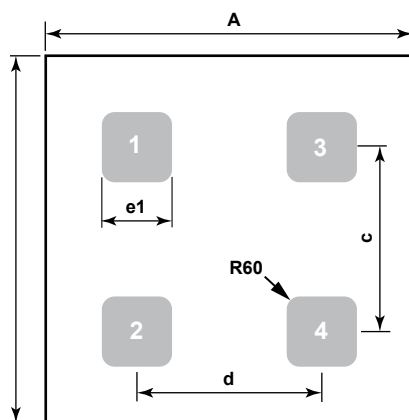
Side View

**RECOMMENDED LAND PATTERN**(measurements in μm)

DIM	Micrometers
A	1300
B	1300
c	650
d	650
e1	230

The land pattern is solder mask defined.

Pad 1 is Gate;
Pad 3 is Drain;
Pads 2, 4 are Source

RECOMMENDED STENCIL DRAWING(measurements in μm)

DIM	Micrometers
A	1300
B	1300
c	650
d	650
e1	230

Recommended stencil should be 4mil (100 μm) thick, must be laser cut, openings per drawing.

The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at
<https://epc-co.com/epc/design-support>

Efficient Power Conversion Corporation (EPC) reserves the right to make changes without further notice to any products herein to improve reliability, function or design. EPC does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights, nor the rights of others.

eGaN® is a registered trademark of Efficient Power Conversion Corporation.

EPC Patent Listing: <https://epc-co.com/epc/about-epc/patents>

Information subject to change without notice.