SY26190VDQ

High-Efficiency, 20A, 16V Input Synchronous Step-Down Regulator

General Description

The SY26190VDQ high-efficiency synchronous step-down DC-DC regulator operates over a wide input voltage range of 3.6V to 16V, and can deliver continuous output current up to 20A. The output voltage is adjustable from 0.6V to 5.5V. It integrates an internal 8.6mΩ main switch and a 2.5mΩ synchronous switch with very low $R_{DS(ON)}$ to minimize conduction loss and provide excellent efficiency for a wide range of applications, especially for low output voltages and low duty cycles. The 1.5MHz pseudoconstant switching frequency enables using small external inductor and capacitor values.

Silergy's proprietary Instant-PWM™ fast-response, constant-on-time (COT) PWM control method supports high input/output voltage ratios (low duty cycles) and responds to load transients within approximately 100ns while maintaining a near-constant operating frequency over line, load, and output voltage ranges. This control method provides stable operation without complex compensation, even with low-ESR ceramic output capacitors.

The stable internal reference (V_{REF}) provides ±1% accuracy over T_J of -40°C to 125°C, and the differential input sense configuration allows feedback sensing at the most relevant load point.

Cycle-by-cycle current limit, input undervoltage lock-out, internal soft-start, output undervoltage and overvoltage protection, and thermal shutdown provide safe operation in all operating conditions.

The SY26190VDQ is available in a compact QFN3mm×4mm package.

Features

- Wide 3.6–16V Input Voltage Range (Minimum of 2.9V with External V_{CC} Applied)
- Up to 20A Output Current
- Low $R_{DS(ON)}$ for Internal Switches: 8.6mΩ Main, 2.5mΩ Synchronous
- 600kHz/800kHz/1000kHz Operating Frequency
- Accurate Feedback Setpoint: 0.6V ±1%
- Differential Remote Sense
- Fast Transient Response
- Selectable Automatic High-Efficiency Discontinuous Operating Mode At Light Loads
- Programmable Valley-Current Limit
- Automatic Recovery for Input Undervoltage (UVLO), Output Undervoltage (UVP), and Overtemperature (OTP) Conditions
- Cycle-by-Cycle Valley and Peak Current Limit (OCP)
- Cycle-by-Cycle Reverse-Current Limit
- Internal Soft-Start Limits Inrush Current
- Smooth Pre-Biased Startup
- Power-Good Output Monitor for Undervoltage and Overvoltage

Applications

- Telecom and Networking Systems
- Servers
- High-Power Access Points
- Storage Systems
- Cellular Base Station

Typical Application

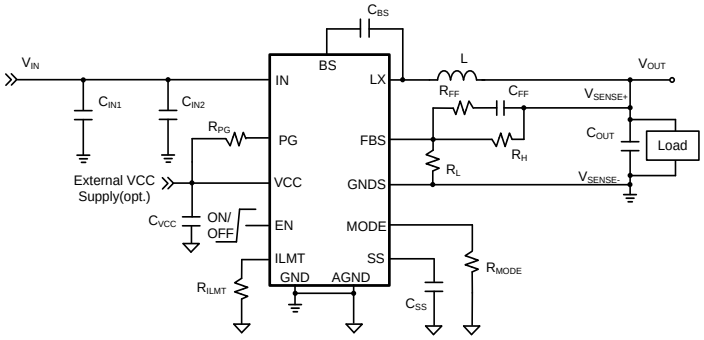


Figure 1. Typical Application Circuit

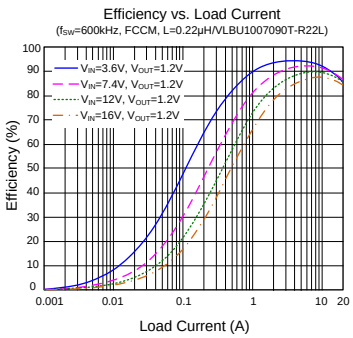


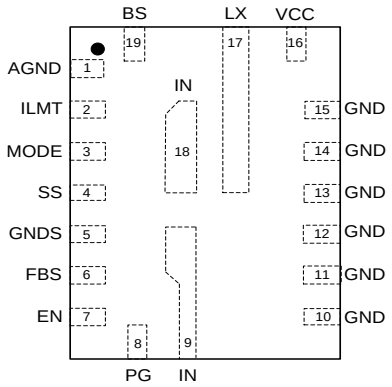
Figure 2. Efficiency vs. Load Current

Ordering Information

Ordering Part Number	Package type	Top Mark
SY26190VDQ	QFN3×4-19 RoHS-Compliant and Halogen-Free	**EDH***xyz*

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	AGND	Analog ground.
2	I_{LMT}	Synchronous rectifier current-limit setting. Connect a resistor to AGND to set the inductor valley-current limit. See detailed description.
3	MODE	Operation mode selection. Program MODE to select FCCM/DCM and the operating switching frequency. See Table 1**.**
4	SS	External soft-start setting. Optionally adjust the soft-start time by adding an appropriate external capacitor between this pin and AGND pin.
5	GNDS	Remote ground sense. Connect this pin directly to the negative side of the preferred voltage sense point. Short to GND if remote sense is not used.
6	FBS	Remote feedback sense. Connect this pin to the center point of the output resistor-divider to program the output voltage.
7	EN	Enable input. Pull low to disable the device; pull high to enable. Do not leave this pin floating. May be used for increasing startup voltage or sequencing.
8	PG	Power-good indicator. Open-drain output when the output voltage is within 92.5% to 120% of the regulation setpoint.
9,18	IN	Power input. Decouple this pin to the GND pin with at least a 30µF ceramic capacitor.
10, 11, 12, 13, 14, 15	GND	Power ground.
16	V_{CC}	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuits. Decouple this pin to GND with at least a 1µF ceramic capacitor. Make a single Kelvin connection from AGND to the V_{CC} capacitor GND connection. Use short, direct connections and avoid the use of vias. May be driven by an external bias supply.
17	LX	Inductor pin. Connect this pin to the switching node of the inductor.
19	BS	Bootstrap supply for the high-side gate driver. Connect a 0.1µF ceramic capacitor between the BS and the LX pins.

Block Diagram

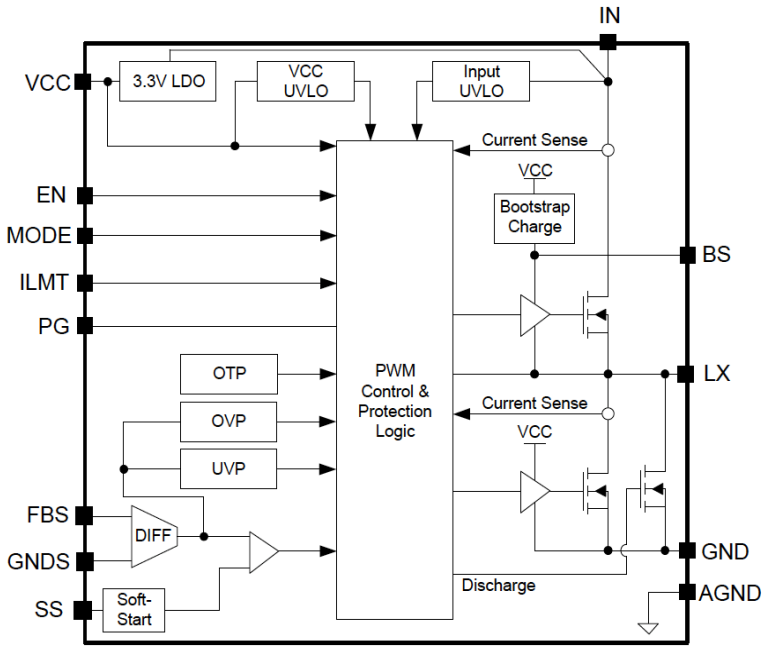


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	18	V
I_{LMT}, SS	-0.3	4	
EN, MODE, LX	-0.3	IN + 0.3	
LX, 10ns Duration	-5	IN + 5	
BS	LX - 0.3	LX + 4	
FBS, GNDS, AGND, V_{CC}, PG	-0.3	4	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	24	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	4.5	
P_D Power Dissipation T_A = 25°C	4.2	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	2.9	16	V
Output Voltage	0.6	5.5	
GNDS	-0.2	0.2	
Output Current		20	A
Output Current-Limit Setting		24	
Peak Inductor Current		28	
Junction Temperature	-40	125	°C

Electrical Characteristics

(V_{IN} = 12V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise specified.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage	V_{IN}		2.9		16	V
	UVLO, rising	$V_{IN,UVLO}$		2.6	2.75	2.9	V
	UVLO, Hysteresis	$V_{IN,HYS}$			200		mV
	Shutdown Current	I_{SHDN}	V_{EN} = 0V, T_J = 25°C		2	5	μA
	Quiescent Current	I_Q	V_{EN} = 2V, V_{FBS} = 0.65V, DCM mode, not switching		550	850	μA
V_{CC}	UVLO, Rising	$V_{VCC,UVLO}$				2.5	V
	UVLO, Hysteresis	$V_{VCC,HYS}$			100		mV
	Output	V_{CC}	I_{VCC} = 0mA	3.15	3.3	3.45	V
	Load Regulation	$V_{CC,REG}$	I_{VCC} = 25mA		1.4		%
FBS	Reference Voltage	V_{REF}	GNDS = 0V	0.594	0.600	0.606	V
	Error Amp Offset	V_{OS}		-3		3	mV
	Input Current	I_{FBS}	V_{EN} = 2V, V_{FBS} = 1V	-50	0	50	nA
Power Switch	On-Resistance	$R_{DS(ON)HS}$	V_{BS-LX} = 3.3V, T_J = 25°C		8.6	12.9	mΩ
	Leakage	$I_{HS, LKG}$	V_{EN} = 0V, V_{LX} = 0V		0.01	8	μA
	Current Limit	$I_{LMT,HS}$		25	32.5	40	A
Synchronous Rectifier	On-Resistance	$R_{DS(ON)LS}$	V_{CC} = 3.3V, T_J = 25°C		2.5	3.8	mΩ
	Leakage	$I_{LS, LKG}$	V_{EN} = 0V, V_{LX} = 12V		0.04	32	μA
	Reverse Current	$I_{LMT,RVS}$		9	13	16	A
		$t_{RCL,BLK}$		40	60		ns
I_{LMT} Pin Output Voltage		V_{ILMT}		1.15	1.2	1.25	V
I_{LMT} Ratio		$I_{ILMT}/I_{LMT,BOT}$	$I_{LMT,BOT}$ > 5A	9	10	11	μA/A
Discharge FET Resistance		R_{DIS}			120		Ω
Enable (EN)	Rising Threshold	$V_{EN,R}$		1.18	1.23	1.28	V
	Threshold Hysteresis	$V_{EN,HYS}$			0.2		V
	Input Current	I_{EN}	V_{EN} = 2V		0		μA
Soft-Start (SS)	Charging current	I_{SS1}	V_{SS} = 0V		46		μA
	Discharge current	I_{SS2}	V_{SS} = 1V		38		mA
	Min soft-start time	$t_{SS,MIN}$			1		ms
Overvoltage Protection Threshold		V_{OVP}		110	120	130	%V_{FBS}
Undervoltage Protection	threshold	V_{UVP}		47	52	57	
	Delay	$t_{UVP,DLY}$			20		μs
UVP/OCP Hiccup On-Time		$t_{HICCUP,ON}$	C_{SS} open		3		ms
UVP/OCP Hiccup Off-Time		$t_{HICCUP,OFF}$			12		
Power-Good	Thresholds	V_{PG}	V_{FBS} falling, fault	77	81	85	%V_{FBS}
			V_{FBS} rising, good	88.5	92.5	96.5	
			V_{FBS} rising, fault	110	120	130	
			V_{FBS} falling, good	102	106	110	
	Delay	$t_{PG,R}$	V_{FBS} rising, good		0.8		ms
		$t_{PG,F}$	V_{FBS} falling, fault		20		μs
	Output low voltage	$V_{PG,LOW}$	V_{IN} = 0V, 100kΩ from PG to 3.3V		550	750	mV
			V_{IN} = 0V, 10kΩ from PG to 3.3V		660	850	
			V_{EN} = 2V, V_{FBS} = 0V, I_{PG} = 10mA			0.4	V
	Output low leakage	$I_{PG,LKG}$	V_{PG} = 3.3V		3	5	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Switching Frequency	f_{SW}	R_{MODE} = 0Ω, I_{OUT} = 0A, FCCM, V_{OUT} = 1V, T_J = 25°C	510	600	690	kHz
		R_{MODE} = 30.1kΩ, I_{OUT} = 0A, FCCM, V_{OUT} = 1V, T_J = 25°C	690	800	910	
		R_{MODE} = 60.4kΩ, I_{OUT} = 0A, FCCM, V_{OUT} = 1V, T_J = 25°C	900	1000	1100	
Min On-Time	$t_{ON,MIN}$	I_{OUT} = 3A		60		ns
Min Off-Time	$t_{OFF,MIN}$	I_{OUT} = 3A		180		
Thermal Shutdown Temperature	T_{SD}			160		˚C
Thermal Shutdown Hysteresis	T_{HYS}			30		

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured with natural convection at T_A = 25˚C on an 8.5cm×8.5cm size four-layer Silergy evaluation board.

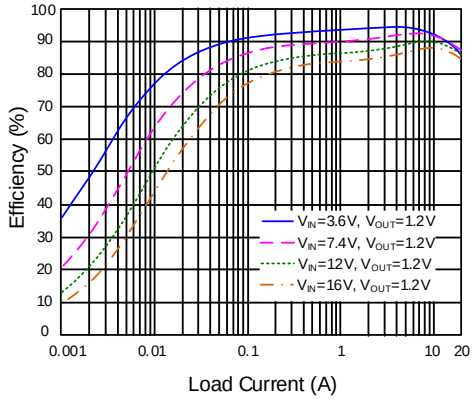
Note 3: The device is not guaranteed to function outside its recommended operating conditions.

Note 4: Production tested at 25˚C. Limits at -40°C to +125°C are guaranteed by design, test or statistical correlation.

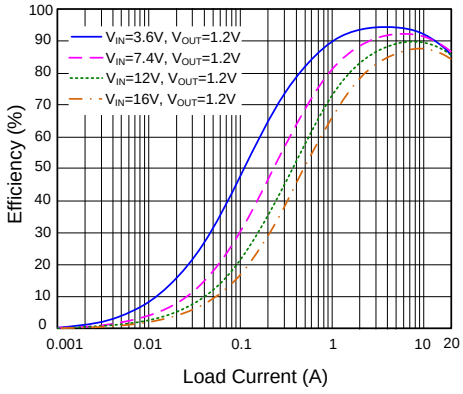
Typical Performance Characteristics

(T_A = 25 ˚C, V_{IN} = 12V, V_{OUT} = 1.2V, L = 0.22µH, C_{OUT} = 235µF, f_{SW} = 600kHz, R_{ILMT} = 5.6kΩ, C_{SS} = 0.22µF, unless otherwise noted)

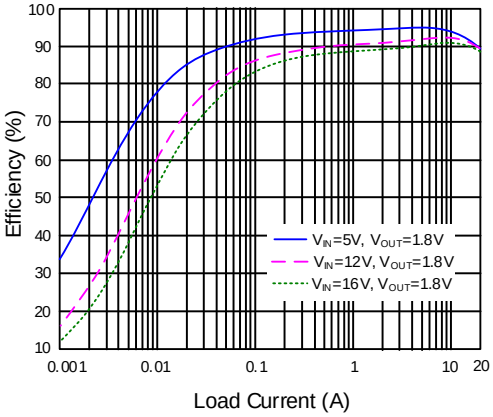
Efficiency vs. Load Current
(f_{SW}=600kHz, DCM, L=0.22µH/VLBU1007090T-R22L)



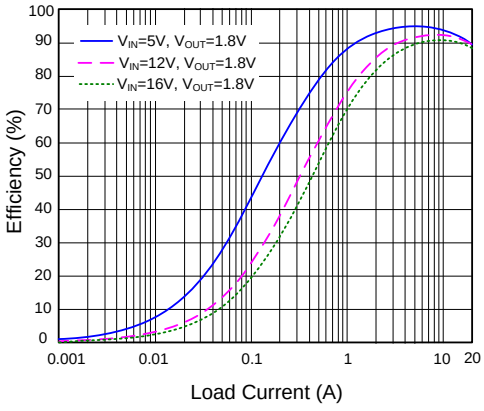
Efficiency vs. Load Current
(f_{SW}=600kHz, FCCM, L=0.22µH/VLBU1007090T-R22L)



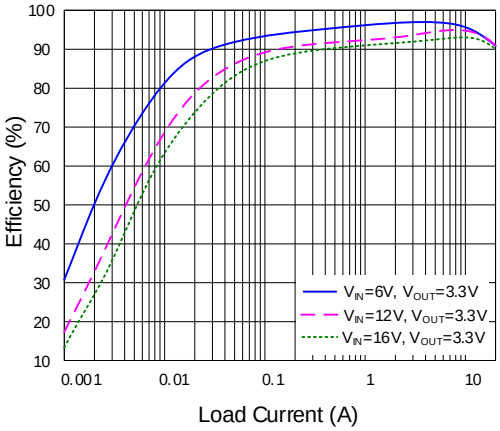
Efficiency vs. Load Current
(f_{SW}=600kHz, DCM, L=0.22µH/VLBU1007090T-R22L)



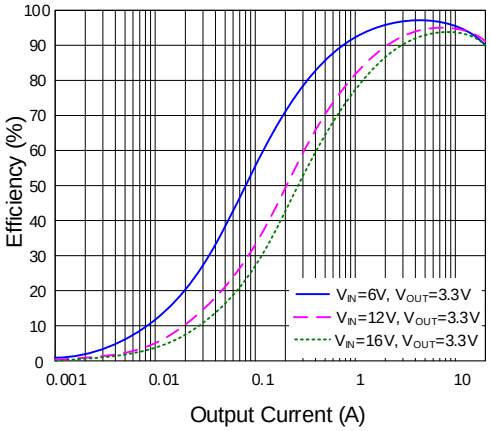
Efficiency vs. Load Current
(f_{SW}=600kHz, FCCM, L=0.22µH/VLBU1007090T-R22L)



Efficiency vs. Load Current
(f_{SW}=800kHz, DCM, L=0.47µH/PCMB104T-R47MS)

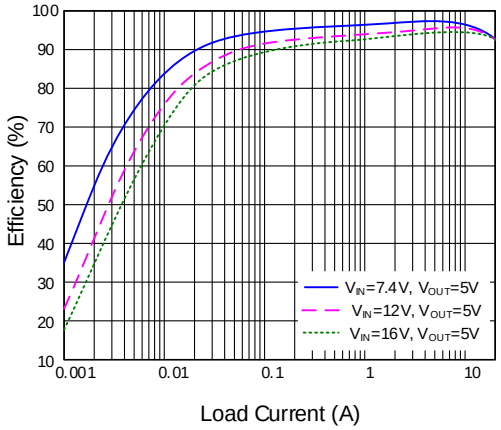


Efficiency vs. Load Current
(f_{SW}=800kHz, FCCM, L=0.47µH/PCMB104T-R47MS)



Efficiency vs. Load Current

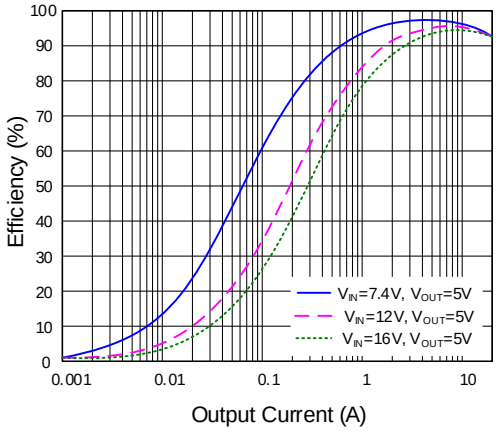
(f_{SW}=800kHz, DCM, L=0.47μH/PCMB104T-R47MS)



Load Current (A)

Efficiency vs. Load Current

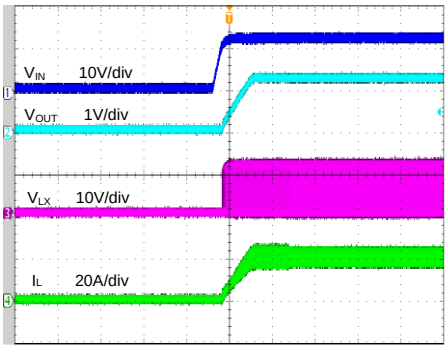
(f_{SW}=800kHz, FCCM, L=0.47μH/PCMB104T-R47MS)



Output Current (A)

Startup from V_{IN}

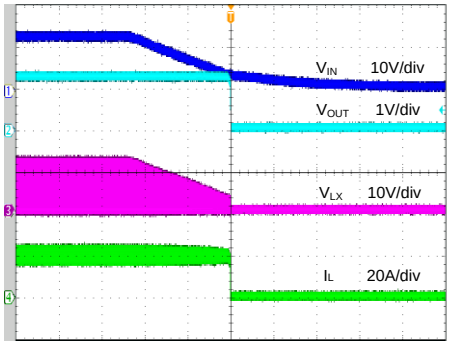
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=20A)



Time (4ms/div)

Shutdown from V_{IN}

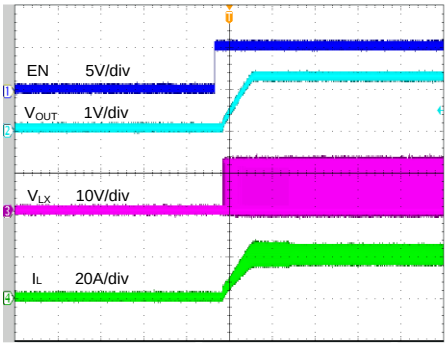
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=20A)



Time (4ms/div)

Startup from EN

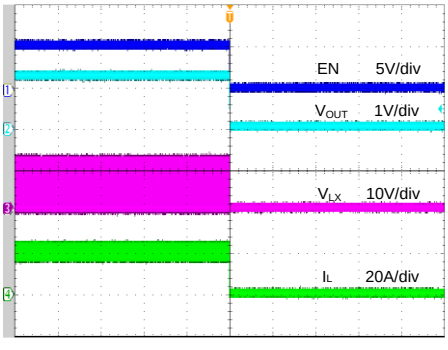
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=20A)



Time (4ms/div)

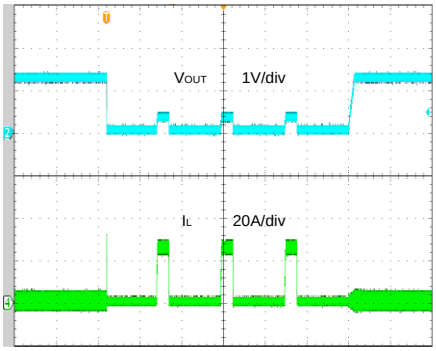
Shutdown from EN

(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=20A)



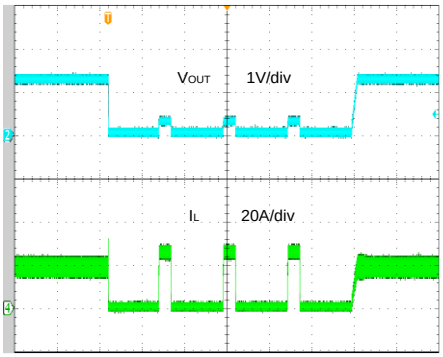
Time (4ms/div)

Short Circuit Protection
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=0A~short, R_{ILMT}=5.6kΩ, FCCM)



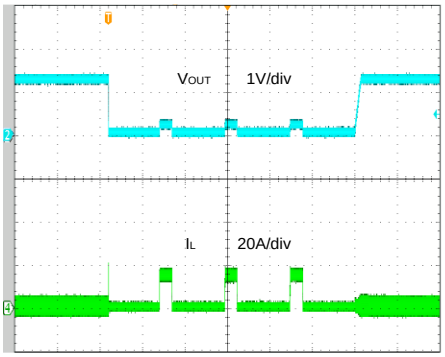
Time (20ms/div)

Short Circuit Protection
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=20A~short, R_{ILMT}=5.6kΩ)



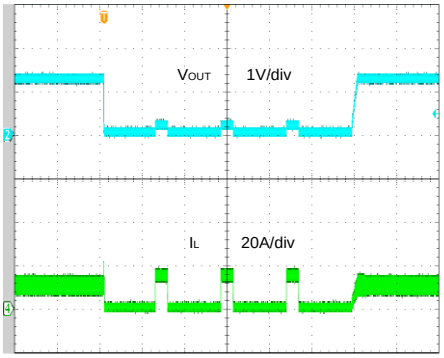
Time (20ms/div)

Short Circuit Protection
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=0A~short, R_{ILMT}=10kΩ, FCCM)



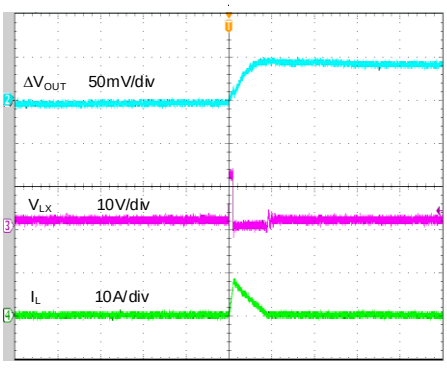
Time (20ms/div)

Short Circuit Protection
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=10A~short, R_{ILMT}=10kΩ)



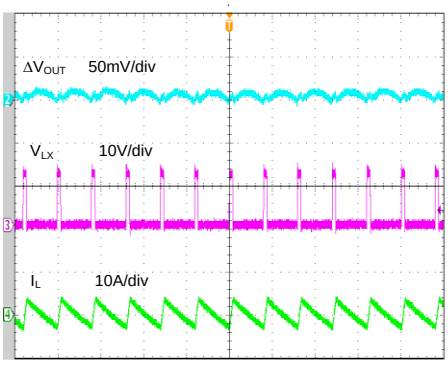
Time (20ms/div)

Output Ripple
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=0A, DCM)



Time (2μs/div)

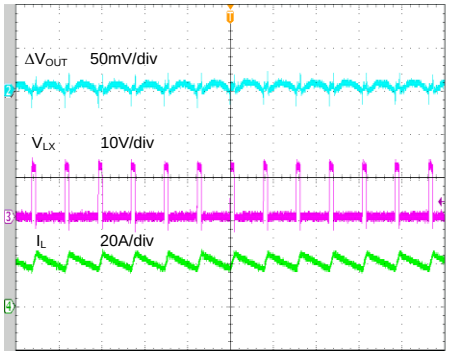
Output Ripple
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=0A, FCCM)



Time (2μs/div)

Output Ripple

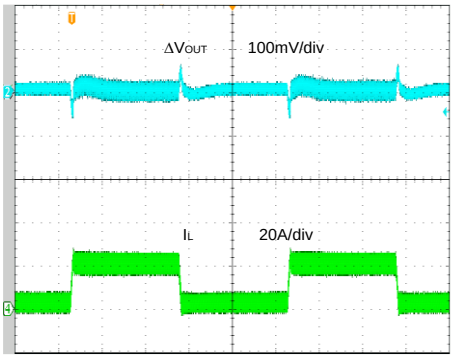
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=20A)



Time (2μs/div)

Load Transient

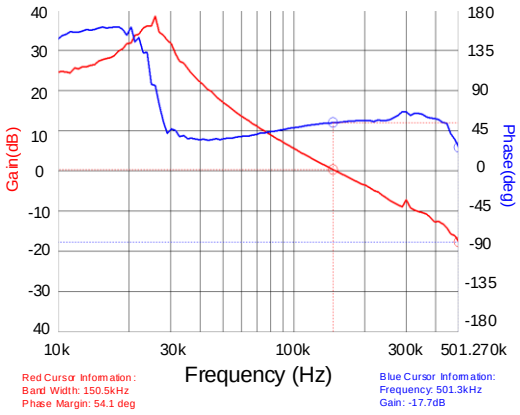
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=2~20A, FCCM)



Time (200μs/div)

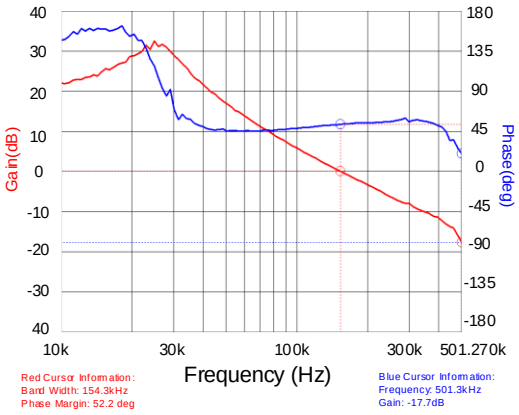
Bode Plot

(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=10A)



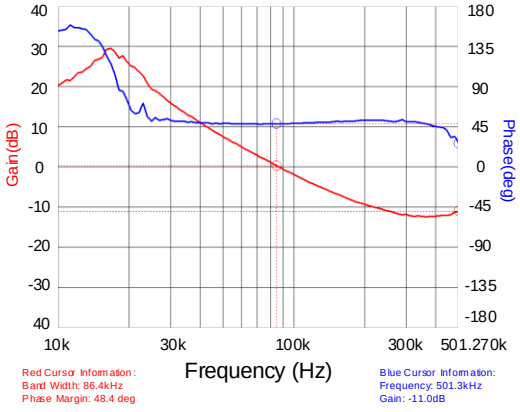
Bode Plot

(V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=10A)



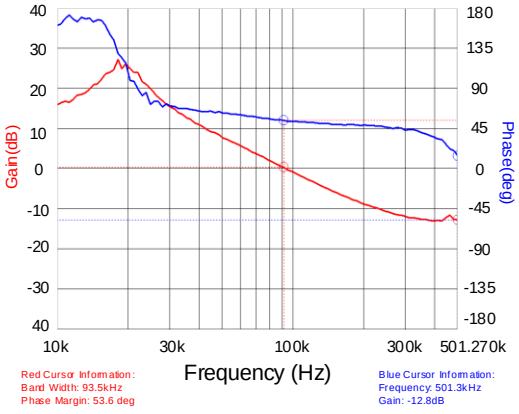
Bode Plot

(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=10A)



Bode Plot

(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=10A)



Detailed Description

Constant-On-Time Architecture

The one-shot circuit or on-time generator, which determines how long to turn on the high-side power switch, is fundamental to any constant-on-time (COT) architecture. Each on-time (t_{ON}) is a fixed period internally calculated to operate the step-down regulator at the desired switching frequency, considering the input and output voltage ratio, $t_{ON} = (V_{OUT}/V_{IN}) \times (1/f_{SW})$. For example, consider a hypothetical converter targeting 1.2V output from a 12V input at 600kHz. The target on-time is (1.2V/12V)×(1/600kHz) = 167ns. Each t_{ON} pulse is triggered by the feedback comparator when the output voltage measured at the FB pin drops below the internal voltage reference value. After one t_{ON} period, a minimum off-time ($t_{OFF,MIN}$) is imposed before any further switching is initiated, even if the output voltage is less than the target. This approach avoids making any switching decisions during the noisy periods immediately after switching events, or while the switching node (LX) is rapidly rising or falling.

There is no fixed clock in the COT control loop, so the high-side power switch can turn on almost immediately after a load transient. Subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays. Conventional current-mode or voltage-mode control methods determine when to turn off the high-side power switch and turn on the low-side synchronous rectifier based on current feedback, feedback voltage, internal ramps, and internal compensation signals, so these must all be monitored. These small signals are difficult to observe in a noisy switching environment immediately after switching large currents, which makes such architectures difficult to use.

Instant-PWM Operation

Silergy's Instant-PWM control method adds several proprietary improvements to the traditional COT architecture. First, whereas most legacy COT implementations require a dedicated connection to the output voltage terminal to calculate the t_{ON} duration, the Instant-PWM control method derives this signal internally.

Additionally, it optimizes operation with low-ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT regulators may become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor may become too small to maintain stable operation. For this reason, Instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the t_{ON} pulse is triggered as long as the minimum t_{OFF} has been satisfied and the inductor current measured flowing through the low-side synchronous rectifier is lower than the bottom FET current limit. When the t_{ON} pulse is triggered, the low-side synchronous rectifier turns off and the high-side power switch turns on. The inductor current then ramps up linearly during the t_{ON} period. At the end of the t_{ON} period, the high-side power switch turns off, the low-side synchronous rectifier turns on, and the inductor current ramps down linearly.

This action also initiates the minimum t_{OFF} timer to ensure sufficient time for stabilizing any transient conditions and settling of the feedback comparator before the next cycle is initiated. This minimum t_{OFF} is relatively short so that transient t_{ON} can be retriggered with minimal delay during high-speed load, allowing the inductor current to ramp quickly and provide sufficient energy to the load.

In order to avoid shoot-through, a dead time (t_{DEAD}) is generated internally between the high-side power switch turn-off and the low-side synchronous rectifier on-period or the low-side synchronous rectifier turn-off and the high-side power turn-on period.

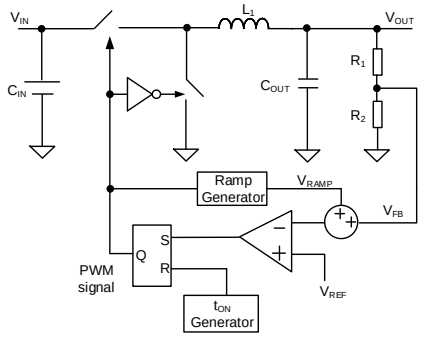


Figure 4. Instant-PWM

Frequency-Locked Loop (FLL)

Although COT provides a relatively constant operating frequency over variations in line and load conditions, Silergy's FLL improves the operating frequency performance by comparing the actual operating frequency with an internal reference frequency. The signal that results is used to adjust t_{ON}, resulting in a stable and predictable operating frequency. Note that the FLL is disabled during soft-start and during discontinuous inductor current mode (DCM) conditions. In these cases, the operating frequency will be lower than the target.

Light-Load Operating Modes

The SY26190VDQ supports two user-selectable light-load operating modes, set with the MODE input (see Table 1). Light load occurs at approximately $I_{OUT} < 0.5 \times \Delta I_L$, when the current through the low-side synchronous rectifier will ramp to near zero before the next t_{ON} time.

In forced continuous inductor current mode (FCCM), the low-side synchronous rectifier remains on until the next t_{ON} cycle, allowing continuous current flow in the inductor. The inductor current ramps below zero, recirculating current from the output to the input. This allows the device to maintain a relatively constant switching frequency over the output current range. This also reduces efficiency at light loads, but is often desirable in equipment that is sensitive to low-frequency operations, such as audio or RF systems.

In discontinuous inductor current mode (DCM), the low-side synchronous rectifier is turned off and remains off when the inductor current reaches zero, preventing recirculation current that can significantly reduce efficiency under these light-load conditions. As load current is further reduced and the V_{OUT} voltage remains greater than the REFIN voltage, the Instant-PWM control loop will not trigger another t_{ON} until needed, so the apparent operating switching frequency will drop, further enhancing efficiency. Continuous inductor current mode (CCM) resumes smoothly as soon as the load current increases sufficiently for the inductor current to remain above zero at the time of the next t_{ON} cycle. This threshold of load current may be determined as follows:

$$I_{OUT\_CTL} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW} \times L_1}$$

Note that the operating frequency of the device in DCM can be very low, and may not be desirable in equipment that is sensitive to low-frequency operations such as audio or RF systems.

Switching Frequency

The SY26190VDQ supports three user-selectable operating frequencies: 600kHz, 800kHz and 1,000kHz. See Table 1.

MODE Input

The MODE pin is an input that provides user-selectable operating frequency, light-load operating modes, and current-limit value. See Table 1 for configuration details. Note that this input is evaluated during startup of the device, and changes to the configuration after startup will not change the device operation. Any change in the configuration requires a restart of the device.

Table 1. MODE Configuration

MODE Pin Connection	Light-Load Mode	Switching Frequency
V_{CC}	DCM	600kHz
240kΩ(±20%) to GND	DCM	800kHz
120kΩ(±20%) to GND	DCM	1000kHz
GND	FCCM	600kHz
30kΩ(±20%) to GND	FCCM	800kHz
60kΩ(±20%) to GND	FCCM	1000kHz

Input Undervoltage Lockout (UVLO)

The SY26190VDQ incorporates input undervoltage lockout (UVLO) protection to prevent operation before all internal circuitry is ready, and to ensure that the top FET and bottom FET are properly biased. The SY26190VDQ remains in a low-current state and all switching actions are inhibited until V_{IN} exceeds its rising threshold. At that time, if EN is enabled, the device will start up by initiating a soft-start ramp. If V_{IN} subsequently falls below $V_{IN,UVLO}$ by more than the input UVLO hysteresis, switching actions are again suppressed. In some systems, it may be desirable to ensure that the device remains in shutdown until Vin is even higher. See EN input description.

Enable Control (EN)

The EN input is a high-voltage-capable input with an accurate logic-compatible threshold voltage. In many systems, pulling EN high from V_{IN} to enable the device is sufficient. However, EN may be used to control startup more precisely by taking advantage of the accurate threshold $V_{EN,R}$ using a resistor-divider, as shown in Figure 5.

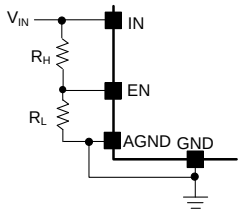


Figure 5. Enable Control

When EN is driven below approximately 0.4V, the V_{CC} regulator will be shut down. It is not recommended to connect EN and IN directly. Use a resistor in the range of 1kΩ to 1MΩ if EN is pulled high by IN.

V_{CC} Linear Regulator

An internal linear regulator (V_{CC}) produces a 3.3V supply from V_{IN} that powers the internal gate drivers, PWM logic, analog circuitry, and other blocks. Connect a 1µF low-ESR ceramic capacitor from V_{CC} to GND. This regulator incorporates undervoltage lockout protection $V_{VCC,UVLO}$.

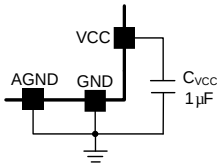


Figure 6. V_{CC} Linear Regulator

V_{CC} may also be used to apply an external 3.3V power source, if available. This external bias will allow device operation with V_{IN} as low as 2.9V

Startup and Shutdown

The SY26190VDQ incorporates an internal soft-start circuit to smoothly ramp the output to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows the output to rise to the desired voltage over approximately one soft-start time, T_{SS}, which avoids high current flow and transients during startup. The startup and shutdown sequences are shown in Figure 7.

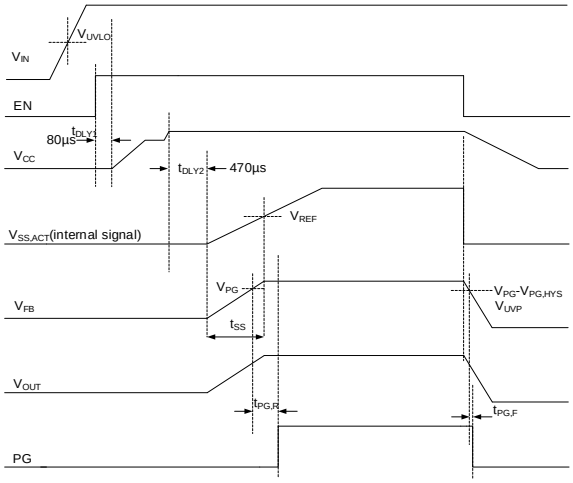


Figure 7. Startup and Shutdown Sequences

Programmable Soft-start Time and On-time Pre-bias Function

The soft-start time is a minimum of 1ms but may be extended by connecting a capacitor between the SS and AGND pins. The soft-start time equation is:

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}}{I_{SS}(\mu A)}$$

where I_{SS} approximately 46µA.

Increasing t_{SS} with an external capacitor also increases $t_{HICCUP,ON}$ and $t_{HICCUP,OFF}$ proportionally.

During startup where the output is greater than zero, a pre-biased condition, switching will be disabled until the voltage on the internal soft-start circuit voltage $V_{SS,ACT}$ exceeds the sensed output voltage at FB. Before switching is initiated, the on-time generator will set t_{ON} to match the pre-bias output voltage.

Note that in a pre-biased scenario, if the BS-LX voltage is lower than 1.8V, the low-side synchronous rectifier will be turned on for one narrow pulse. Any drop in the pre-biased output level as a result is negligible.

GNDS Differential Output Remote Ground Sense

The SY26190VDQ features a dedicated remote ground-sense pin GNDS to improve output voltage accuracy at the load. Connect this pin directly to the negative side of the preferred voltage sense point. Short to AGND if remote sense is not used.

Output Discharge Function

An internal discharge FET of approximately 120Ω is turned on whenever the shutdown logic is triggered, discharging the output through the inductor. Although only active during the shutdown process, this brings the output to a low-voltage state until the device is once again enabled.

Power-Good Indicator (PG)

PG is an open-drain output controlled by a window comparator connected to the feedback signal. PG allows system monitoring of the device. If V_{FB} is greater than $V_{PG,R}$ and less than V_{OVP} for at least $t_{PG,R}$, PG will be high-impedance.

Connect PG with a resistor in the range 10kΩ–100kΩ to V_{CC} or another voltage source less than 4V. During startup, PG is pulled to GND. PG becomes high-impedance approximately 800µs after V_{FB} reaches $V_{PG,R}$, indicating that the output is good. If V_{FB} drops below $V_{PG,F}$, or rises above V_{OVP}, and the condition remains for at least the appropriate PG delay, PG is pulled low. See the Electrical Characteristics table.

PG functionality is active even in the absence of V_{IN} or V_{CC}, as long as the pullup power source is available.

External Bootstrap Capacitor Connection

The SY26190VDQ integrates a floating power supply for the gate driver that operates the high-side power switch. Proper operation requires a 0.1µF low-ESR ceramic capacitor to be connected between the BS and LX pins. This bootstrap capacitor provides the gate driver supply voltage for the high-side N-channel MOSFET power switch.

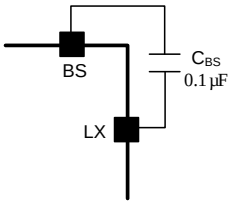


Figure 8. Bootstrap Capacitor Connection

Fault Protection

Overcurrent Protections (OCP)

Three cycle-by-cycle overcurrent protections are integrated in the SY26190VDQ to prevent excessive current flow. Although current-limit protections will not force a shutdown of the device, continuous operation in these conditions is expected to result in the output voltage dropping below the undervoltage protection threshold, or for the junction temperature to rise above the thermal protection limit, which will shut down the device. See the UVP and OTP sections.

Valley-Current Limit

Inductor current is measured in the low-side synchronous rectifier when it turns on and as the inductor current ramps down. If the current exceeds $I_{LMT,BOT}$ the synchronous rectifier is turned off and t_{ON} is inhibited until the current is less than $I_{LMT,BOT}$.

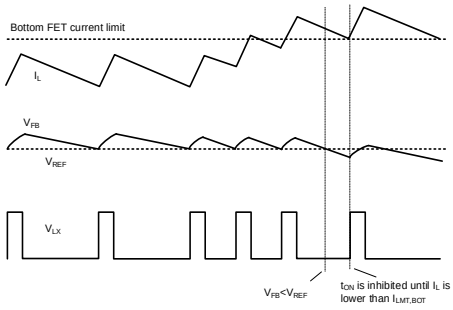


Figure 9. Valley-Current Limit

$I_{LMT,BOT}$ may be adjusted by selecting R_{ILIMIT} as follows:

$$I_{BOT,LMT} = \frac{V_{ILMT}}{G_{MIRROR} \times R_{ILMT}(\Omega)}$$

where V_{ILMT} is 1.2V and the low-side synchronous rectifier mirror ratio G_{MIRROR} is approximately 10µA/A.

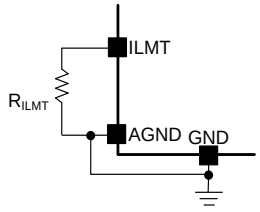


Figure 10. Valley-Current Limit

Peak-Current Limit

During t_{ON}, and after $t_{ON,MIN,}$ if the high-side power switch current exceeds $I_{LMT,HS}$, the switch is turned off, the low-side synchronous rectifier is turned on, and t_{ON} is inhibited until the low-side synchronous rectifier current is below $I_{LMT,BOT}$. Peak-current limit is disabled during initial t_{ON} at startup.

Reverse-Current Limit

In FCCM mode, if the low-side synchronous rectifier current exceeds $I_{LMT,RVS}$ for more than $t_{RCL,BLK}$, the low-side synchronous rectifier is turned off and the high-side power switch is turned on. Reverse-current limit is disabled during initial t_{OFF} at startup.

Output Undervoltage Protection (UVP)

After startup, if FBS drops below V_{UVP} for more than $t_{UVP,DLY,}$ UVP will be triggered and the SY26190VDQ will shut down for $t_{HICCUP,OFF}$. The device will then restart with a complete soft-start cycle. If the fault condition remains after $t_{HICCUP,ON}$ this 'hiccup' cycle of startup and shutdown will continue unless the junction temperature exceeds T_{SD}. If the fault condition is resolved, the device will resume normal operation.

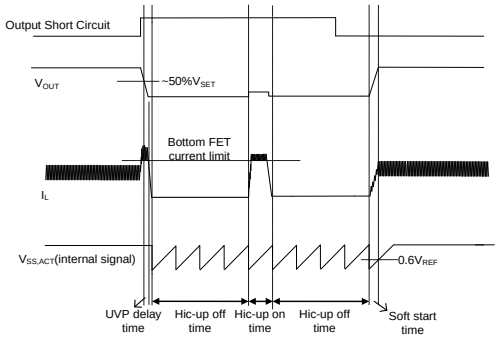


Figure 11. Output Undervoltage Protection

Output Overvoltage Protection (OVP)

If FBS exceeds $V_{OVP,}$ the low-side synchronous rectifier will be turned on in an attempt to bring the FBS below $V_{OVP.}$ If DCM operation has been selected, the low-side synchronous rectifier will remain on until the inductor current reaches zero. If FBS still exceeds $V_{OVP,}$ the operating mode will be changed to FCCM, with the low-side synchronous rectifier remaining on at a very high duty factor, pulling the inductor current as low as $I_{LMT,RVS}$. This continues until FBS is once again in regulation or until the junction temperature exceeds T_{SD}.

Overtemperature Protection (OTP)

The overtemperature protection (OTP) circuitry prevents overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds T_{SD}. Once the junction temperature cools down by approximately 30°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the T_{SD}.

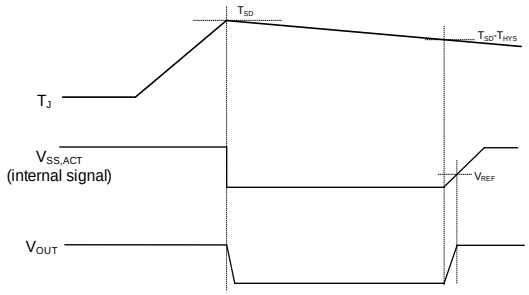


Figure 12. Overtemperature Protection

Application Information

Feedback Resistor-Divider R1 and R2

Choose R1 and R2 to program the proper output voltage. A value between 10kΩ and 1MΩ is recommended for both resistors to minimize power consumption under light loads. If V_{SET} is 1.2V and R_1 = 100kΩ, then R2 can be calculated to be 100kΩ using the following equation:

$$R_2 = \frac{0.6V}{V_{SET}\text{-}0.6V} \times R_1$$

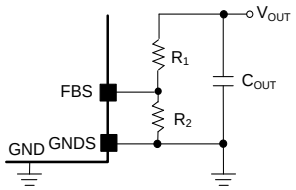


Figure 13. Feedback Resistor-Divider

Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R or X7R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current,

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated by

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1\text{-}D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications two 22µF X5R capacitors are sufficient. Place the ceramic input capacitors as close to the device IN and GND pins as possible.

Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage.

Instant-PWM™ operates well over a wide range of inductor values. This flexibility allows for optimization to find the best trade-off of efficiency, cost, and size for a particular application. Selecting a low inductor value will help reduce size and cost, and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low-value inductors may help reduce DC losses and increase efficiency. Higher inductor values tend to have higher DCR and will slow the transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current (ΔI_L) approximately 20–50% of the desired full output load current. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_{SW}), the maximum output current ($I_{OUT,MAX}$), and estimated ΔI_L as a percentage of that current:

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak-current inductor current $I_{L,PEAK}$.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

$$I_{L,PEAK} = I_{OUT,MAX} \times \frac{\Delta I_L}{2}$$

Select an inductor with a saturation current and thermal rating in excess of $I_{L,PEAK}$.

For maximum efficiency, select an inductor with a low DCR that meets the inductance, size, and cost targets. Low-loss ferrite materials should be considered.

Inductor Design Example

Consider a typical design for a device providing $1.2V_{OUT}$ at 20A from $12V_{IN}$, operating at 600kHz and using target inductor ripple current (ΔI_L) of 50%, or 10A. Determine the approximate inductance value first:

$$L_1 = \frac{1.2V \times (12V - 1.2V)}{12V \times 600kHz \times 10A} = 0.18\mu H$$

Next, select the nearest standard inductance value, in this case 0.22µH, and calculate the resulting inductor ripple current (ΔI_L):

$$\Delta I_L = \frac{1.2V \times (12V - 1.2V)}{12V \times 600kHz \times 0.22\mu H} = 8.18A$$

$$I_{L,PEAK} = 20A + 8.18A/2 = 24.09A$$

The resulting 8.18A ripple current is 8.18A/20A is approximately 40.9%, well within the 20%– 50% target.

$$I_{L,PEAK,RVS} = 8.18A/2 = 4.09A < I_{LIM,RVS}$$

Finally, select an available inductor with a saturation current higher than the resulting $I_{L,PEAK}$ of 24.09A.

Output Capacitor Selection

Instant-PWM provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

Output Ripple

Output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors ESR (ESR ripple) as well as the stored charge (capacitive ripple). When considering the total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with ΔI_L = 8.18A using five 47µF ceramic capacitors, each with an ESR of approximately 5mΩ for a parallel total of 235µF and 1mΩ ESR.

$$V_{RIPPLE,ESR} = 8.18A \times 1m\Omega = 8.18mV$$

$$V_{RIPPLE,CAP} = \frac{8.18A}{8 \times 235\mu F \times 600kHz} = 7.25mV$$

Total ripple = 15.43mV.

The actual capacitive ripple may be higher than the calculated value because the capacitance decreases with the voltage on the capacitor. Using a 150µF 40mΩ POS cap, the above result is as follows:

$$V_{RIPPLE,ESR} = 8.18A \times 40m\Omega = 327.20mV$$

$$V_{RIPPLE,CAP} = \frac{8.18A}{8 \times 150\mu F \times 600kHz} = 11.36mV$$

Total ripple = 338.56mV

Output Transient Undershoot/Overshoot

If very fast load transients must be supported, consider the effect of the output capacitor on the output transient undershoot and overshoot. Instant-PWM™ responds quickly to changing load conditions, but some considerations are still required, especially when using small ceramic capacitors. These capacitors have low capacitance, which results in insufficient stored energy for load transients. Output-transient undershoot and overshoot have two causes: voltage changes caused by the ESR of the output capacitor, and voltage changes caused by the output capacitance and inductor current slew rate.

ESR undershoot or overshoot may be calculated as $V_{ESR} = \Delta I_{OUT} \times ESR$. Using the ceramic capacitor example above and a fast load transient of ±10A, V_{ESR} = ±10A × 1mΩ = ±10mV. The POS capacitor result with the same load transient is V_{ESR} = ±10A × 40mΩ = ±400mV.

Capacitive undershoot (load increasing) is a function of the output capacitance, the load step, the inductor value and the input-output voltage difference and the maximum duty factor. During a fast load transient, the maximum duty factor of instant-PWM is a function of t_{ON} and the minimum t_{OFF} as the control scheme is designed to rapidly ramp the inductor current by grouping together many t_{ON} pulses in this case. The maximum duty factor D_{MAX} may be calculated by

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF,MIN}}$$

Given this, the capacitive undershoot may be calculated as

$$V_{UNDERSHOOT,CAP} = -\frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times (V_{IN,MIN} \times D_{MAX} - V_{OUT})}$$

Consider a 10A load increase using the ceramic capacitor case when V_{IN} = 12V. At V_{OUT} = 1.2V, the result is t_{ON} = 167ns, $t_{OFF,MIN}$ = 180ns, D_{MAX} = 167 / (167 + 180) = 0.481 and

$$V_{UNDERSHOOT,CAP} = -\frac{0.22\mu H \times (10A)^2}{2 \times 235\mu F \times (12V \times 0.481 - 1.2V)} = -10.23mV$$

Using the POS capacitor, the calculated undershoot is

$$V_{UNDERSHOOT,CAP} = -\frac{0.22\mu H \times (10A)^2}{2 \times 150\mu F \times (12V \times 0.481 - 1.2V)} = -16.04mV$$

Capacitive overshoot (load decreasing) is a function of the output capacitance, the inductor value and the output voltage.

$$V_{OVERSHOOT,CAP} = \frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times V_{OUT}}$$

Consider a 10A load decrease using the ceramic capacitor case above. At V_{OUT} = 1.2V the result is

$$V_{OVERSHOOT,CAP} = \frac{0.22\mu H \times (10A)^2}{2 \times 235\mu F \times 1.2V} = 39.01mV$$

Using the POS capacitor, the calculated overshoot is

$$V_{OVERSHOOT,CAP} = \frac{0.22\mu H \times (10A)^2}{2 \times 150\mu F \times 1.2V} = 61.11mV$$

Combine the ESR and capacitive undershoot and overshoot to calculate the total overshoot and undershoot for a given application.

Load-Transient Considerations:

The internal compensation of this device is sufficient for most low-duty cycle applications. In applications with fast, dynamic load currents, adding an RC feed-forward compensation network R_{FF} and C_{FF} may further improve the transient responses. R_{FF} = 1kΩ and C_{FF} = 220pF have been shown to perform well in most applications. Increase C_{FF} will speed up the load transient response but may reduce stability.

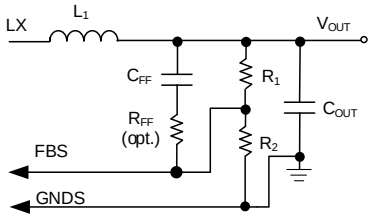


Figure 14. Feed-Forward Network

Note: when C_{OUT} > 500µF and minimum load current is low, use the feed-forward values as R_{FF} = 1kΩ and C_{FF} > 2.2nF to provide sufficient ripple at the FB pin.

Thermal Design Considerations

The maximum power dissipation depends on multiple factors: PCB layout, IC package thermal resistance, local airflow, and the junction temperature relative to ambient. The maximum power dissipation may be calculated as:

$$P_{D,MAX} = \frac{(T_{J,MAX} - T_A)}{\theta_{JA}}$$

Where, $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is 125℃. The junction-to-ambient thermal resistance θ_{JA} is layout dependent. For the QFN3×4-19 package the thermal resistance θ_{JA} is 24°C /W when measured on a standard Silergy four-layer thermal test board. These standard thermal test layouts have a very large area with long 2-oz. copper traces connected to each IC pin and very large, unbroken 1-oz. internal power and ground planes.

To meet the performance of the standard thermal test board in a typical tiny evaluation board area, wide copper traces are required well-connected to the IC's backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane, and perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at T_A = 25°C may be calculated using the following formula:

$$P_{D,MAX} = \frac{(125°C - 25°C)}{24°C/W} = 4.2W$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA}. Use the derating curve in Figure 13 below to calculate the effect of rising ambient temperature on the maximum power dissipation.

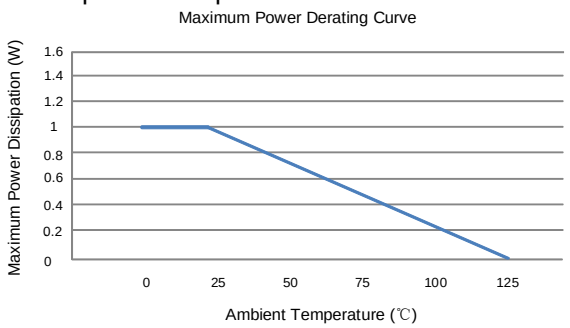
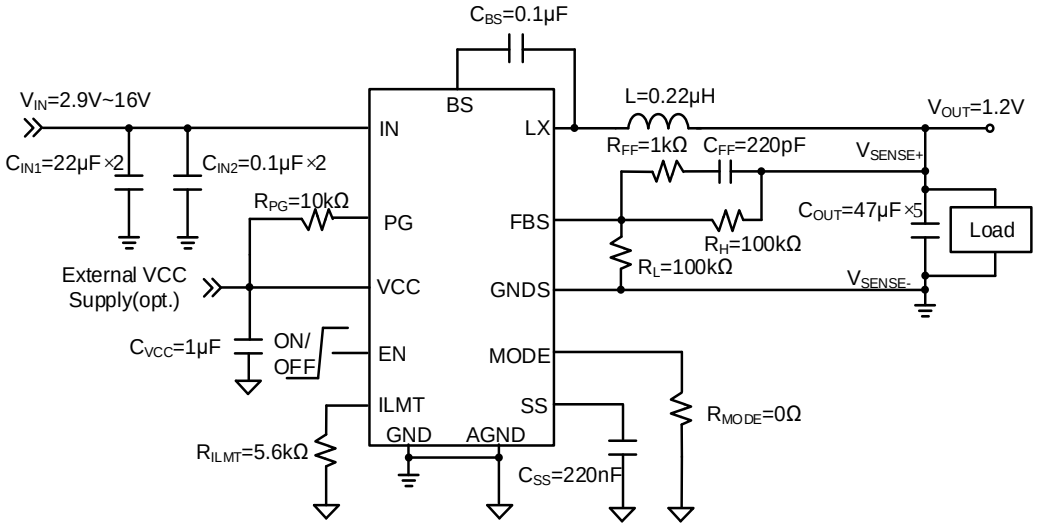


Figure 13. Maximum Power Dissipation

Application Schematic (V_{OUT} = 1.2V）



BOM List

Designator	Description	Part Number	Manufacturer
C_{IN1}	22μF/25V/X5R,1206	GRM31CR61E226ME15L	muRata
C_{IN2}	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	muRata
C_{FF}	220pF/50V/C0G, 0603	GRM1885C1H221JA01D	muRata
C_{OUT}	47μF/6.3V/X5R,1206	GRM31CR60J476KE19L	muRata
C_{SS}	220nF/50V/X5R, 0603	GRM188R61H224KAC4	muRata
C_{BS}	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	muRata
C_{VCC}	1.0μF/25V/X5R, 0603	GRM155R61E105KE11D	muRata
L	0.22μH/57A, inductor	VLBU1007090T-R22L	TDK
R1	100kΩ, 1%, 0603		
R2	100kΩ, 1%, 0603		
R_{PG}	10kΩ, 1%, 0603		
R_{MODE}	0Ω, 1%, 0603		
R_{ILMT}	5.6kΩ, 1%, 0603		
R_{FF}	1kΩ, 1%, 0603		

Recommended Components Table for Typical Applications

V_{OUT}(V)	R_{MODE}(kΩ)	Frequency (kHz)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/(Rated/Saturating Current)	C_{OUT}
1.2	0	600, FCCM	100	100	220	0.22μH/(28A/30A)	47μF×5/10V/X7R,1206
1.8	0	600, FCCM	100	49.9	220	0.22μH/(28A/30A)	47μF×5/10V/X7R,1206
3.3	30	800, FCCM	100	22.1	220	0.47μH/(28A/30A)	47μF×5/10V/X7R,1206
5	30	800, FCCM	100	13.7	220	0.47μH/(28A/30A)	47μF×5/10V/X7R,1206

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation.

- Place the major MLCC capacitors (C_{IN}, C_{OUT}) on the same layer as the device.
- Place the input capacitors as close as possible to the IN and GND pins, minimizing the loop formed by these connections. To reduce parasitic inductance, avoid using direct vias in the power trace between the input capacitors and IN, PGND.
- Place one smaller package input MLCC capacitor at the reach-out port of Pin 18. This capacitor can be connected with GND by vias.
- Place the V_{CC} capacitor close to V_{CC} using short, direct connections instead of vias.
- Use a single Kelvin connection between AGND and GND at the C_{VCC} ground point.
- Place the feedback components (R1, R2, R_{FF}, and C_{FF}) as close to the FBS pin as possible. Avoid routing the remote output-sense line and remote GND-sense (GNDS) line near LX, BS, or other high-frequency traces as they are noise-sensitive.
- Connect the feedback resistor directly to COUT rather than the inductor output terminal.
- Guarantee the C_{OUT} negative sides are connected to the GND pin by wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.
- The LX connection has large voltage swings and fast edges and can easily radiate noise to adjacent components. Keep its area small to prevent excessive EMI, while providing wide copper traces to minimize parasitic resistance and inductance. Keep sensitive components away from the switching node or provide ground traces between them for shielding, to prevent stray capacitive noise pickup.
- Place the BS capacitor on the same layer as the device; keep the BS voltage path (BS, LX, and C_{BS}) as short as possible.
- It is not recommended to connect control signals and IN directly. A resistor in the range of 1kΩ to 1MΩ should be used if they are pulled high by IN.
- Provide dedicated wide copper traces for the power-path ground between the IC and the input and output capacitor grounds, rather than connecting each of these individually to an internal ground plane.
- Connect the exposed GND pad to a large copper area and place several GND vias on it for heat sinking and noise minimization.
- A four-layer layout is strongly recommended to achieve better thermal performance. For example, an 8.5cm × 8.5cm four-layer PCB with 2oz copper.
- Keep the high current traces (IN, GND, LX, and OUT traces) as short and wide as possible.
- Utilize the top layer and bottom layers for power IN and GND, making the copper plane as wide as possible. Dedicate one middle layer to GND for conducting heat and shielding the other middle layer signal lines from top-layer crosstalk.

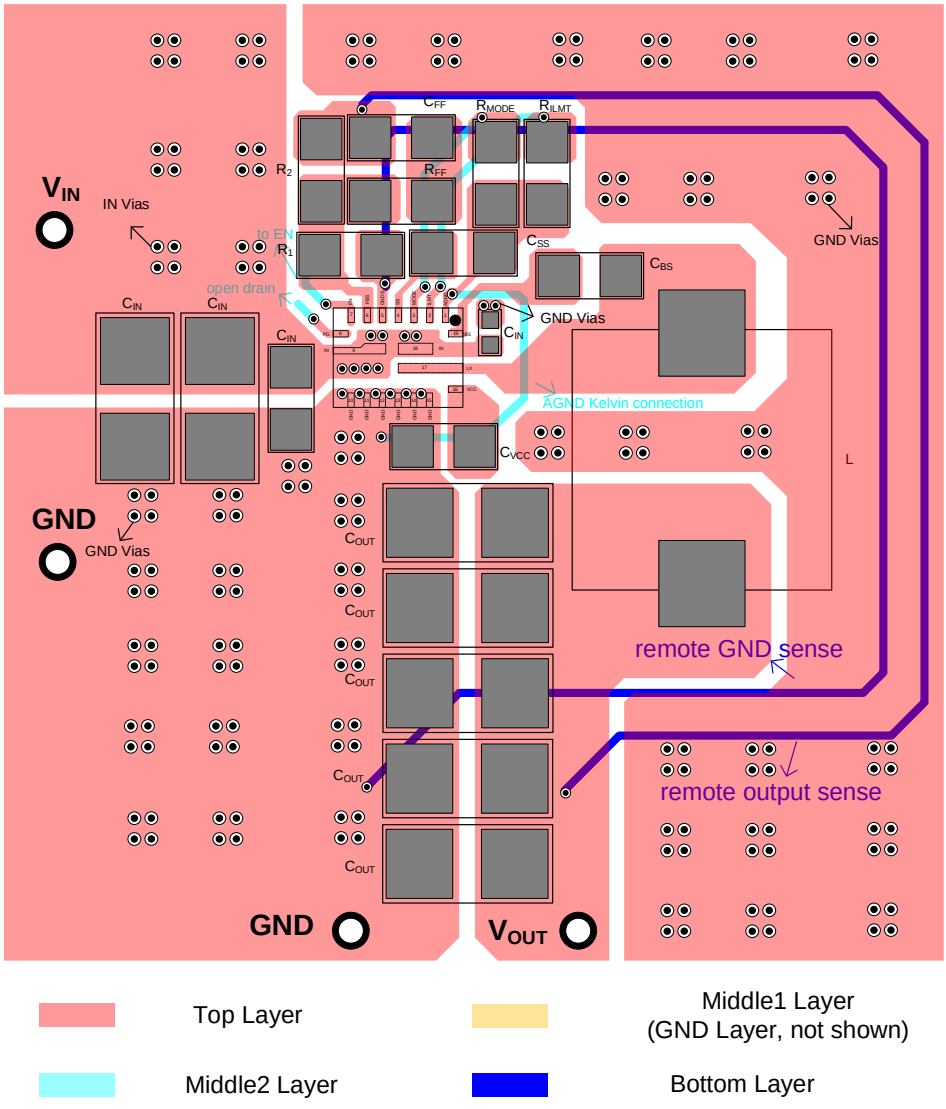
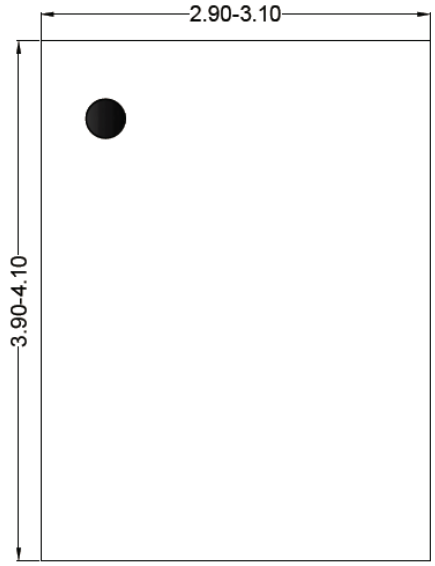
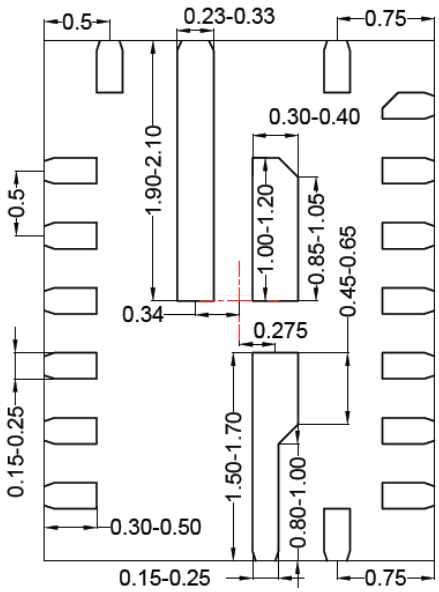


Figure 14. Suggested PCB Layout

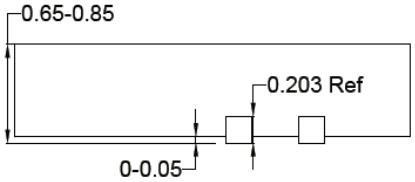
QFN3×4-19 Package Outline Drawing



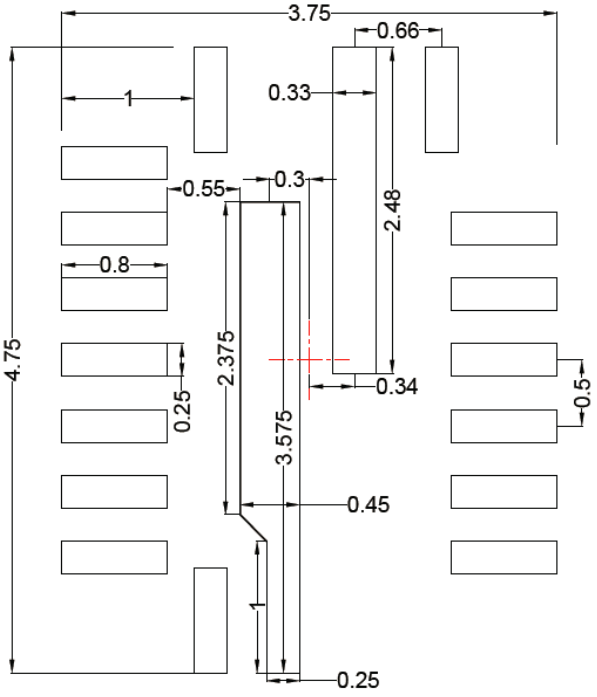
Top view



Bottom view



Front view

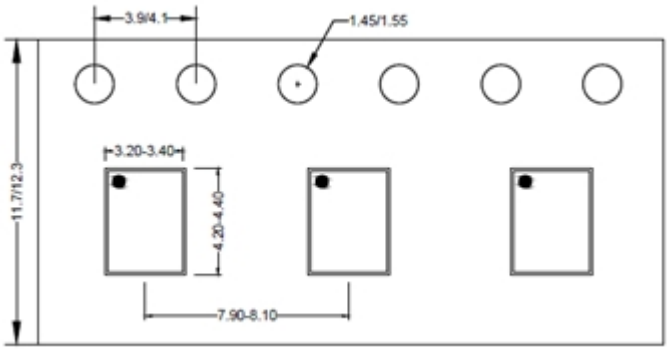


Recommended PCB layout (reference only)

Note: All dimensions are in millimeters and exclude mold flash and metal burr. Center line refers to chip body center.

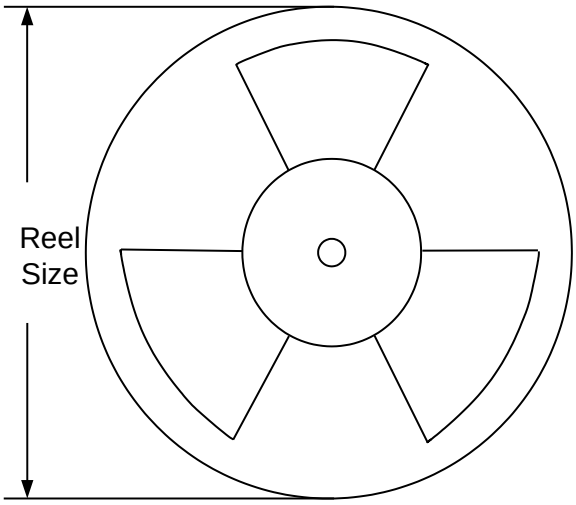
Taping and Reel Specification

Package orientation



Feeding direction ⟶

Carrier tape and reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length (mm)	Leader length (mm)	Qty per reel
QFN3×4	12	8	13"	400	400	5000

Revision History

Revision Number	Revision Date	Description	Pages changed
1.0	10/9/2023	Production Release	
0.9	12/27/2021	Initial Release	-

Revision history is for reference only and may not be comprehensive or complete.

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