SY21249C1

High-Efficiency Fast-Response, 11A, 24V Input Synchronous Step-Down Regulator

General Description

The SY21249C1 high-efficiency synchronous step-down DC/DC regulator is capable of delivering 11A current over a wide input voltage range of 5.5V to 24V. To minimize conduction loss, it integrates a main switch and a synchronous switch with very low $R_{DS(ON)}$. It operates at a pseudoconstant frequency of 600kHz under heavy load conditions to minimize inductor and capacitor sizes.

The SY21249C1 also provides a fixed 5V LDO with 100mA current capability, which can be used to power external peripherals. Under light load conditions, the LDO can be switched over to the buck regulator output to reduce power loss.

Silergy's constant on-time (COT) ripple-based control strategy supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near-constant operating frequency over line, load, and output voltage ranges. This control method provides stable operation without complex compensation, even with low-ESR ceramic capacitors.

The SY21249C1 offers protection against multiple conditions, including cycle-by-cycle current limit, input undervoltage lockout, output undervoltage and overvoltage protection, internal soft-start, and thermal shutdown.

The SY21249C1 is available in a compact QFN3mm×4mm-13 package.

Features

- 5.5–24V Input Voltage Range
- Up to 11A Output Current
  100mA LDO Current
- Low $R_{DS(ON)}$ for Internal Switches: 17mΩ Top, 7.5mΩ Bottom
- Integrated 1.5Ω Bypass Switch
- COT Ripple-Based Control to Achieve Fast Transient Responses
- Soft-Start Inrush Current Limit
- Pseudoconstant Frequency: 600kHz
- Fixed 5.15V Output Voltage
- ±1.5% Internal Reference Voltage
- PFM/Ultrasonic (USM) Selectable Light-Load Operation Mode
- Power-Good Indicator
- Output-Discharge Function
- Cycle-by-Cycle Valley/Peak Current Limit
- Buck Protection: Latch-Off Mode Output Undervoltage (UVP), Overvoltage (OVP) and Overtemperature (OTP)
- LDO Protection: Auto-Recovery Mode, Output Undervoltage and Overtemperature
- Input Undervoltage (UVLO)
- RoHS-Compliant and Halogen-Free
- Compact Package: QFN3mm×4mm-13

Applications

- LCD TV/3DTV
- Set-Top Box
- Notebook
- High-Power AP

Typical Application

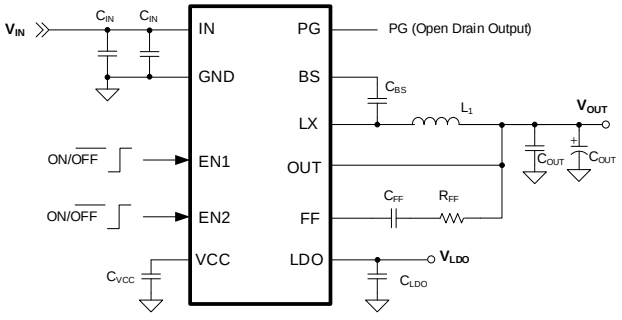


Figure 1. Typical Application Circuit

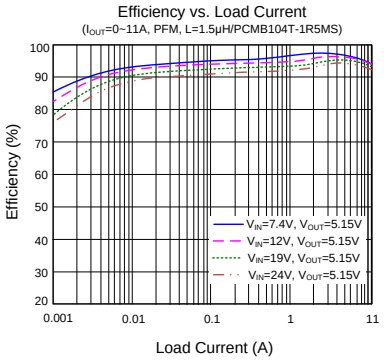


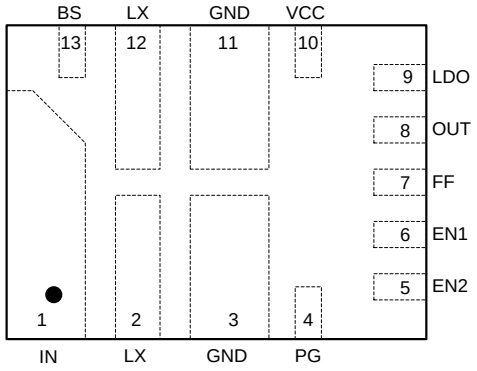
Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY21249C1TMC	QFN3mm×4mm-13 RoHS-Compliant and Halogen-Free	**DTRxyz**

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	IN	Input pin. Decouple this pin to the GND pin with at least a 20µF ceramic capacitor. A 0.1µF input ceramic capacitor is recommended to reduce input noise.
2, 12	LX	Inductor pin. Connect this pin to the switching node of the inductor.
3, 11	GND	Ground pin.
4	PG	Power-good indicator. Open-drain output when the output voltage is within 90% to 120% of the regulation point.
5	EN2	Enable control of the IC and internal LDO. Pull this pin high to turn on the IC and the internal LDO. Do not leave this pin floating.
6	EN1	Enable control of the DC/DC regulator. Pull this pin high to turn on the regulator. Do not leave this pin floating. This pin is also used for controlling the operating mode of the regulator under light-load condition when the output of the buck regulator is within the regulation range. When its voltage is less than 1.6V, the buck regulator operates in ultrasonic mode. When its voltage is larger than 2.2V, the buck regulator operates in PFM mode.
7	FF	Output feed-forward pin. Connect the RC network from the output to this pin.
8	OUT	Output pin. Connect to the output of the buck regulator. The pin also provides the bypass input for the internal LDO.
9	LDO	5V LDO output. Decouple this pin to ground with a 4.7µF ceramic capacitor.
10	V_{CC}	Internal 3.6V LDO output. Power supply for internal analog circuits and driving. Decouple this pin to ground with a 2.2µF ceramic capacitor.

Block Diagram

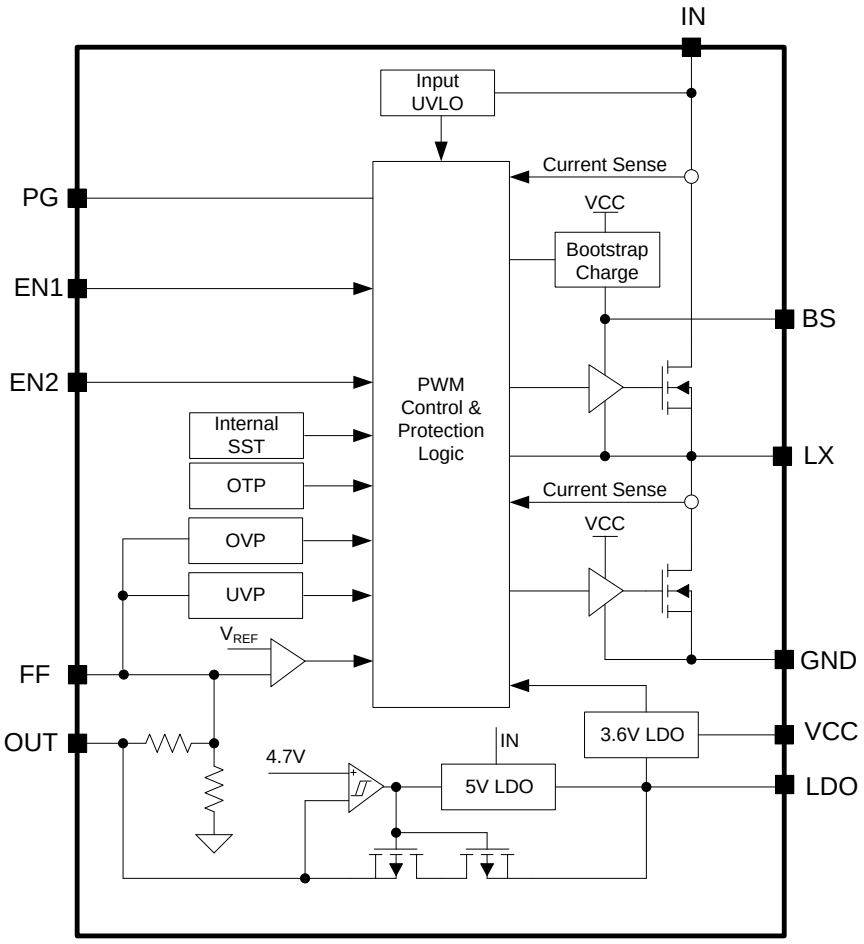


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	26	V
IN-LX, LX, PG, EN2, EN1	-0.3	IN+0.3	
BS-LX, V_{CC}, FF	-0.3	4	
OUT, LDO	-0.3	6.5	
Dynamic LX Voltage in 10ns Duration (3)	GND-5	IN+3	
Dynamic LX Voltage in 20ns Duration (3)	GND-1	IN+2	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10sec.)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	27	°C/W
θ_{JC} Junction-to-case Thermal Resistance	4.3	
P_D Power Dissipation T_A = 25°C	3.7	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	5.5	24	V
Junction Temperature, Operating	-40	125	
Ambient Temperature	-40	85	°C

Electrical Characteristics

(V_{IN} = 12V, C_{OUT} = 88μF, TA = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage Range	V_{IN}		5.5		24	V
	UVLO Threshold	V_{UVLO}	V_{IN} rising			5	V
	UVLO Hysteresis	V_{HYS}			0.5		V
	Quiescent Current	I_Q	I_{OUT} = 0A, V_{OUT} = V_{SET} × 105%		110	140	μA
	Shutdown Current 1	I_{SHDN1}	EN1 = 0, EN2 = 1		65	90	μA
	Shutdown Current 2	I_{SHDN2}	EN1 = 0, EN2 = 0		4.5	9	μA
Output	Voltage Setpoint	V_{SET}	CCM	5.07	5.15	5.23	V
	Discharge Current	I_{DIS}	V_{OUT} = 5.15V		100		mA
	Soft-Start Time	t_{SS}	V_{OUT} from 0% to 100% V_{SET}		0.8		ms
	OVP Threshold	V_{OVP}	V_{FF} rising	115	120	125	% V_{REF}
	OVP Hysteresis	$V_{OVP,HYS}$			5		% V_{REF}
	OVP Delay	$t_{OVP,DLY}$	(Note4)	30	40		μs
	UVP Threshold	V_{UVP}		55	60	65	% V_{REF}
	UVP Delay	$t_{UVP,DLY}$	(Note4)		200		μs
MOSFET	Top FET $R_{DS(ON)}$	$R_{DS(ON)1}$			17		mΩ
	Bottom FET $R_{DS(ON)}$	$R_{DS(ON)2}$			7.5		mΩ
	Top FET Current Limit	$I_{LMT,TOP}$			22		A
	Bottom FET Current Limit	$I_{LMT,BOT}$		14			A
	Bottom FET Reverse-Current Limit	$I_{LMT,RVS}$	USM	4	6.5		A
Enable (EN)	Input Voltage High	$V_{EN,H}$		1			V
	Input Voltage Low	$V_{EN,L}$				0.4	V
	EN1 Voltage for Ultrasonic Mode	$V_{EN1,USM}$		1		1.6	V
	EN1 Voltage for PFM Mode	$V_{EN1,PFM}$		2.2		V_{IN}	V
Frequency	Switching Frequency	f_{SW}	CCM	510	600	690	kHz
	Ultrasonic Mode Frequency	f_{USM}	USM mode, I_{OUT} = 0A		27		kHz
	Min ON Time	$t_{ON,MIN}$	V_{IN} = $V_{IN,MAX}$		50		ns
	Min OFF Time	$t_{OFF,MIN}$			150		ns
Power-Good	Falling Threshold	V_{PG}	V_{FF} falling (not good)	80	83	86	% V_{REF}
	Threshold Hysteresis	$V_{PG,HYS}$	V_{FF} rising (good)		7		% V_{REF}
	Delay Time	$t_{PG,R}$	Low to high (Note4)		200		μs
		$t_{PG,F}$	High to low (Note4)		40		μs
	Low Voltage	$V_{PG,LOW}$	V_{FF} = 0V, I_{PG} = 5mA			0.45	V
	Leakage Current	$I_{PG,LKG}$	PG connects 3.6V			5	μA
LDO	Output Voltage	V_{LDO}	BYP off, I_{LDO} = 0mA	4.9	5	5.15	V
	Dropout Voltage	$V_{DROPOUT}$	I_{LDO} = 100mA		300		mV
	Output Current Limit	$I_{LMT,LDO}$		150		310	mA

Electrical Characteristics (cont.)

(V_{IN} = 12V, C_{OUT} = 88µF, TA = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
V_{CC}	Output Voltage	V_{CC}	V_{CC} adds 1mA load	3.45	3.6	3.75	V
BYP	$R_{DS(ON)}$	$R_{DS(ON),BYP}$			1.5		Ω
	Turn-On Voltage	V_{BYP}		4.5	4.7	4.9	V
	Turn-On Hysteresis	$V_{BYP, HYS}$			0.2		V
	OVP Voltage	$V_{BYP, OVP}$	V_{OUT} sweeps	114	120	126	% V_{LDO}
OTP	Buck Temperature	$T_{OTP,BUCK}$	T_J rising (Note4)		150		°C
	Buck Temperature Hysteresis	$T_{BUCK,HYS}$	T_J falling (Note4)		15		°C
	LDO Temperature	$T_{OTP,LDO}$	(Note4)		160		°C
	LDO Temperature Hysteresis	$T_{LDO,HYS}$	(Note4)		25		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: Package thermal resistance is measured in the natural convection at T_A = 25°C on an 8.5cm × 8.5cm four-layer Silergy Evaluation Board with 2oz copper.

Note 3: The device is not guaranteed to function outside its operating conditions.

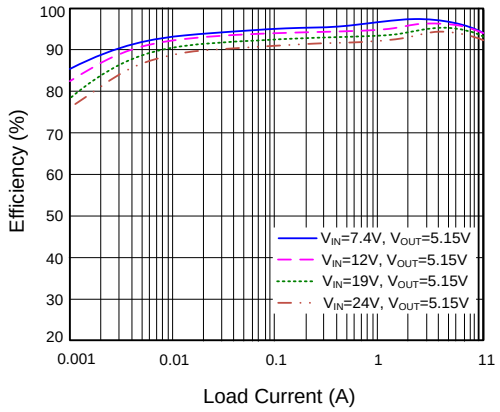
Note 4：Guaranteed by design.

Typical Performance Characteristics

(T_A = 25°C, V_{IN} = 12V, V_{OUT} = 3.3V, L = 1.5µH, C_{OUT} = 66µF, unless otherwise noted)

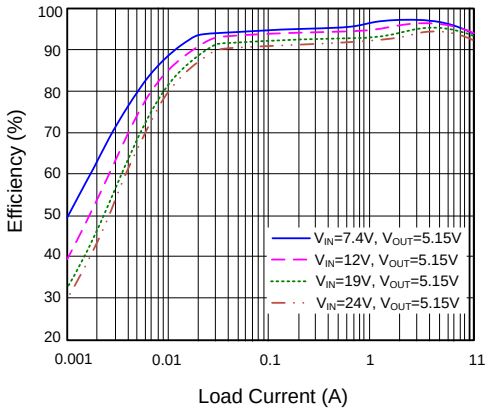
Efficiency vs. Load Current

(I_{OUT}=0~11A, PFM, L=1.5µH/PCMB104T-1R5MS)



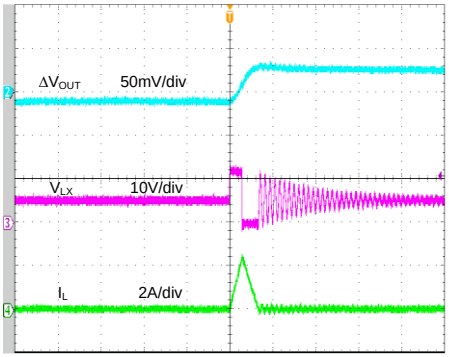
Efficiency vs. Load Current

(I_{OUT}=0~11A, USM, L=1.5µH/PCMB104T-1R5MS)



Output Ripple

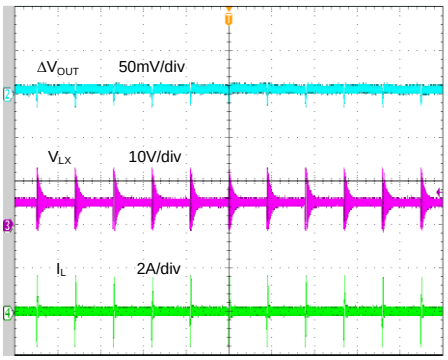
(V_{IN}=12V, V_{OUT}=5.15V, I_{OUT}=0A, PFM)



Time (2µs/div)

Output Ripple

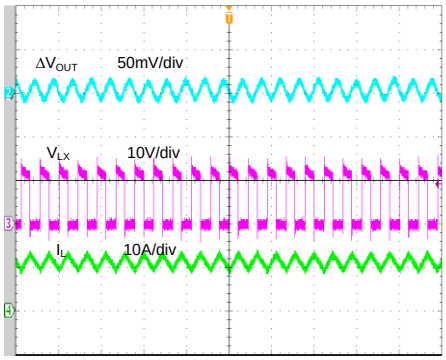
(V_{IN}=12V, V_{OUT}=5.15V, I_{OUT}=0A, USM)



Time (40µs/div)

Output Ripple

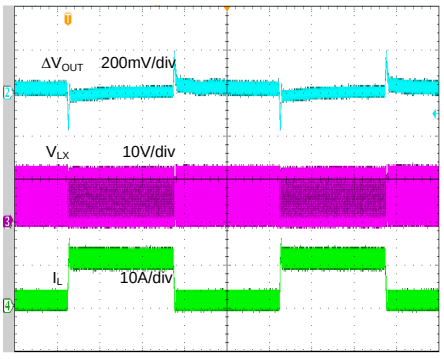
(V_{IN}=12V, V_{OUT}=5.15V, I_{OUT}=11A)



Time (4µs/div)

Load Transient

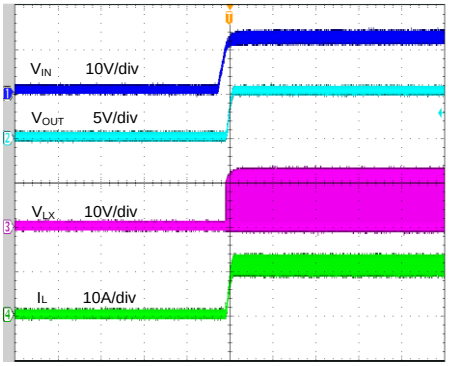
(V_{IN}=12V, V_{OUT}=5.15V, I_{OUT}=1.1~11A, PFM)



Time (200µs/div)

Startup from V_{IN}

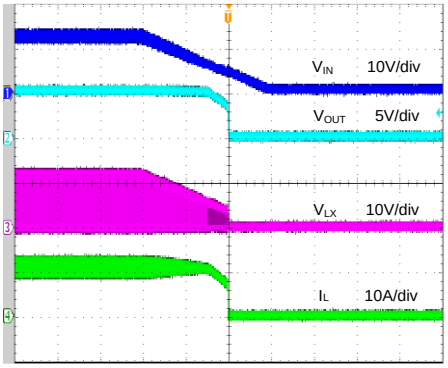
(V_{IN}=12V, V_{OUT}=5.15V, I_{OUT}=11A)



Time (4ms/div)

Shutdown from V_{IN}

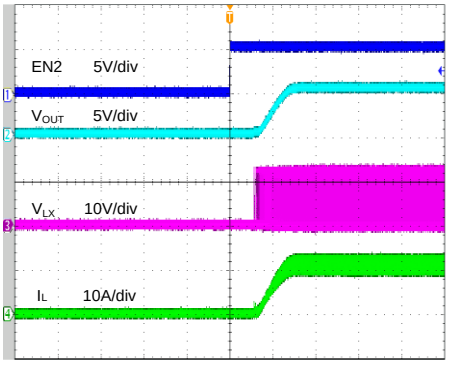
(V_{IN}=12V, V_{OUT}=5.15V, I_{OUT}=11A)



Time (4ms/div)

Startup from EN2

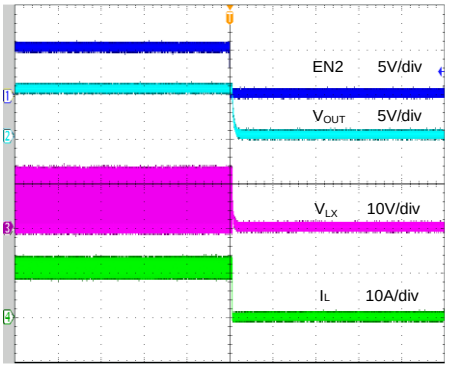
(V_{IN}=12V, V_{OUT}=5.15V, I_{OUT}=11A)



Time (800µs/div)

Shutdown from EN2

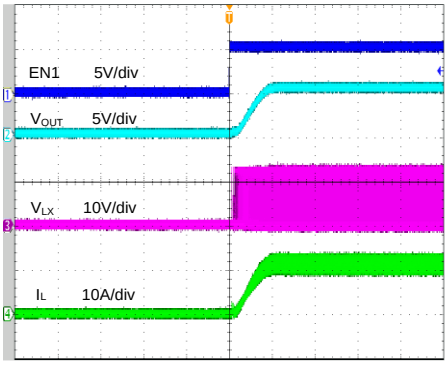
(V_{IN}=12V, V_{OUT}=5.15V, I_{OUT}=11A)



Time (800µs/div)

Startup from EN1

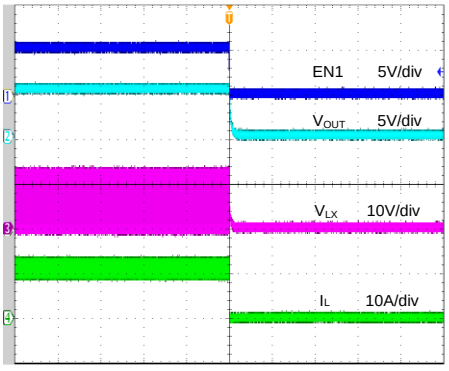
(V_{IN}=12V, V_{OUT}=5.15V, I_{OUT}=11A)



Time (800µs/div)

Shutdown from EN1

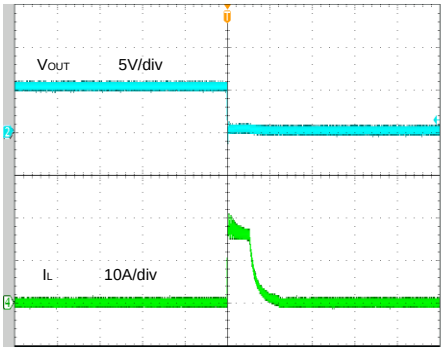
(V_{IN}=12V, V_{OUT}=5.15V, I_{OUT}=11A)



Time (800µs/div)

Short Circuit Protection

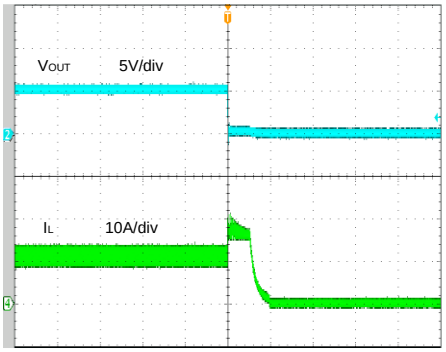
(V_{IN}=12V, V_{OUT}=5.15V, I_{OUT}=0A~Short)



Time (400µs/div)

Short Circuit Protection

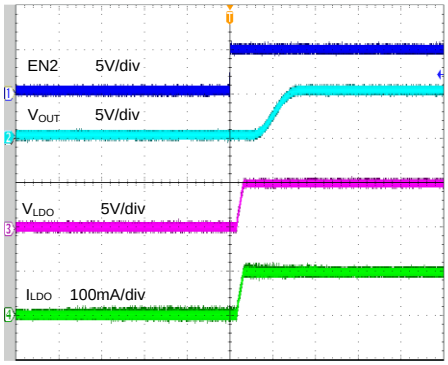
(V_{IN}=12V, V_{OUT}=5.15V, I_{OUT}=11A~Short)



Time (400µs/div)

LDO Startup from EN2

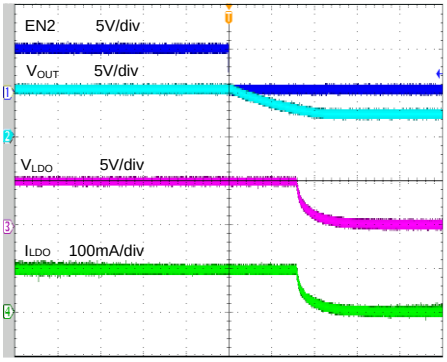
(V_{IN}=12V, V_{OUT}=5.15V, I_{OUT}=11A, I_{LDO}=100mA, EN1=1)



Time (800µs/div)

LDO Shutdown from EN2

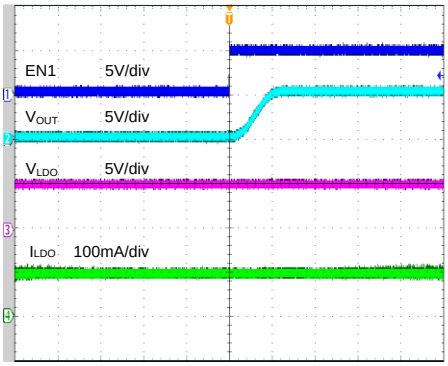
(V_{IN}=12V, V_{OUT}=5.15V, I_{OUT}=11A, I_{LDO}=100mA, EN1=1)



Time (800µs/div)

LDO Switchover when EN1 ON

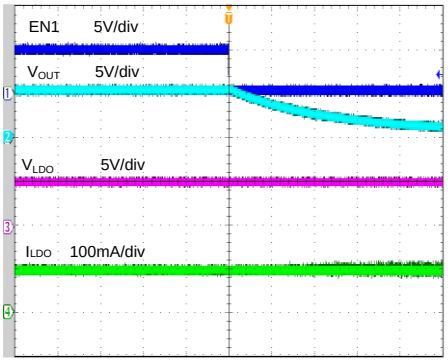
(V_{IN}=12V, V_{OUT}=5.15V, I_{OUT}=11A, I_{LDO}=100mA, EN2=1)



Time (800µs/div)

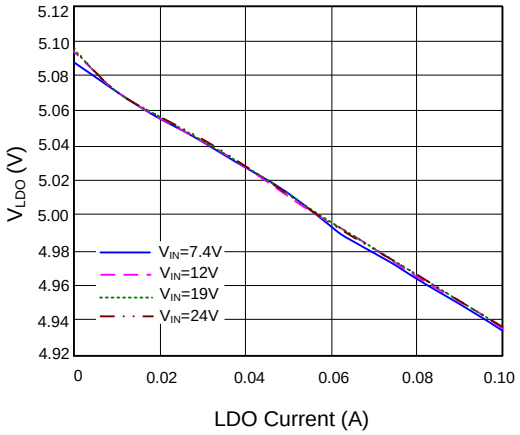
LDO Switchover when EN1 OFF

(V_{IN}=12V, V_{OUT}=5.15V, I_{OUT}=11A, I_{LDO}=100mA, EN2=1)

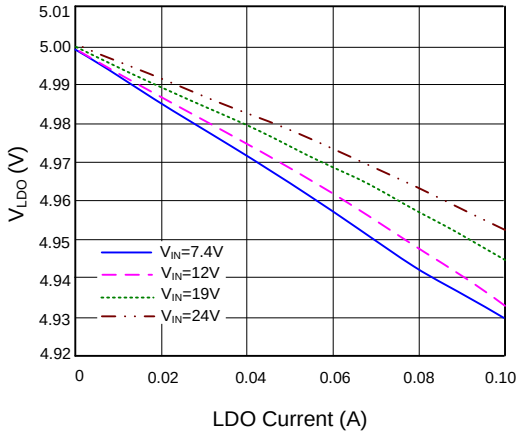


Time (800µs/div)

LDO Load Regulation(BYP ON)

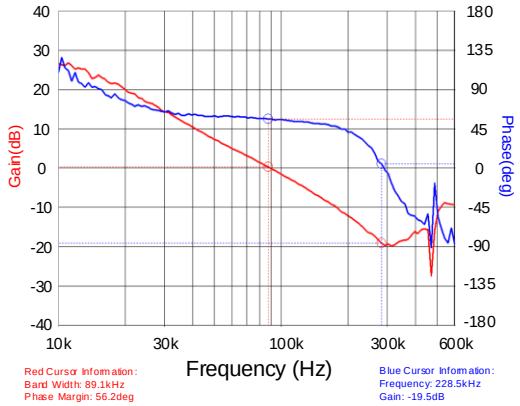


LDO Load Regulation (BYP OFF)



Bode Plot

(V_{IN}=20V, V_{OUT}=5.15V, I_{OUT}=5.5A)



Detailed Description

General Features

Constant-On-Time Architecture

The one-shot circuit or on-time generator, which determines how long to turn on the high-side power switch, is fundamental to any constant-on-time (COT) architecture. Each on-time (t_{ON}) is a fixed period internally calculated to operate the step-down regulator at the desired switching frequency, considering the input and output voltage ratio, $t_{ON} = (V_{OUT}/V_{IN}) \times (1/f_{SW})$. For example, considering that a hypothetical converter targets 5.15V output from a 12V input at 600kHz, the target on-time is (5.15V/12V) × (1/600kHz) = 715.28ns. Each t_{ON} pulse is triggered by the feedback comparator when the output voltage as measured at FF drops below the target value. After one t_{ON} period, a minimum off-time ($t_{OFF,MIN}$) is imposed before any further switching is initiated, even if the output voltage is less than the target. This approach avoids making any switching decisions during the noisy periods immediately after switching events, or while the switching node (LX) is rapidly rising or falling.

There is no fixed clock in a COT architecture, so the high-side power switch can turn on almost immediately after a load transient. Subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays. Conventional current-mode or voltage-mode control methods determine when to turn off the high-side power switch and turn on the low-side synchronous rectifier based on current feedback, feedback voltage, internal ramps, and internal compensation signals, so these must all be monitored. These signals are difficult to observe immediately after switching large currents, however, which makes such architectures difficult to implement in noisy environments and at low duty cycles.

Minimum Duty Cycle and Maximum Duty Cycle

There is no limitation for minimum duty cycle in COT architecture. This is because when the on-time is close to the minimum on-time, the switching frequency can be reduced as needed to always ensure proper operation.

The SY21249C1 can support 5.15V fixed output when TJ = -40–125°C, even if the input voltage is as low as 5.5V. To accomplish this, t_{ON} can be stretched to extend the duty cycle as much as necessary. When the device detects that feedback voltage is lower than the reference voltage under normal on-time operation, t_{ON} will be stretched. The maximum limitation of t_{ON} is 3–4 normal switching cycles. The on-time stretch function is disabled when the feedback voltage is less than the undervoltage protection (UVP) threshold.

Instant-PWM Operation

Silergy's instant-PWM control method adds several proprietary improvements to the traditional COT architecture. First, whereas most legacy COT implementations require a dedicated connection to the output voltage terminal to calculate the t_{ON} duration, the instant-PWM control method derives this signal internally.

Additionally, it optimizes operation with low-ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT regulators may become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor may become too small to maintain stable operation. For this reason, instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the t_{ON} pulse is triggered as long as the minimum t_{OFF} has been satisfied and the inductor current as measured in the low-side synchronous rectifier is lower than the bottom FET current limit. When the t_{ON} pulse is triggered, the low-side synchronous rectifier turns off and the high-side power switch turns on. The inductor current then ramps up linearly during the t_{ON} period. At the end of the t_{ON} period, the high-side power switch turns off, the low-side synchronous rectifier turns on, and the inductor current ramps down linearly.

This action also initiates the minimum t_{OFF} timer to ensure sufficient time for stabilizing any transient conditions and settling the feedback comparator before the next cycle is initiated. This minimum t_{OFF} is relatively short so that transient t_{ON} can be retriggered with minimal delay during high-speed load, allowing the inductor current to ramp quickly and provide sufficient energy to the load side.

In order to avoid shoot-through, a dead time (t_{DEAD}) is generated internally between the time when the high-side power switch turns off and the low-side synchronous rectifier on-period, or between the time when the low-side synchronous rectifier turns off and the high-side power switch on-period.

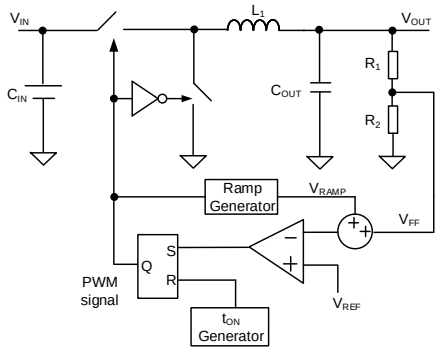


Figure 4. Instant-PWM

Light-Load Operation Mode Selection

PFM or USM light load operation is selected using the EN1pin. EN1is not only used as an enable pin, but also for mode selection to control the operation of the regulator under light-load conditions, after the output is within the regulation range. When the voltage on this pin is lower than 1.6V and higher than its rising threshold, the regulator operates in ultrasonic mode (USM). If the voltage on this pin is greater than 2.2V, the buck regulator operates in pulse-frequency modulation mode (PFM).

If PFM light-load operation is selected, under light load conditions (typically when $I_{OUT} < 0.5 \times \Delta I_L$), the current through the low-side synchronous rectifier will decrease to near zero before the next t_{ON} time. When this occurs, the low-side synchronous rectifier turns off, preventing recirculation current that can seriously reduce efficiency under light-load conditions. As the load current is further reduced and the combined feedback and ramp signals remain much greater than the reference voltage, the instant-PWM control loop will not trigger another t_{ON} until needed. The apparent operating switching frequency will drop accordingly, further enhancing efficiency. The switching frequency can be in the audible range under deep light-load or no-load conditions. Continuous conduction mode (CCM) resumes smoothly as soon as the load current increases sufficiently for the inductor current to remain above zero at the time of the next t_{ON} cycle. The device enters CCM once the load current exceeds this threshold. Above this level, the switching frequency stays fairly constant over the entire output current range. The transition level of the load current is determined as follows:

$$I_{OUT\_CTL} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \times (1-D)}{2 \times f_{SW} \times L_1}$$

If USM light-load operation is selected, the control loop keeps the switching frequency above the audible frequency range, even under light-load or no-load conditions. Once the device detects that both the high-side power switch and the low-side synchronous rectifier turn off for more than a specified duration, it forces the low-side synchronous rectifier to turn on in advance of one t_{ON} cycle and discharge the output capacitor in order to keep the switching frequency out of audio range. A separate control loop is used to force the low-side synchronous rectifier on to prevent the output voltage from becoming too high.

Input Undervoltage Lockout (UVLO)

To prevent operation before all internal circuitry is ready, and to ensure that the power and synchronous rectifier switches can operate normally, instant-PWM incorporates an input undervoltage lockout protection. The SY21249C1 remains in a low-current state and all switching actions are inhibited until V_{IN} exceeds the UVLO (rising) threshold. At this time, if EN is enabled, the device will start up by initiating a soft-start ramp. If V_{IN} falls below V_{UVLO} by more than the input UVLO hysteresis, switching actions and LDO operation will again be suppressed.

If the input UVLO threshold is too low for some high-input UVLO threshold requirement applications, an external resistor-divider connected to EN2 can be used to adjust UVLO threshold.

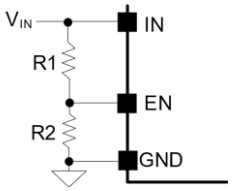


Figure 5. UVLO adjustment

EN1/EN2 Control

The SY21249C1 has two enable pins to control the synchronous buck regulator and LDO. The LDO is only enabled when EN2 is high, and the buck regulator is only enabled when both EN1 and EN2 are high. See Table 1.

Table 1. EN1/EN2 Control

EN2	EN1	STATE	LDO	BUCK
High	High	S0	On	On
High	Low	S3	On	Off
Low	Low/High	S4/S5	Off	Off

The EN1/EN2 inputs are high-voltage-capable inputs with logic-compatible threshold. When EN1/EN2 are driven above 1V, normal device operation is enabled. When driven below 0.4V, the device will be shut down, reducing the input current to < 10μA.

It is not recommended to connect EN2/EN1 to the IN pin directly. A resistor with a value between 1kΩ and 1MΩ should be used to pull these pins up to IN.

Startup and Shutdown

The SY21249C1 incorporates an internal soft-start circuit to smoothly ramp the output to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows the output to rise to the target voltage over approximately 1.2ms, which avoids high current flow during startup. The startup and shutdown sequences are shown in Figure 6.

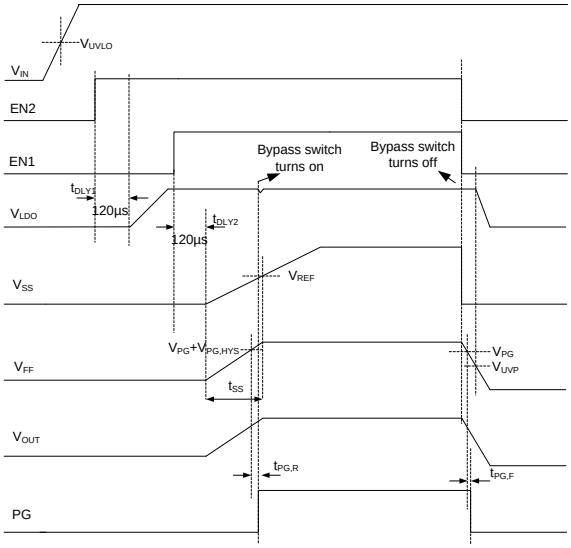


Figure 6. Startup and shutdown sequence

When the input voltage exceeds its the UVLO (rising) threshold, the LDO is turned on after EN2 is enabled for one delay time t_{DLY1}. The buck regulator is turned on if EN1 is also enabled for one delay time t_{DLY2}. When the output voltage is 90% of the regulation point, PG becomes high-impedance after one delay time $t_{PG,R}$, and the LDO output switches over to the buck output if OUT voltage is higher than the bypass switch turn-on voltage. The LDO output will switch over to the internal LDO regulator once either EN1 or EN2 is disabled.

If the output is pre-biased to a certain voltage before startup, the device disables the switching of both the high-side power switch and the low-side synchronous rectifier until the voltage on the internal soft-start circuit voltage V_{SS} exceeds the sensed output voltage at the FB node.

Output Discharge

The SY21249C1 discharges the output voltage when the converter shuts down from V_{IN} UVLO, using EN/EN2 to disable operation, or due to thermal shutdown, so that the output voltage can be discharged in a minimal amount of time, even if the output load current is zero. The discharge FET in parallel with the low-side synchronous rectifier turns on after the low-side synchronous rectifier turns off when shutdown logic is triggered. The output discharge current is typically 100mA when LX voltage is 5V. Note that the discharge FET is not active outside of the shutdown conditions.

Buck Output Power-Good Indicator

The buck power-good indicator is an open-drain output controlled by a window comparator connected to the feedback signal. If V_{FF} is greater than V_{PG} + $V_{PG,HYS}$ and less than V_{OVP} for at least the power-good delay time (low to high), PG will be high-impedance.

PG should be connected to V_{IN} or another voltage source through a resistor (e.g., 100kΩ). After the input voltage exceeds the UVLO (rising) threshold, the PG MOSFET is turned on so that PG is pulled to GND before the output voltage is ready. After the feedback voltage V_{FF} reaches V_{PG} + $V_{PG,HYS}$, PG is pulled high (after one delay time, typical 200μs). When V_{FF} drops to V_{PG}, or rises to V_{OVP} for one OVP delay time, PG is pulled low (after a delay, typical 40μs).

External Bootstrap Capacitor Connection

The SY21249C1 integrates a floating power supply for the gate driver that operates the high-side power switch. Proper operation requires a 0.1μF low-ESR ceramic capacitor to be connected between BS and LX, which provides the gate-driver supply voltage for the high-side N-channel MOSFET power switch.

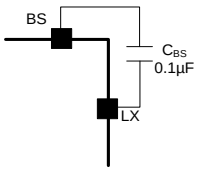


Figure 7. Bootstrap capacitor connection

V_{CC} Linear Regulator

An internal linear regulator (V_{CC}) produces a 3.6V supply from V_{IN} that powers the internal gate drivers, PWM logic, analog circuitry, and other blocks. V_{CC} is supplied by the LDO. Connect a 2.2µF low-ESR ceramic capacitor from V_{CC} to GND as shown in Figure 8. Make sure the loop formed by the V_{CC} capacitor is shorter than the LDO output capacitor loop, if there is a placement conflict between them.

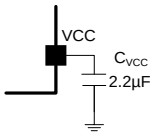


Figure 8. V_{CC} regulator

Fault Protection Modes

Output Current Limit

Instant-PWM architecture incorporates a cycle-by-cycle "valley" current limit. The inductor current is measured in the low-side synchronous rectifier when it turns on and as the inductor current ramps down. If the current exceeds the current-limit threshold, t_{ON} is inhibited until the current returns to a level at or below the limit threshold, as shown in Figure 9.

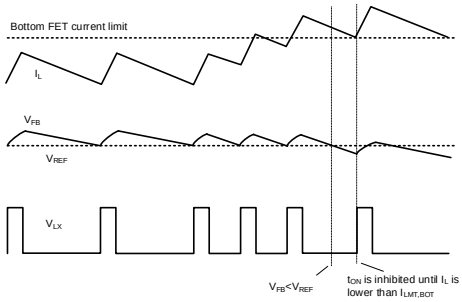


Figure 9. Output current limit

When the valley current-limit is reached, the output current-limit value is given by the following equations:

$$I_{LMT,OUT} = I_{LMT,BOT} + \Delta I_L/2,$$

where ΔL is derived as follows:

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

The overcurrent limit protection (OCP) limits the inductor current. When the load current is higher than the bottom FET current limit threshold by one half of the peak-to-peak inductor ripple current, the output voltage starts to drop. When the feedback voltage falls lower than the undervoltage protection threshold (UVP) and continues for one UVP delay time, the device will latch off. Overtemperature protection may also be triggered under an overcurrent condition, and the device will OTP latch off.

The SY21249C1 also incorporates a cycle-by-cycle "peak" current limit (top FET current limit). The high-side power-switch current is monitored during t_{ON} time. If the monitored current exceeds the threshold, the high-side power switch is turned off, the low-side synchronous rectifier is turned on, and t_{ON} is inhibited. t_{ON} is no longer inhibited once low-side synchronous-rectifier current is lower than the bottom-FET current-limit value.

Output Undervoltage Protection (UVP)

If V_{OUT} is less than approximately 60% of the setpoint for approximately 200µs when the output short circuits or the load current is much higher than the maximum current capacity, the output undervoltage protection (UVP) will be triggered, and the device will latch off. Cycle EN1 or EN2 to re-enable the device. See Figure 10 for details.

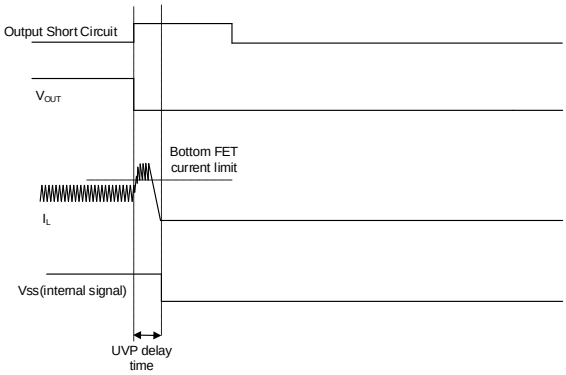


Figure 10. Output undervoltage protection

Output Overvoltage Protection (OVP)

If the output voltage rises above the feedback regulation level, the high-side power switch naturally remains off, and the protection is activated depending on the operation mode.

When operating in PFM light-load mode, if the feedback voltage remains high, the low-side synchronous rectifier remains on until the inductor current reaches zero and the switching actions are suppressed. The switching actions are resumed once the combined feedback and ramp signals are lower than the reference voltage.

When operating in USM light-load mode, if the feedback voltage remains high, the reverse-current limit will be triggered, and the inductor current average value becomes negative as the device attempts to lower the output voltage. If the feedback voltage continues to rise and exceeds the output overvoltage threshold for more than the OVP delay time, and the output voltage exceeds the bypass switch OVP voltage, the output overvoltage protection (OVP) will be triggered, and the device will latch off. Cycle EN2 or EN1 to re-enable the device. False OVP may happen under a USM light-load condition if the chosen inductance is too small, and the reverse-current limit is triggered.

Buck Overtemperature Protection (OTP)

Instant-PWM includes overtemperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The device will latch off when the junction temperature exceeds 150°C, but LDO output voltage will still be active. Cycle EN1 or EN2 to re-enable the device after the junction temperature cools by 15°C.

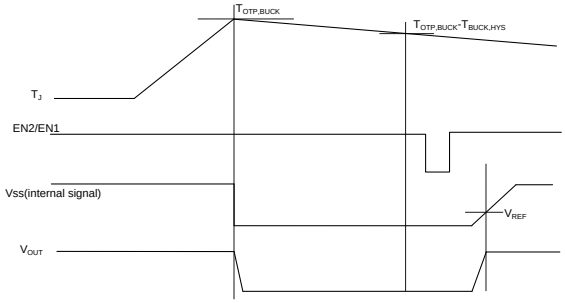


Figure 11. Overtemperature protection

LDO Overtemperature Protection (OTP)

The SY21249C1 also features LDO overtemperature protection with auto-recovery to guarantee safe LDO operation in the presence of internal LDO regulator power loss. When the LDO thermal sensor detects that the LDO junction temperature exceeds 160°C, the LDO and buck converter will be turned off. When the LDO junction temperature cools down by approximately 25°C, the LDO will return to normal operation. To enable the buck converter after OTP, EN2 must be cycled.

Application Information

Input Capacitor Selection

Input filter capacitors reduce the ripple voltage on the input, filter the switched current drawn from the input supply, and reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating higher than the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge-current capability, and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases. Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. Two 10µF X5R capacitors are sufficient for most applications. Locate the ceramic input capacitor as close as possible to the device IN and GND pins.

Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage.

Instant-PWM operates well over a wide range of inductor values. This flexibility allows for optimization to find the best trade-off of efficiency, cost, and size for a particular application. Selecting a low inductor value will help reduce size and cost, and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low-value inductors may help reduce DC losses and increase efficiency. On the other hand, higher inductor values tend to have higher DCR and will slow transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current (ΔI_L) approximately 20–50% of the desired full output load current. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_{SW}), and the maximum output current ($I_{OUT,MAX}$), and then estimating a ΔI_L as some percentage of that current:

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak-current inductor current $I_{L,PEAK}$.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

$$I_{L,PEAK} = I_{OUT,MAX} + \Delta I_L/2$$

Select an inductor with a saturation current and thermal rating in excess of $I_{L,PEAK}$.

If USM light-load operation is selected, make sure the inductor value is high enough to avoid triggering the

reverse-current limit just under steady state if the load current is zero.

For maximum efficiency, select an inductor with a low DCR that meets the inductance, size, and cost targets. Low-loss ferrite materials should be considered.

Inductor Design Example

Consider a typical design for a device providing 5.15V$_{OUT}$ at 11A from 12V$_{IN}$, operating at 600kHz and using target inductor ripple current (ΔI_L) of 40% or 4.4A. First, determine the approximate inductance value:

$$L_1 = \frac{5.15V \times (12V - 5.15V)}{12V \times 600kHz \times 4.4A} = 1.11\mu H$$

Next, select the nearest standard inductance value, in this case 1.5µH, and calculate the resulting inductor ripple current (ΔI_L):

$$\Delta I_L = \frac{5.15V \times (12V - 5.15V)}{12V \times 600kHz \times 1.5\mu H} = 3.27A$$

$$I_{L,PEAK} = 11A + 3.27A/2 = 12.635A$$

The resulting 3.27A ripple current is 29.73% (3.27A/11A), well within the 20–50% target.

$$I_{L,PEAK,RVS} = 3.27A/2 = 1.635A < I_{LIM,RVS}$$

Finally, select an available inductor with a saturation current higher than the resulting $I_{L,PEAK}$ of 12.635A.

Output Capacitor Selection

Instant-PWM provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

Output Ripple

Output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors ESR (ESR ripple), as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with ΔI_L = 3.27A using three 22µF ceramic capacitors, each with an ESR of approximately 6mΩ for a parallel total of 66µF and 2mΩ ESR.

$$V_{RIPPLE,ESR} = 3.27A \times 2m\Omega = 6.54mV$$

$$V_{RIPPLE,CAP} = \frac{3.27A}{8 \times 66\mu F \times 600kHz} = 10.32mV$$

Total ripple = 16.86mV. The actual capacitive ripple may be higher than the calculated value because the capacitance derating with the voltage on the capacitor.

Using a 150µF 40mΩ POS cap, the result is:

$$V_{RIPPLE,ESR} = 3.27A \times 40m\Omega = 130.80mV$$

$$V_{RIPPLE,CAP} = \frac{3.27A}{8 \times 150\mu F \times 600kHz} = 4.54mV$$

Total ripple = 135.34mV.

Output Transient Undershoot/Overshoot

If very fast load transients must be supported, consider the effect of the output capacitor on the output transient undershoot and overshoot. Instant-PWM responds quickly to changing load conditions, but some considerations are still required, especially when using small ceramic capacitors. These capacitors have low capacitance at low output voltages, which results in insufficient stored energy for load transients. Output-transient undershoot and overshoot have two causes: voltage changes caused by the ESR of the output capacitor, and voltage changes caused by the output capacitance and inductor current slew rate.

ESR undershoot or overshoot may be calculated as $V_{ESR} = \Delta I_{OUT} \times ESR$. Using the ceramic capacitor example above and a fast load transient of +/- 5.5A, V_{ESR} = +/- 5.5A × 2mΩ = +/- 11mV. The POS capacitor result with the same load transient, V_{ESR} = +/- 5.5A × 40mΩ = +/- 220mV.

Capacitive undershoot (load increasing) is a function of the output capacitance, load step, inductor value, input-output voltage difference, and maximum duty factor. During a fast load transient, the maximum duty factor of instant-PWM is a function of t_{ON} and the minimum t_{OFF}, as the control scheme is designed to rapidly ramp the inductor current by grouping together many t_{ON} pulses in this case. The maximum duty factor D_{MAX} may be calculated as:

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF,MIN}}$$

Given this, the capacitive undershoot may be calculated as:

$$V_{UNDERSHOOT,CAP} = -\frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times (V_{IN,MIN} \times D_{MAX} - V_{OUT})}$$

Consider a 5.5A load increase using the ceramic capacitor case when V_{IN} = 12V. At V_{OUT} = 5.15V, the result is t_{ON} = 715.28ns, $t_{OFF,MIN}$ = 150ns, D_{MAX} = 715.28 / (715.28 + 150) = 0.826 and

$$V_{UNDERSHOOT,CAP} = -\frac{1.5\mu H \times (5.5A)^2}{2 \times 66\mu F \times (12V \times 0.826 - 5.15V)} = -72.19mV$$

Using the POS capacitor case, the result is

$$V_{UNDERSHOOT,CAP} = -\frac{1.5\mu H \times (5.5A)^2}{2 \times 150\mu F \times (12V \times 0.826 - 5.15V)} = -31.76mV$$

Capacitive overshoot (load decreasing) is a function of the output capacitance, inductor value, and output voltage.

$$V_{OVERSHOOT,CAP} = \frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times V_{OUT}}$$

Consider a 5.5A load decrease using the ceramic capacitor case above. At V_{OUT} = 5.15V the result is

$$V_{OVERSHOOT,CAP} = \frac{1.5\mu H \times (5.5A)^2}{2 \times 66\mu F \times 5.15V} = 66.75mV$$

Using the POS capacitor case, the above result is

$$V_{OVERSHOOT,CAP} = \frac{1.5\mu H \times (5.5A)^2}{2 \times 150\mu F \times 5.15V} = 29.37mV$$

Combine the ESR and capacitive undershoot and overshoot to calculate the total overshoot and undershoot for a given application.

Load-Transient Considerations

The SY21249C1 uses the instant-PWM architecture to achieve good stability and fast transient responses. In applications with high step load current, adding an RC feed-forward compensation network, consisting of R_{FF} and C_{FF} between the OUT pin and the FF pin may further speed up the load-transient responses. R_{FF} = 1kΩ and C_{FF} = 470pF have been shown to perform well in most applications. Increasing C_{FF} will speed up the load-transient response if there is no stability issue.

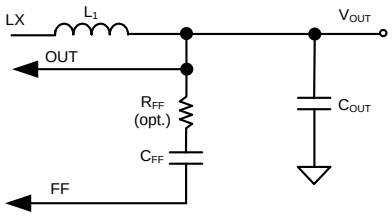


Figure 13. Feed-forward network

Note that when C_{OUT} > 500µF and minimum load current is low, using R_{FF} = 1kΩ and C_{FF} = 2.2nF is recommended, to provide sufficient ripple to FB, enable small output ripple and good transient behavior.

Thermal Design Considerations

The maximum power dissipation depends on multiple factors: PCB layout, IC package thermal resistance, local airflow, and the junction temperature relative to ambient. The maximum power dissipation may be calculated as:

$$P_{D,MAX} = (T_{J,MAX} - T_A) / \theta_{JA}$$

Where, $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For the QFN2.5×2.5-16 package the thermal resistance θ_{JA} is 27°C /W when measured on a standard Silergy 8.5cm×8.5cm four-layer thermal test board. These standard thermal test layouts have a very large area with long 2-oz. copper traces connected to each IC pin and very large, unbroken 1-oz. internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical tiny evaluation board area requires wide copper traces well-connected to the IC's backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane and, perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at T_A = 25°C may be calculated using the following formula:

$$P_{D,MAX} = (125°C - 25°C) / (27°C/W) = 3.7W$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA}. Use the derating curve in figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.

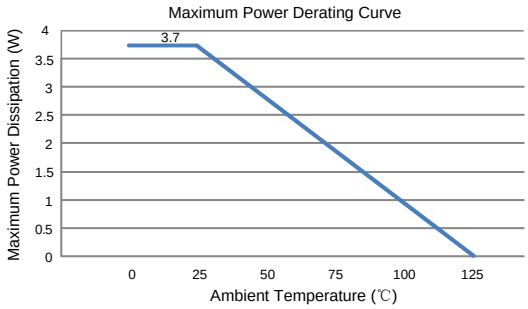
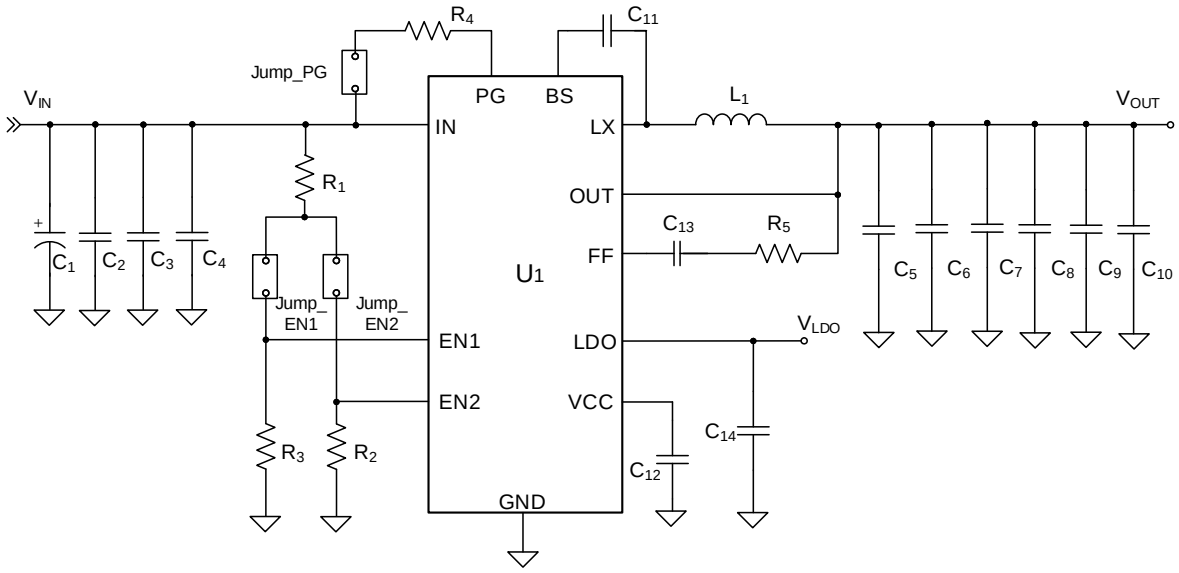


Figure 14. Maximum power dissipation

Application Schematic



BOM List

Designator	Description	Part Number	Manufacturer
U1	11A, Buck with 5V LDO	SY21249C1TMC	Silergy
C1	47μF/50V, Electrolytic Cap		
C2, C3	10μF/50V/X5R, 1206	GRM31CR61H106KA12L	mμRata
C4, C11	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	mμRata
C5, C6, C7, C8	22μF/16V/X5R, 1206	GRM31CR61C226ME15L	mμRata
C9, C10	NC		
C12	2.2μF/16V/X5R, 0603	GRM188R61C225KE15D	mμRata
C13	470pF/50V/C0G, 0603	GRM1885C1H471JA01D	mμRata
C14	4.7μF/16V/X5R, 0603	GRM185R61C475KE11D	mμRata
L1	1.5μH/16A, inductor	PCMB104T-1R5MS	CYNTEC
R1	10kΩ, 1%, 0603		
R2, R3	1MΩ, 1%, 0603		
R4	100kΩ, 1%, 0603		
R5	1kΩ, 1%, 0603		
R6, R7	NC		
U1	11A, Buck with 5V LDO	SY21249C1TMC	Silergy

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

- **Input Capacitors:** Place the input capacitors close to the IN and GND pins, minimizing the loop formed by these connections. The input capacitor should be connected to the IN and GND using wide copper areas. A 0.1μF input ceramic capacitor in parallel with C_{IN} is recommended to reduce the input noise.
- **Output Capacitors:** Connect the C_{OUT} negative sides to the GND pin by wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.
- **V_{CC} Capacitor:** Place the V_{CC} capacitor close to V_{CC} using short, a direct copper trace to one nearest device GND pin (pin 14).
- **BYP Capacitor:** Place the BYP capacitor close to BYP using a short, direct copper trace to the nearest device GND pin (pin 14) if the bypass function is used.
- **Feedback Network:** Place the feedback components (R1, R2, R_{FF}, and C_{FF}) as close to the FB pin as possible. Avoid routing the feedback line near LX, BS, or other high-frequency signals as it is noise-sensitive. Use a Kelvin connection for the feedback sampling point to C_{OUT}, rather than the inductor output terminal.
- **LX Connection:** Keep the LX area small to prevent excessive EMI, while providing a wide copper area to minimize parasitic resistance and inductance. Use wide LX copper traces between pin 2 and pin 12 to improve efficiency.
- **BS Capacitor:** Place the BS capacitor on the same layer as the device, keep the BS voltage path (BS, LX, and C_{BS}) as short as possible.
- **Control Signals:** It is not recommended to connect control signals directly to IN. A resistor in a range of 1kΩ to 1MΩ should be used if they are pulled high by IN.
- **GND Vias:** Place an adequate number of vias on the GND layer around the device for better thermal performance. Specifically, create good thermal contact by adding several GND vias around pin 3 and pin 11.
- **PCB Board:** A four-layer layout with 2oz copper is strongly recommended to achieve better thermal performance. Provide large copper areas for IN and GND on the top land bottom layers and maximize their size. Middle1 layer should be used as GND plane layer for conducting heat and shielding the middle2 layer signal lines from top layer crosstalk. Place signal lines on middle2 layer instead of the other layers, to reduce any cuts in the GND planes on the other layers.

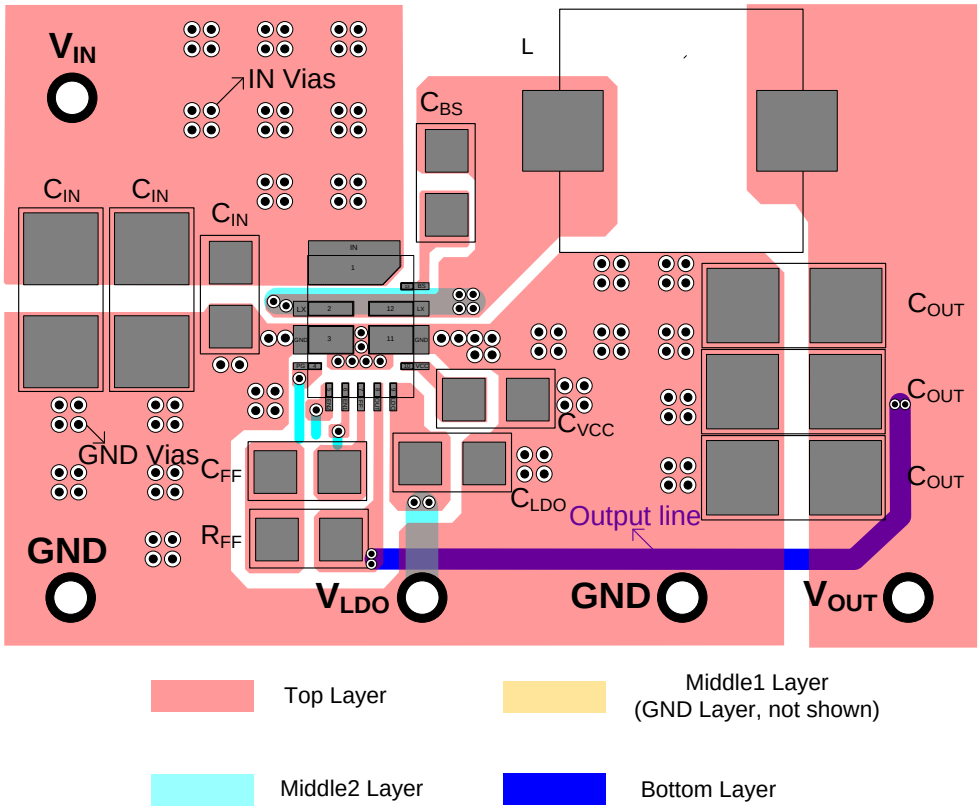
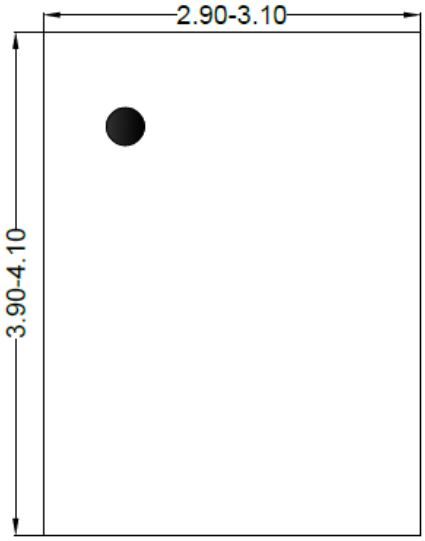
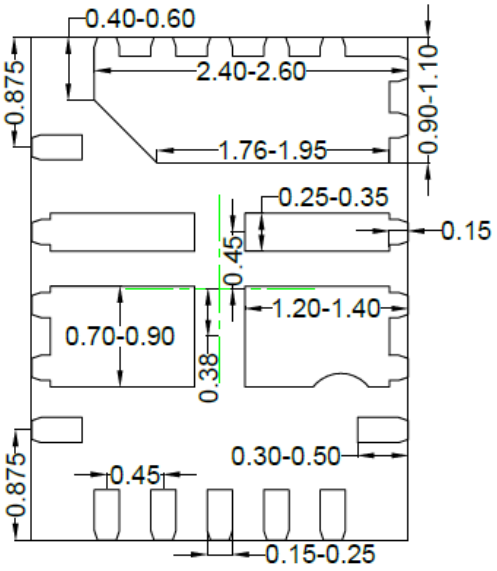


Figure 4. PCB Layout Suggestion

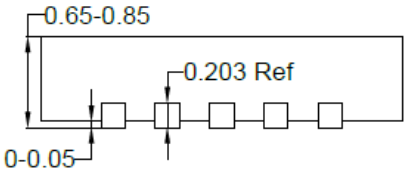
QFN3×4-13 Package Outline and PCB Layout Design



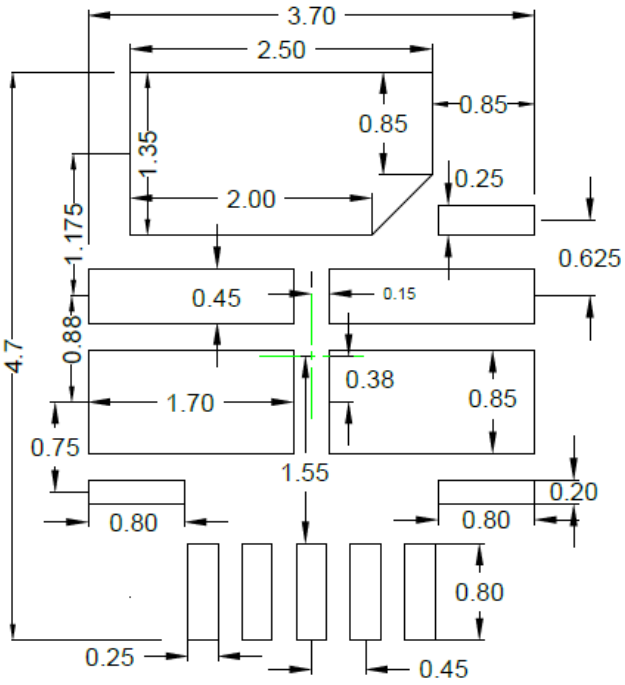
Top view



Bottom view



Side view

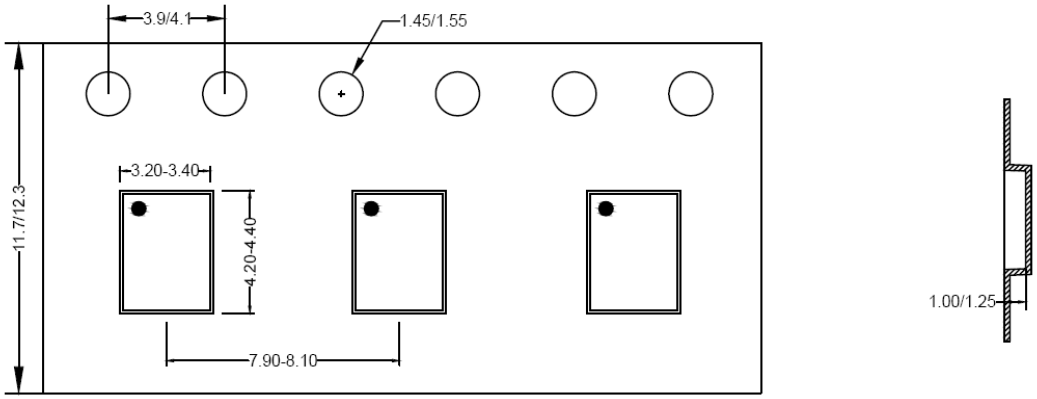


Recommended PCB layout
(Reference only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr. Center line indicates chip body center.*

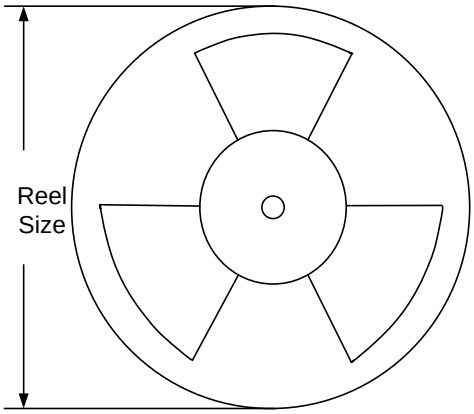
Taping and Reel Specification

QFN3×4-13 taping orientation



Feeding direction →

Carrier Tape and Reel specification for packages



Package Type	Tape Width (mm)	Pocket Pitch (mm)	Reel Size (Inch)	Trailer Length (mm)	Leader Length (mm)	Qty per Reel
QFN3×4	12	8	13"	400	400	5000

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Sep.17, 2022	Revision 1.0	Product Release
Sep.17, 2021	Revision 0.9C	Fix an error in page 20: tape width changes from 12mm to 8mm
Jan.22, 2021	Revision 0.9B	Add (IN-LX) voltage in Absolute Maximum Ratings; Add “A 0.1μF input ceramic capacitor is recommended to reduce the input noise.” in the pin description and the layout design; Add Table1: Programmable Valley Current Limit in page 14.
Sep.9, 2020	Revision 0.9A	Revise some design formulas in the section of “Output Transient Undershoot/Overshoot” (page 16)

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