IS34ML04G088/168
IS35ML04G088/168

4Gb SLC-8b ECC

3.3V X8/X16 NAND FLASH MEMORY STANDARD NAND INTERFACE

4Gb (x8/x16) 3.3V NAND FLASH MEMORY with 8b ECC

FEATURES

- **Flexible & Efficient Memory Architecture**
  - Memory Cell: 1bit/Memory Cell
  - Organization: 512Mb x8, 256Mb x16
  - Page Size for x8: (4K + 256) Bytes
  - Page Size for x16: (2K + 128) words
  - Block Size for x8: 64x (4K + 256) Bytes
  - Block Size for x16: 64x (2K + 128) words
  - Number of Plane = 1
  - Number of Block per Die (LUN) = 2048

- **Highest performance**
  - Read Performance:
    - Random Read: 25us (Max.)
    - Serial Access: 25ns (Max.)
  - Write Performance:
    - Program time: 300us (typ.), 700us (max.)
    - Block Erase time: 3.5ms (typ.), 10ms (max.)

- **Voltage and Temp. Ranges**
  - Single 3.3V (2.7V to 3.6V) Voltage Supply
  - Temp Grades:
    - Industrial: -40°C to +85°C
    - Automotive, A2: -40°C to +105°C

- **Reliable CMOS Floating Gate Technology**
  - ECC Requirement: **8bit/512Byte**
  - Endurance: 60K Program/Erase cycles
  - Data Retention: 10 years

- **Efficient Read and Program modes**
  - Command/Address/Data Multiplexed I/O Interface
  - Command Register Operation
  - Automatic Page 0 Read at Power-Up Option
    - Boot from NAND support
    - Automatic Memory Download
  - NOP: 4 cycles
  - Cache Program Operation for High Performance Program
  - Cache Read Operation
  - Copy-Back Operation
  - OTP operation
  - EDO mode
  - Block Protection
  - Page copy

- **Advanced Security Protection**
  - Hardware Data Protection: Program/Erase Lockout during Power Transitions

- **Industry Standard Pin-out & Packages**
  - T =48-pin TSOP (Type I)
  - B =63-ball VFBGA

GENERAL DESCRIPTION

The device has 4352-byte static registers which allow program and read data to be transferred between the register and the memory cell array in 4352-byte increments. The Erase operation is implemented in a single block unit (256Kbytes + 16Kbytes).

Data in the page mode can be read out at 25ns cycle time per Word. The I/O pins serve as the ports for address and command inputs as well as data input/output.

The copy back function allows the optimization of defective blocks management: when a page program operation fails, the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase.

The cache program feature allows the data insertion in the cache register while the data register is copied into the Flash array.

This pipelined program operation improves the program throughput when long files are written inside the memory. A cache read feature is also implemented. This feature allows to dramatically improving the read throughput when consecutive pages have to be streamed out. This device includes extra feature: Automatic Read at Power Up.

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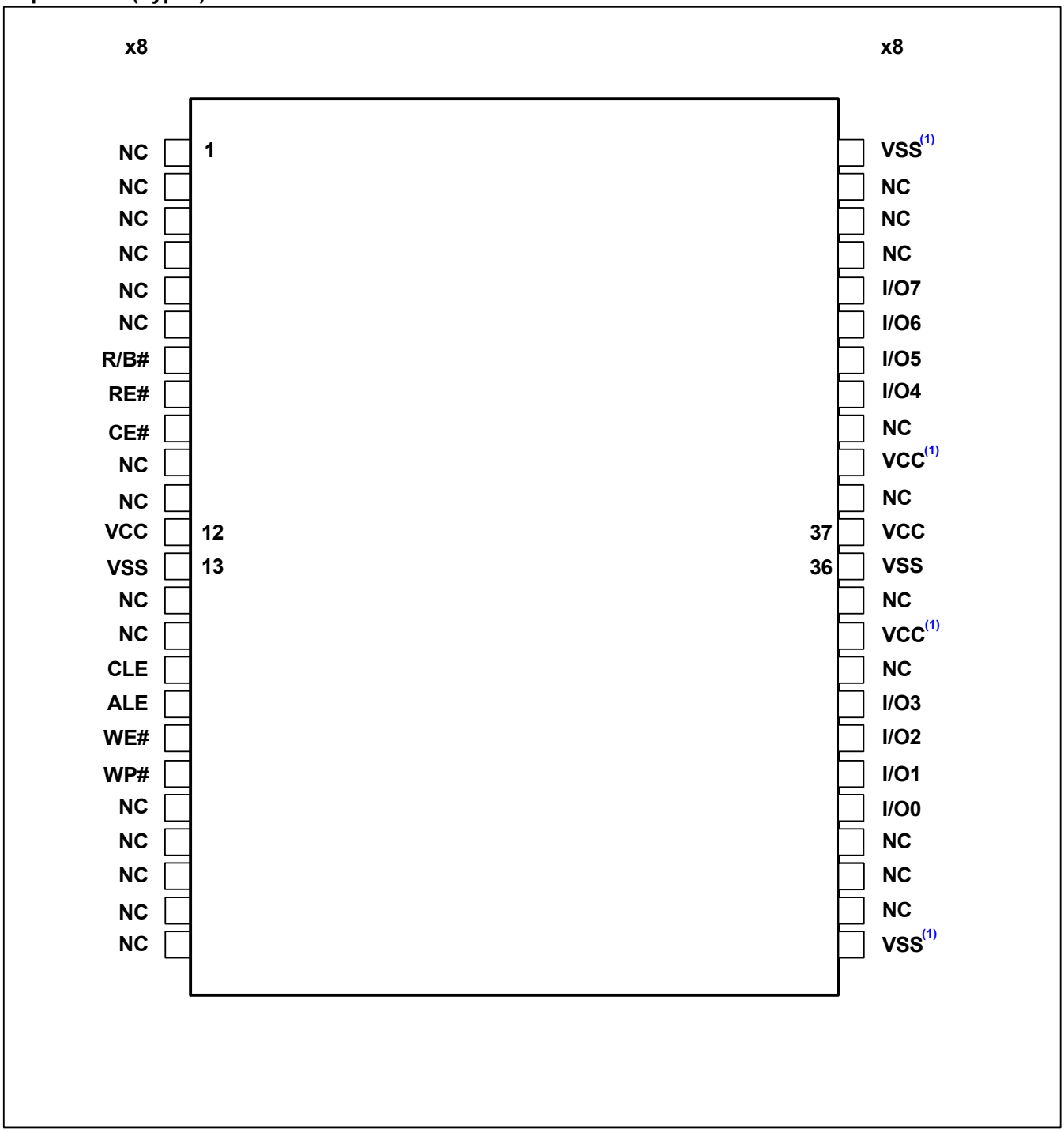
1. PIN CONFIGURATION

48-pin TSOP (Type I)



Note:

1. These pins might not be bonded in the package (NC); however it is recommended to connect these pins to the designated external sources.

63-ball VFBGA(x8)

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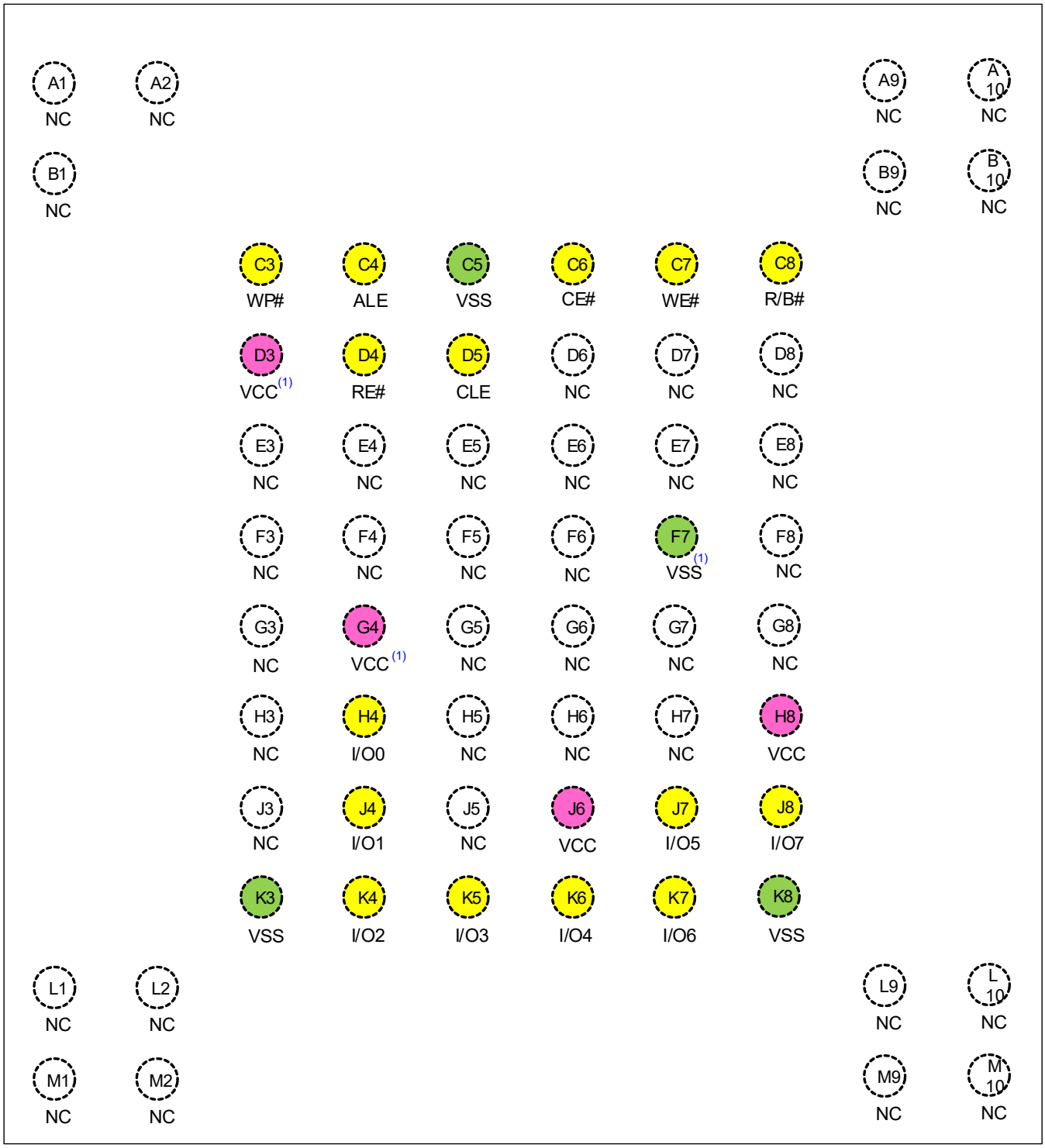

Note:

1. These pins might not be bonded in the package; however it is recommended to connect these pins to the designated external sources for ONFI compatibility.

63-ball VFBGA (x16)

Balls Down, Top View
(x16)
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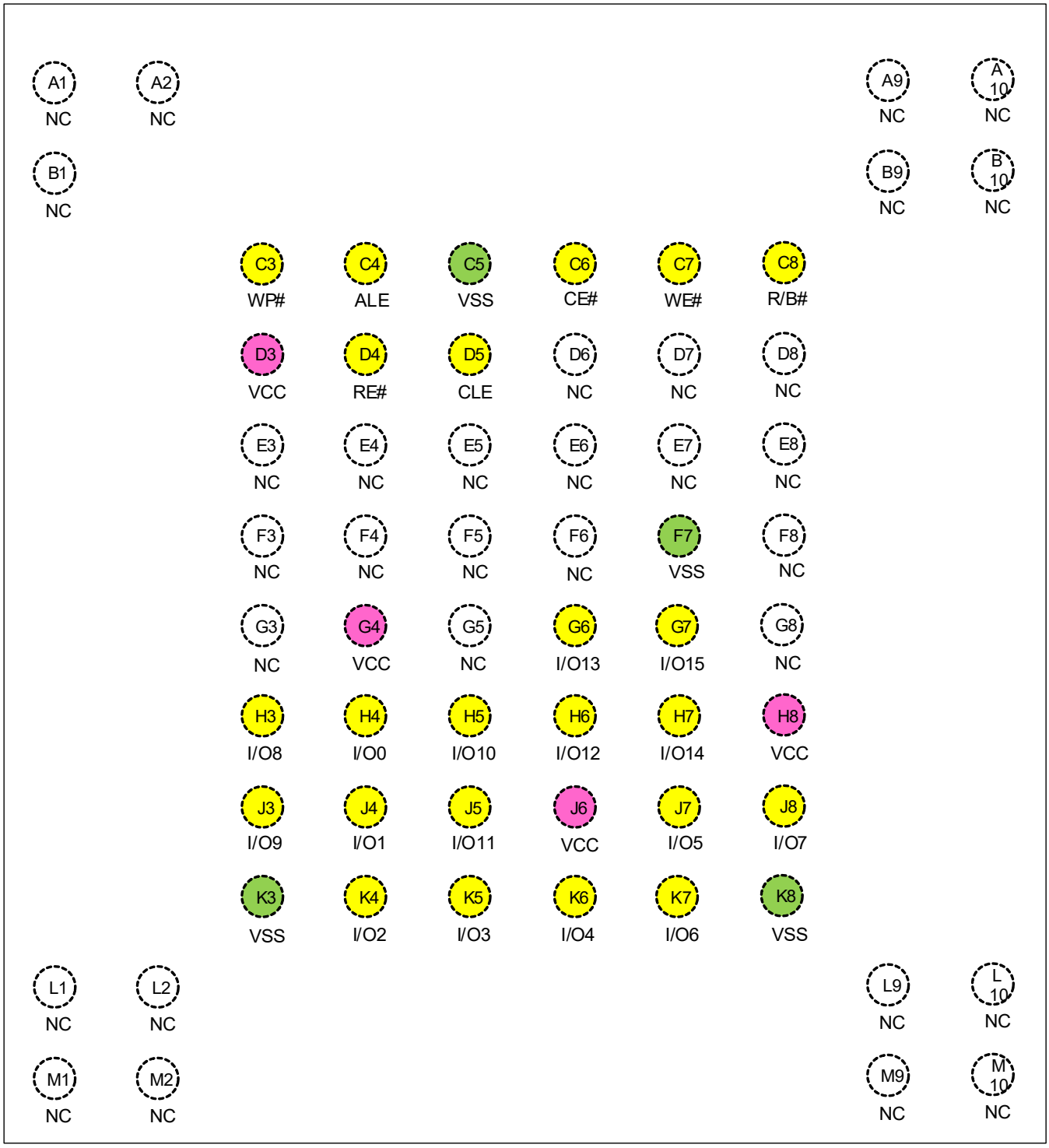


2. PIN DESCRIPTIONS

Pin Name	Pin Function
I/O0 ~ I/O7 (X8) I/O0 ~ I/O15 (X16)	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the internal command registers. Commands are latched into the command register through the I/O ports on the rising edge of the WE# signal with CLE high.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for addresses sent to the internal address registers. Addresses are latched into the address register through the I/O ports on the rising edge of WE# with ALE high.
CE#	**CHIP ENABLE** The CE# input is the device selection control. When the device is in the Busy state, CE# high is ignored, and the device does not return to standby mode in program or erase operation. Regarding CE# control during read operation, refer to 'Page read' section of Device operation.
RE#	**READ ENABLE** The RE# input is the serial data-out control, and when it is active low, it drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE# which also increments the internal column address counter by one.
WE#	**WRITE ENABLE** The WE# input controls writes to the I/O ports. Commands, address and data are latched on the rising edge of the WE# pulse.
WP#	**WRITE PROTECT** The WP# pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the WP# pin is active low.
R/B#	**READY/BUSY OUTPUT** The R/B# output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in progress and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
VCC	**POWER** VCC is the power supply for device.
VSS	**GROUND**
N.C.	**NO CONNECTION** Lead is not internally connected.

3. BLOCK DIAGRAM

3.1 BLOCK DIAGRAM

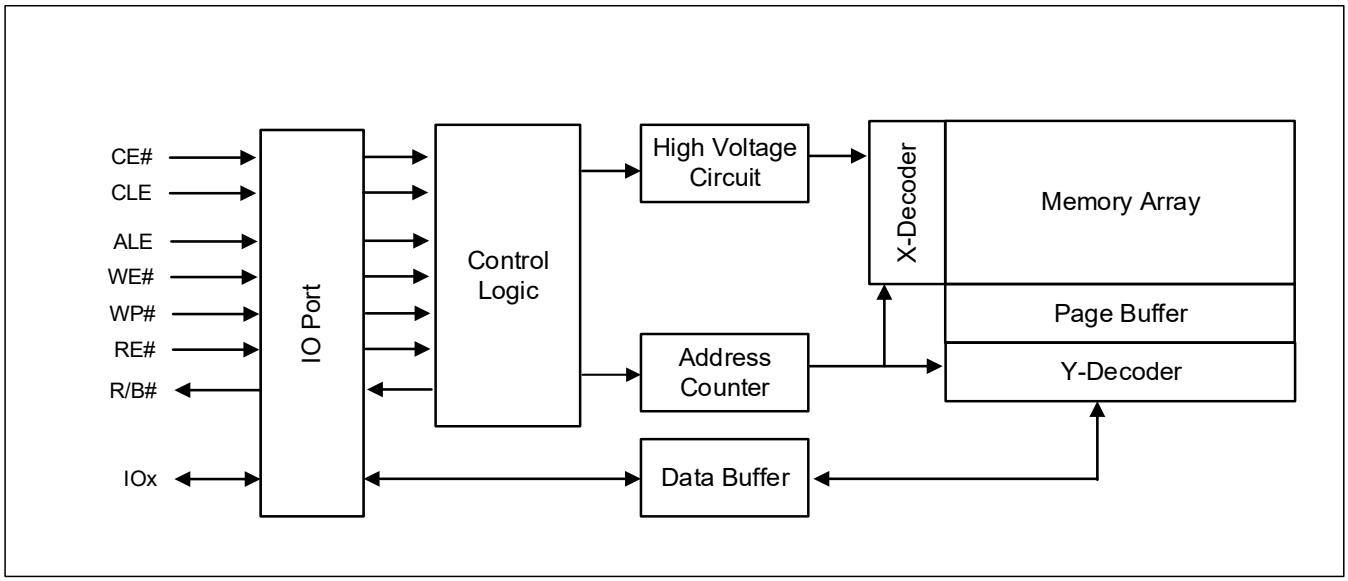


Figure 3.1 Functional Block Diagram

3.2 ADDRESSING

There are two address types used: the column address and the row address. The column address is used to access bytes within a page, i.e. the column address is the byte offset into the page. The row address is used to address pages, blocks, and LUNs.

When both the column and row addresses are required to be issued, the column address is always issued first in one or more 8-bit address cycles. The row addresses follow in one or more 8-bit address cycles. There are some functions that may require only row addresses, such as Block Erase. In this case the column addresses shall not be issued.

For both column and row addresses, the first address cycle always contains the least significant bits and the last cycle always contains the most significant bits. If there are bits in the most significant cycles of the column and row addresses that are not used, then they are required to be cleared to zero.

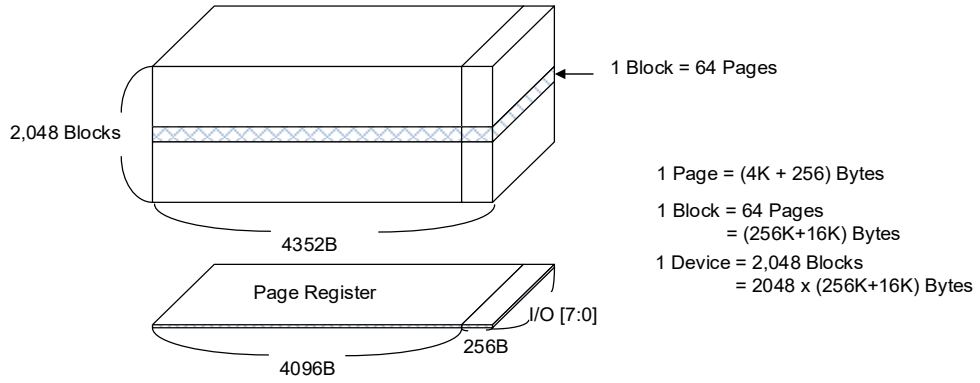


Figure 3.2 Array Organization (x8)

Table 3.1 ARRAY Address (x8)

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	Address
1st cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	Column Address
2nd cycle	A_8	A_9	A_{10}	A_{11}	A_{12}	*L	*L	*L	Column Address
3rd cycle	A_{13}	A_{14}	A_{15}	A_{16}	A_{17}	A_{18}	A_{19}	A_{20}	Row Address
4th cycle	A_{21}	A_{22}	A_{23}	A_{24}	A_{25}	A_{26}	A_{27}	A_{28}	Row Address
5th cycle	A_{29}	*L	*L	*L	*L	*L	*L	*L	Row Address

Notes:
1. Column Address: Starting Address of the Register.
2. *L must be set to “Low”.
3. The device ignores any additional input of address cycles than required.
4. A_{13} ~ A_{18} are for Page Address, A_{19} ~ A_{29} are for Block Address.

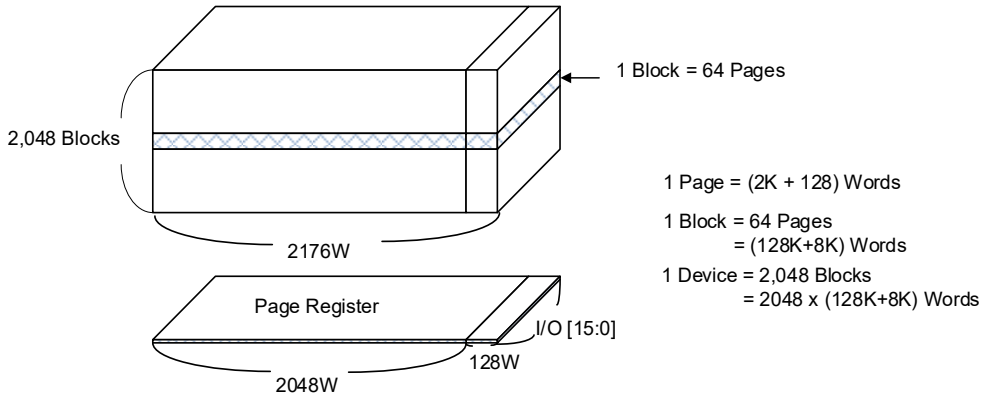


Figure 3.2 Array Organization (x16)

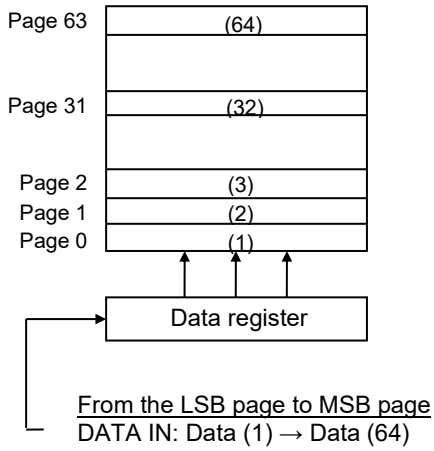
Table 3.2 ARRAY Address (x16)

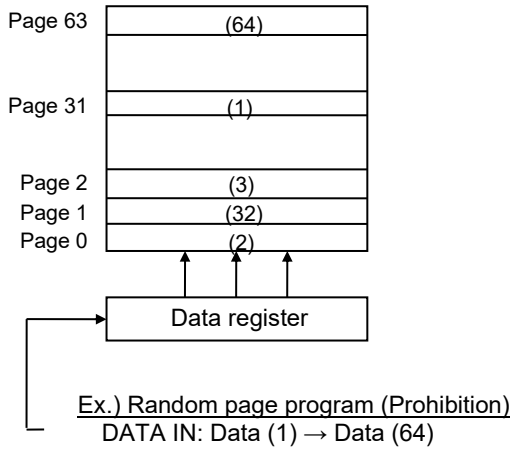
	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	I/O 8~I/O15	Address
1st cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	*L	Column Address
2nd cycle	A_8	A_9	A_{10}	A_{11}	*L	*L	*L	*L	*L	Column Address
3rd cycle	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	A_{17}	A_{18}	A_{19}	*L	Row Address
4th cycle	A_{20}	A_{21}	A_{22}	A_{23}	A_{24}	A_{25}	A_{26}	A_{27}	*L	Row Address
5th cycle	A_{28}	*L	*L	*L	*L	*L	*L	*L	*L	Row Address

Notes:
1. Column Address: Starting Address of the Register.
2. *L must be set to “Low”.
3. The device ignores any additional input of address cycles than required.
4. A_{12} ~ A_{17} are for Page Address, A_{18} ~ A_{28} are for Block Address.

3.3 ADDRESSING FOR PROGRAM OPERATION

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB page doesn't need to be page 0.





4. FUNCTION DESCRIPTION

The IS34/35ML04G088 is a 4Gbit memory organized as 128K rows (pages) by 4,352x8 columns. Spare 256x8 columns are located from column address of 4,096~4,351.

The IS34/35ML04G168 is a 4Gbit memory organized as 128K rows (pages) by 2,176x16 columns. Spare 128x16 columns are located from column address of 2,048~2,175.

A 4,096-byte data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 2,048 separately erasable 256K-byte blocks.

The device has addresses multiplexed into 8 I/Os for x8, and 16 I/Os for x16. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing WE# to low while CE# is low. Those are latched on the rising edge of WE#. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution.

In addition to the enhanced architecture and interface, the device incorporates copy-back program feature from one page to another page without need for transporting the data to and from the external buffer memory.

4.1 WRITE PROTECT

When WP# is enabled, Flash array is blocked from any program and erase operations. This signal shall only transitioned when a target is idle. The host shall be allowed to issue a new command after tWW once WP# is enabled. Figures below describes the tWW timing requirement, shown with the start of a Program command and the start of an Erase command.

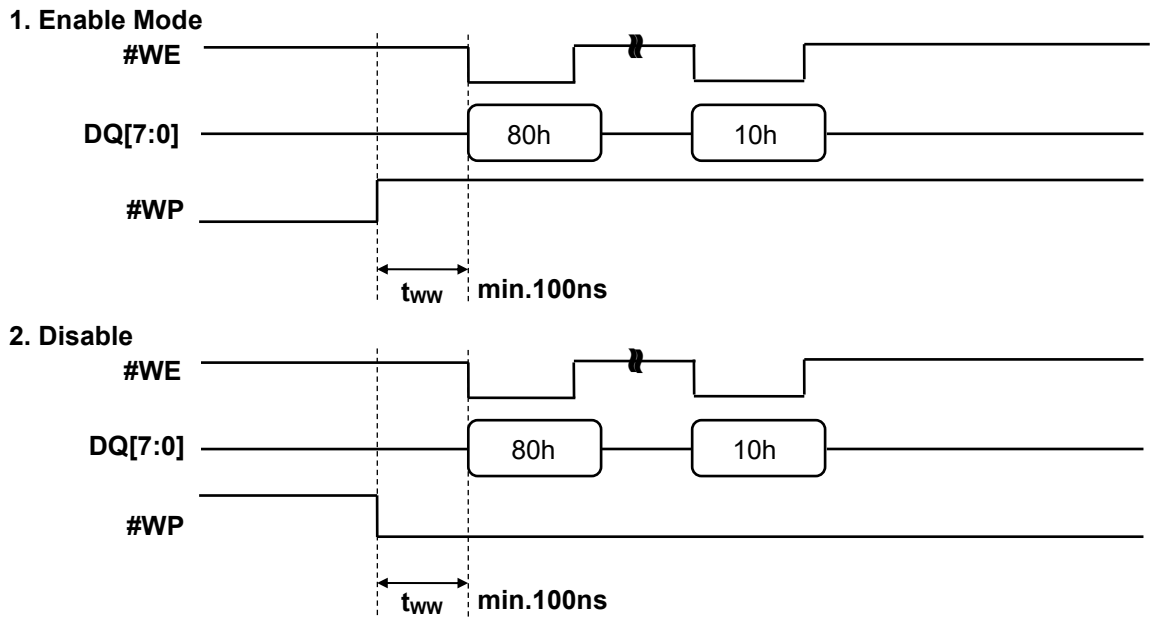


Figure 4.1 WRITE PROTECT timing requirements of the Program operation.

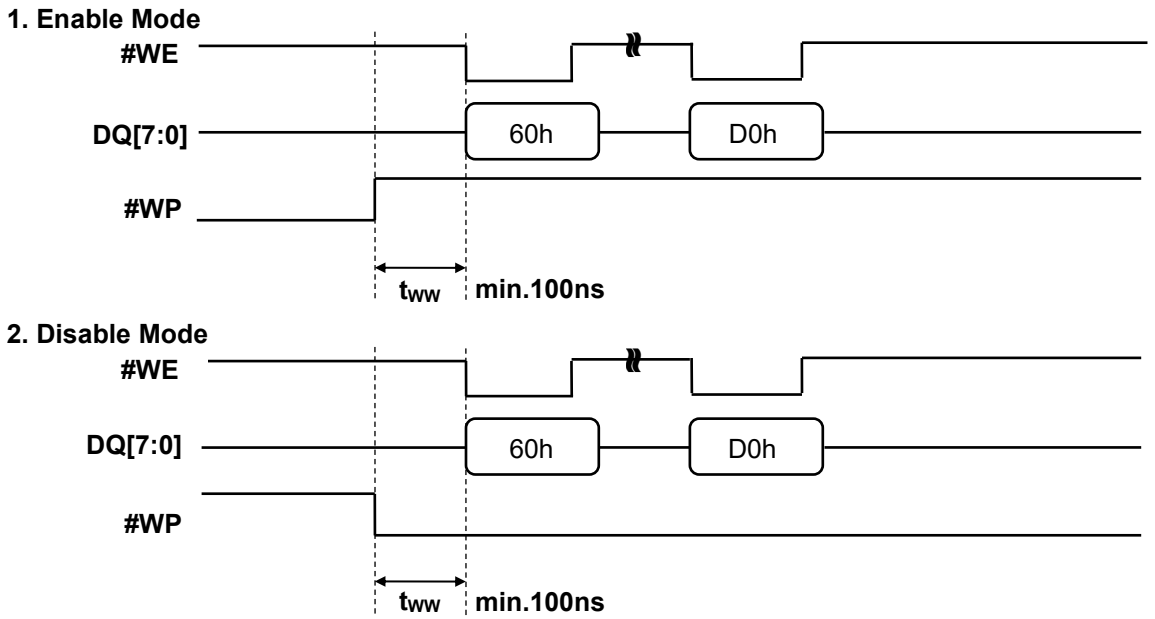


Figure 4.2 WRITE PROTECT timing requirements of the Erase operation.

4.2 DISCOVERY AND INITIALIZATION

The device is designed to offer protection from any involuntary program/erase during power transitions. An internal voltage detector disables all functions whenever V_{CC} is below about 2.3V. Max busy time is 5ms after Power-On Reset. During busy time of resetting, the acceptable command is the Read Status (70h).

WP# provides hardware protection and is recommended to be kept at V_{IL} during power up and power down. The two step command sequence for program/erase provides additional protection. Figure below defines the Initialization behavior and timings.

4.3 DATA PROTECTION AND POWER ON SEQUENCE

The timing sequence shown in the figure below is necessary for the power-on/off sequence.

The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence. During the initialization the device R/B# signal indicates the Busy state as shown in the figure below. In this time period, the acceptable commands are 70h.

The WP# signal is useful for protecting against data corruption at power on/off.

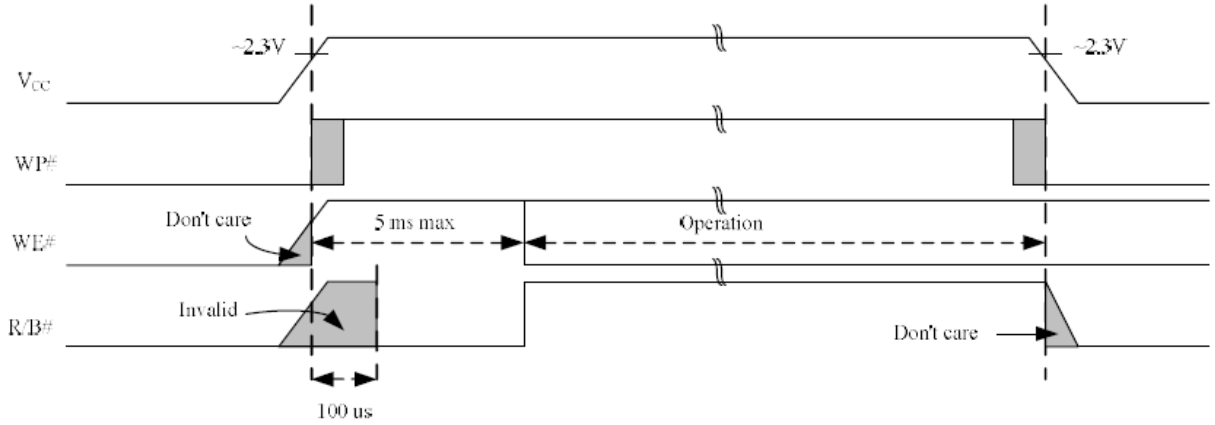


Figure 4.3 AC Waveforms for POWER TRANSITION

4.4 COMMAND SET

Table 4.1 Command Set

Function	1st Cycle	2nd Cycle	Acceptable Command during Busy
Read	00h	30h	
Read for Copy-Back	00h	35h	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input (1)	85h	-	
Random Data Output (1)	05h	E0h	
Read Status	70h	-	O
Block Protection Status Read(2)	74h	-	O
Cache Program	80h	15h	
Cache Read	31h	-	
Read Start for Last Page Cache Read	3Fh	-	
Block Protection-Prohibit both programing and erasing	43h-80h	10h	
Block Protection-Prohibit erasing	42h-80h	10h	
Block Protection-Prohibit programing	41h-80h	10h	
Block Protection Status	00h	34h	
Read for Page Copy with Data Out	00h	3Ah	
Auto Program with Data Cache during Page Copy	8Ch	15h	
Auto Program for last page during Page Copy	8Ch	10h	
Set Features	EFh	-	
Read Parameter Page	ECh	-	
Read Unique ID	EDh	-	

Notes:

1. Random Data Input/Output can be executed in a page.

5. ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATINGS (1)

Storage Temperature	-65°C to +150°C
Input Voltage with Respect to Ground on All Pins	-0.6V to +4.6V
All I/O Voltage with Respect to Ground	-0.6V to V_{CC} + 0.3V(< 4.6V)
V_{CC}	-0.6V to +4.6V
Short Circuit Current	5mA
Electrostatic Discharge Voltage (Human Body Model)(2)	-2000V to +2000V

Notes:

1. **Applied conditions greater than those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**
2. **ANSI/ESDA/JEDEC JS-001**

5.2 RECOMMENDED OPERATING CONDITIONS

Part Number		IS34/35ML04G088, IS34/35ML04G168
Operating Temperature	Industrial Grade	-40°C to 85°C
	Automotive Grade A2	-40°C to 105°C
V_{CC} Power Supply		2.7V (VMIN) – 3.6V (VMAX); 3.3V (Typ)

5.3 DC CHARACTERISTICS

(Under operating range)

Parameter		Symbol	Test Conditions	Min	Typ.	Max	Unit
Operating Current	Page Read with Serial Access	ICC1	tRC=tRC$_{MIN}$, CE#=VIL, IOUT=0mA	-	15	30	mA
	Program	ICC2	-	-	15		
	Erase	ICC3	-	-	15		
Stand-by Current (TTL)		ISB1	CE#=VIH, WP#=0V/VCC	-	-	1	
Stand-by Current (CMOS)		ISB2	CE#=VCC-0.2, WP#=0V/VCC	-	10	50	uA
Input Leakage Current		ILI	VIN=0 to Vcc (max)	-	-	+/-10	
Output Leakage Current		ILO	VOUT=0 to Vcc (max)	-	-	+/-10	
Input High Voltage		VIH (1)		0.8xVCC	-	Vcc+0.3	V
Input Low Voltage, All inputs		VIL (1)		-0.3	-	0.2xVCC	
Output High Voltage Level		VOH	IOH=-400 uA	2.4	-	-	
Output Low Voltage Level		VOL	IOL=2.1mA	-	-	0.4	
Output Low Current (R/B#)		IOL (R/B#)	VOL=0.4V	8	10	-	mA

Notes:
1. VIL can undershoot to -2V and VIH can overshoot to VCC + 2V for durations of 20 ns or less.
2. Typical value are measured at Vcc=3.3V, TA=25℃. Not 100% tested.

5.4 VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
IS34/35ML04G088/168	NVB	2,008	-	2,048	Block

Notes:
1. The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment and is guaranteed to be a valid block with 8bit ECC per 544 bytes - 512Byte (main)+ 16Byte (Spare)+16Byte (parity) - of data.

5.5 AC MEASUREMENT CONDITION

Symbol	Parameter	Min	Max	Units
CL	Output Load	1 TTL GATE and CL = 50pF		pF
TR,TF	Input Rise and Fall Times		5	ns
VIN	Input Pulse Voltages	0V to V_{CC}		V
VREFI	Input Timing Reference Voltages	$0.5V_{CC}$		V
VREFO	Output Timing Reference Voltages	$0.5V_{CC}$		V

Note:
1. Refer to Ready/Busy#, R/B#'s Busy to Ready time is decided by pull up register (Rp) tied to R/B# pin.

5.6 AC PIN CAPACITANCE (TA = 25°C, VCC=3.3V, 1MHZ)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	-	-	10	pF
$C_{I/O}$	Input /Output Capacitance	$V_{I/O}$ = 0V	-	-	10	pF

Note:
1. These parameters are characterized and not 100% tested.

5.7 MODE SELECTION

CLE	ALE	CE#	WE#	RE#	WP#	Mode	
H	L	L	↑	H	X	Read Mode	Command Input
L	H	L	↑	H	X		Address Input (5 clock)
H	L	L	↑	H	H	Write Mode	Command Input
L	H	L	↑	H	H		Address Input (5 clock)
L	L	L	↑	H	H	Data Input	
L	L	L	H	↓	X	Data Output	
X	X	X	X	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}(2)	Stand-by	

Notes :
1. X can be VIL or VIH.
2. WP# should be biased to CMOS high or CMOS low for standby.

5.8 READ/ROGRAM/ERASE PERFORMANCNE

Parameter	Symbol	Min	Typ	Max	Unit
Data Transfer from Cell to Register	tR	-	-	25	us
Program Time	tPROG	-	300	700	us
Last Page Program Time	tLPROG(4)	-	-	-	us
Dummy Busy Time for Cache Operation	tCBSY	-	3	750	us
Number of Partial Program Cycles in the Same Page	NOP	-	-	4	cycle
Block Erase Time	tBERS	-	3.5	10	ms
Data Cache Busy Time in Write Cache (following 15h)	tDCBSYW2	-	-	700	us

Notes:
1. Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 3.3V Vcc and 25℃ temperature.
2. tCBSY max.time depends on timing between internal program completion and data-in.
3. tDCBSYW2 depends on the timing between internal programming time and data in time.
4. tLPROG=tPROG(last page)+tPROG(last-1 page) – Command load time(last page) – Address load time(last page) – Data load time(last page)

5.9 AC CHARACTERISTICS FOR ADDRESS/ COMMAND/DATA INPUT

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	tCLS(1)	12	-	ns
CLE Hold Time	tCLH	5	-	ns
CE# Setup Time	tCS(1)	20	-	ns
CE# Hold Time	tCH	5	-	ns
WE# Pulse Width	tWP	12	-	ns
ALE Setup Time	tALS(1)	12	-	ns
ALE Hold Time	tALH	5	-	ns
Data Setup Time	tDS(1)	12	-	ns
Data Hold Time	tDH	5	-	ns
Write Cycle Time	tWC	25	-	ns
WE# High Hold Time	tWH	10	-	ns
Address to Data Loading Time	tADL(2)	70(2)	-	ns

Notes:
1. The transition of the corresponding control pins must occur only once while WE# is held low.
2. tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

5.10 AC CHARACTERISTICS FOR OPERATION

Parameter		Symbol	Min	Max	Unit
Data Transfer from Cell to Register		tR	-	25	us
ALE to RE# Delay		tAR	10	-	ns
CLE to RE# Delay		tCLR	10	-	ns
Ready to RE# Low		tRR	20	-	ns
Ready to WE# Falling Edge		tRW	20	-	ns
RE# Pulse Width		tRP	12	-	ns
WE# High to Busy		tWB	-	100	ns
WP# Low to WE# Low (disable mode)		tWW	100	-	ns
WP# High to WE# Low (enable mode)					
Read Cycle Time		tRC	25	-	ns
CE# Low to RE# Low		tCR	9	-	ns
RE# Access Time		tREA	-	20	ns
CE# Access Time		tCEA	-	25	ns
RE# High to Output Hi-Z		tRHZ	-	100	ns
CE# High to Output Hi-Z		tCHZ	-	30	ns
CLE High to Output Hi-Z		tCLHZ	-	30	ns
RE# High to Output Hold		tRHOH	15	-	ns
RE# Low to Output Hold		tRLOH	5		ns
CE# High to Output Hold		tCOH	15	-	ns
RE# High Hold Time		tREH	10	-	ns
Output Hi-Z to RE# Low		tIR	0	-	ns
RE# High to WE# Low		tRHW	100	-	ns
WE# High to CE# Low		tWHC	30	-	ns
WE# High to RE# Low		tWHR	60	-	ns
Device Resetting Time during…	Read	tRST	-	5	us
	Program		-	10	us
	Erase		-	250	us
	Ready		-	5	us
Cache Busy in Read Cache (following 31h and 3Fh)		tDCBSYR1 (tDCBSYR)	-	30	us
Busy time for Set OTP		tFEAT	-	1	us

6. TIMING DIAGRAMS

6.1 COMMAND/ADDRESS/DATA LATCH CYCLE

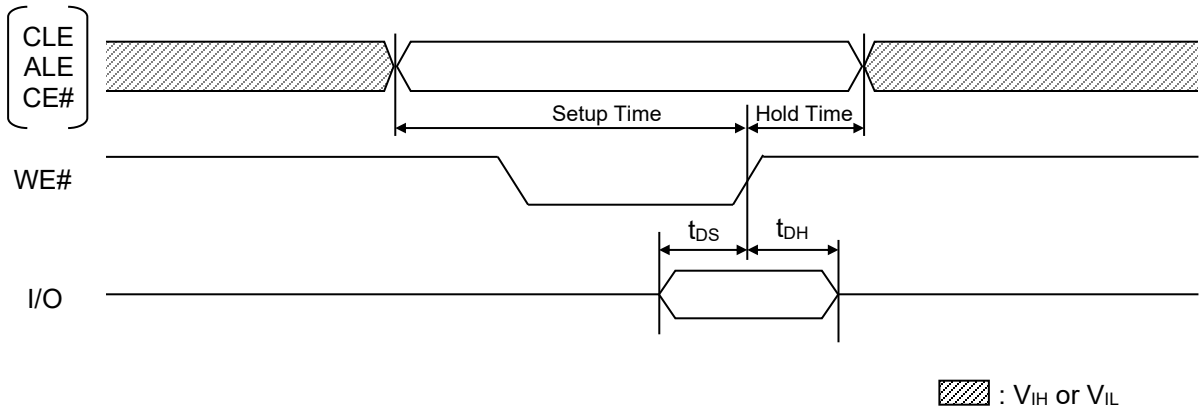


Figure 6.1 Command Latch Cycle

6.2 COMMAND INPUT CYCLE

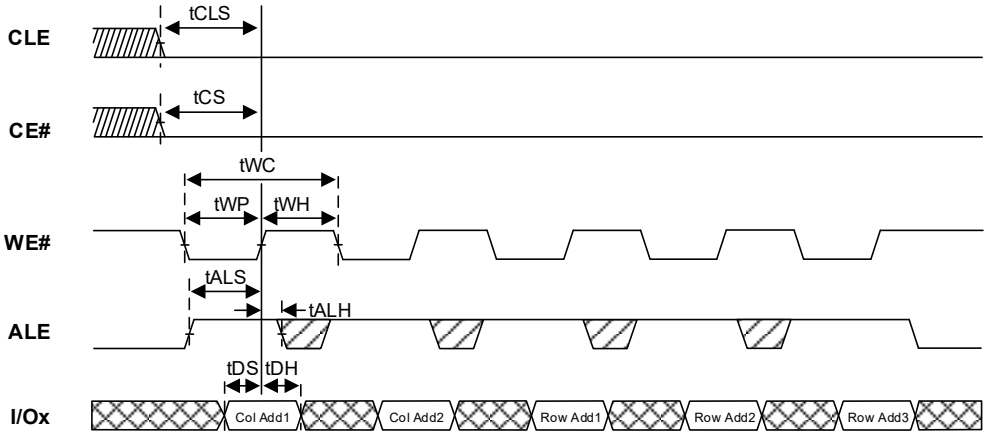


Figure 6.2 Command Input Cycle Timing

6.3 ADDRESS INPUT CYCLE

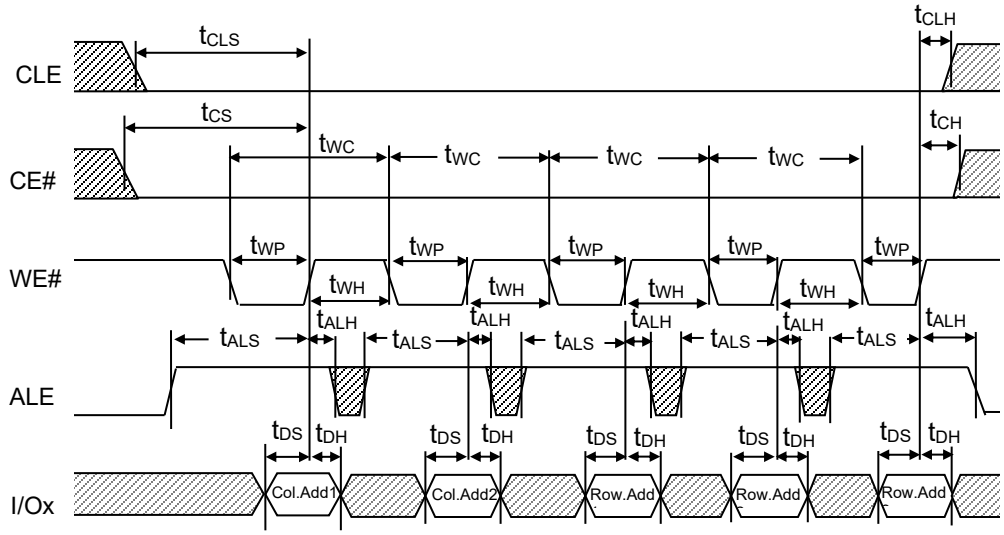
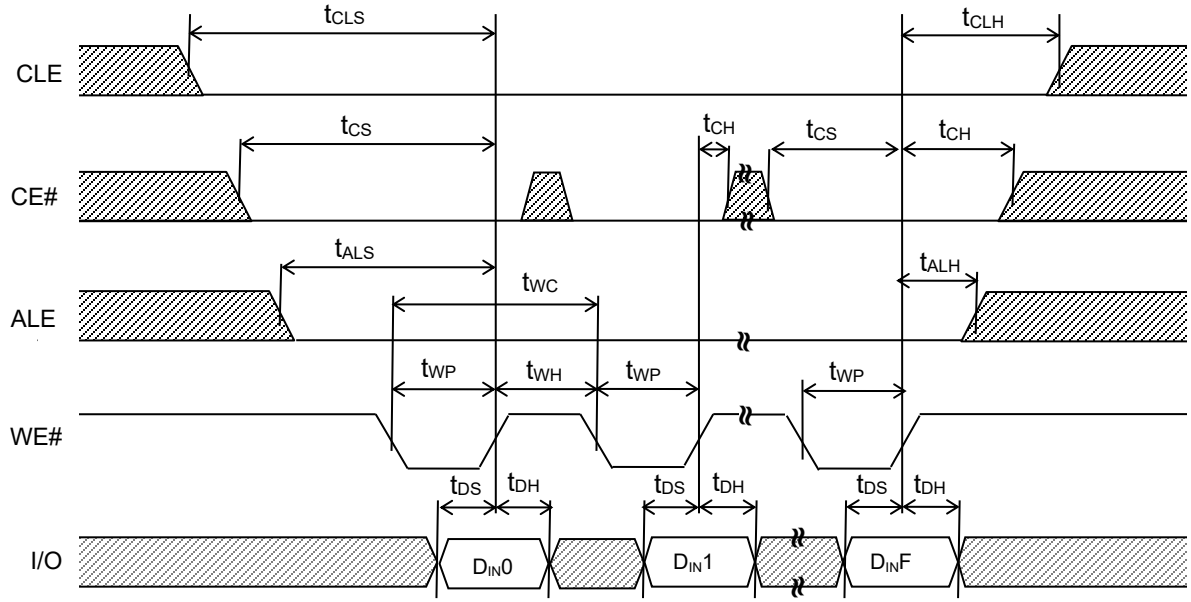


Figure 6.3 Address Input Cycle Timing

6.4 DATA INPUT CYCLE



Note:

1. DINF = DIN4319, DINF means the Final Data Input.

Figure 6.4 Data Input Cycle Timing

6.5 DATA OUT CYCLE

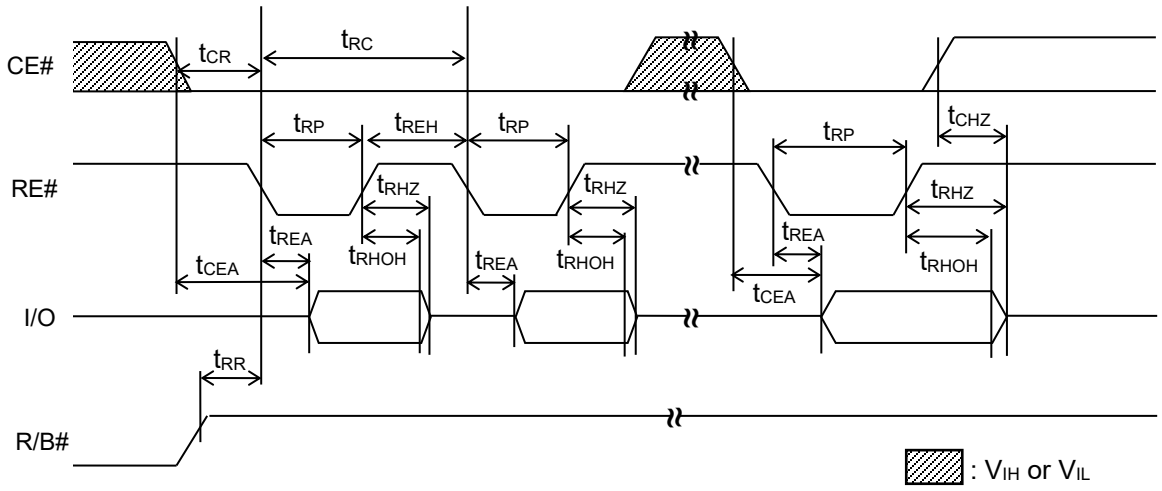


Figure 6.5 Data Output Cycle Timing

6.6 BASIC DATA OUTPUT

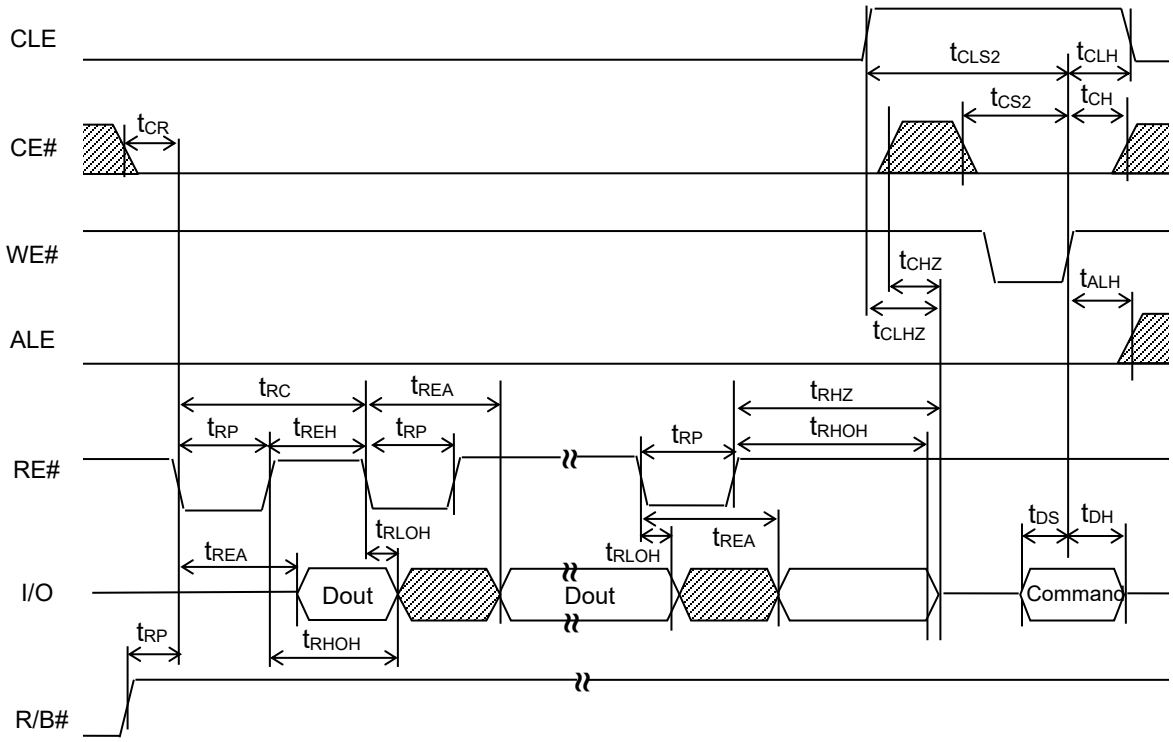


Figure 6.6 Status Read Cycle

6.7 READ ID

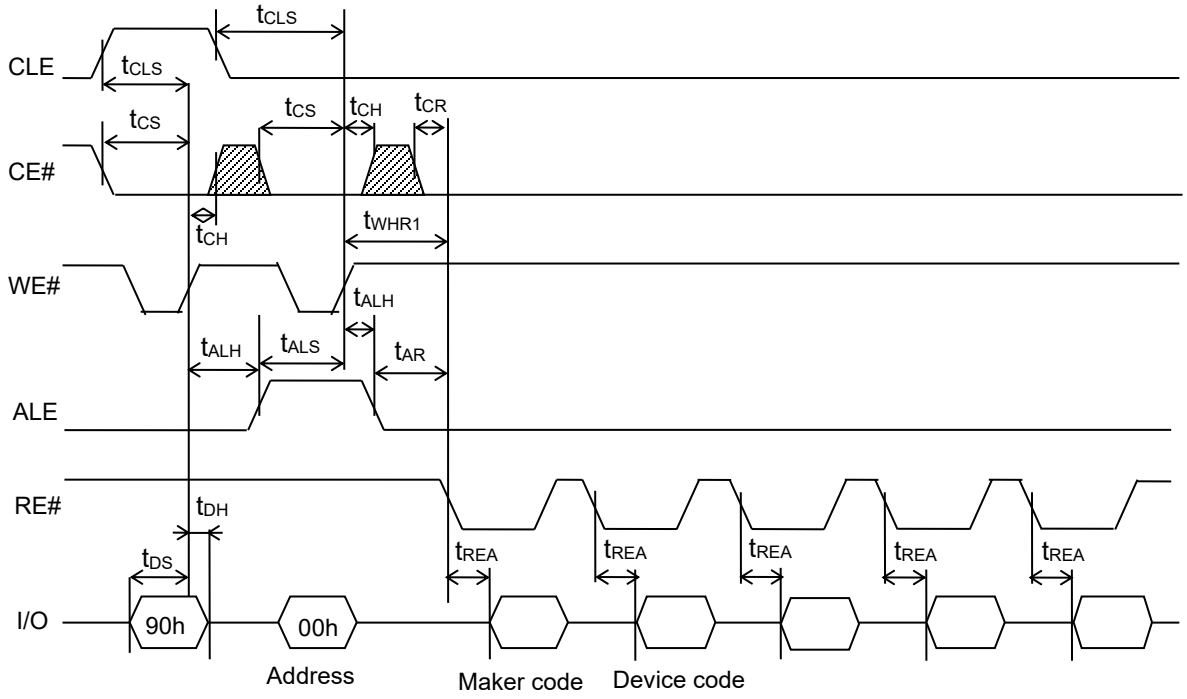


Figure 6.7 Read ID Operation Timing

6.8 STATUS READ CYCLE

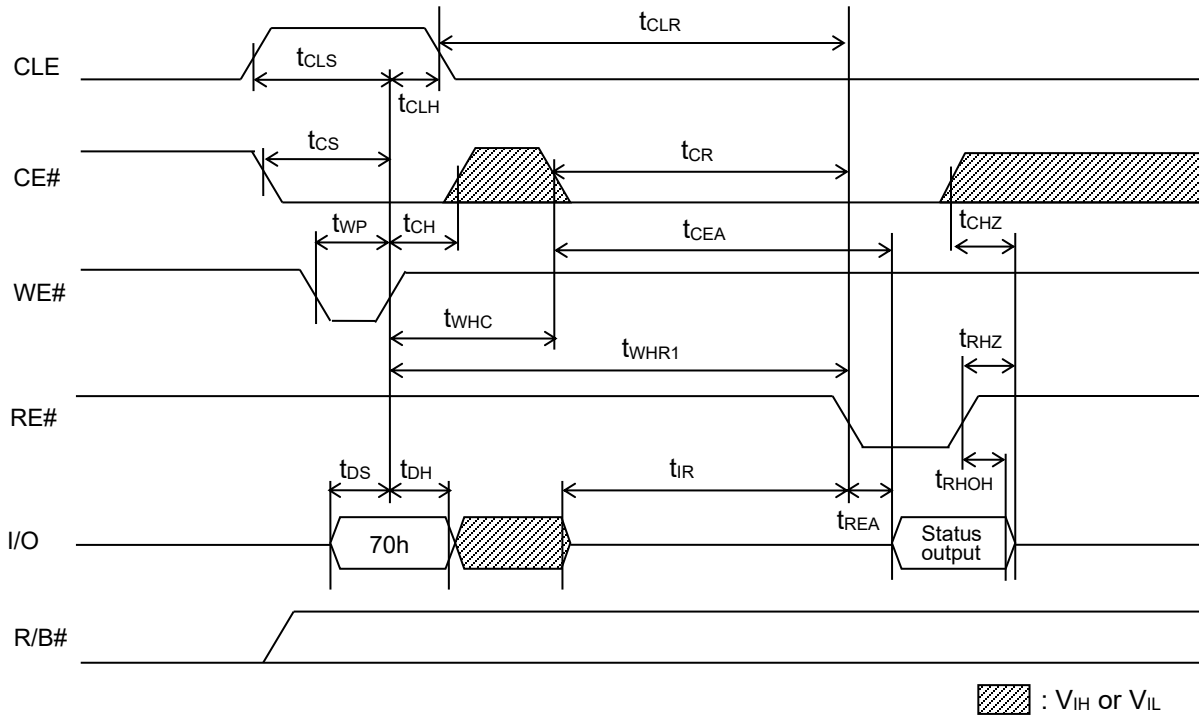


Figure 6.8 Status Read Cycle Timing

6.9 PAGE READ OPERATION

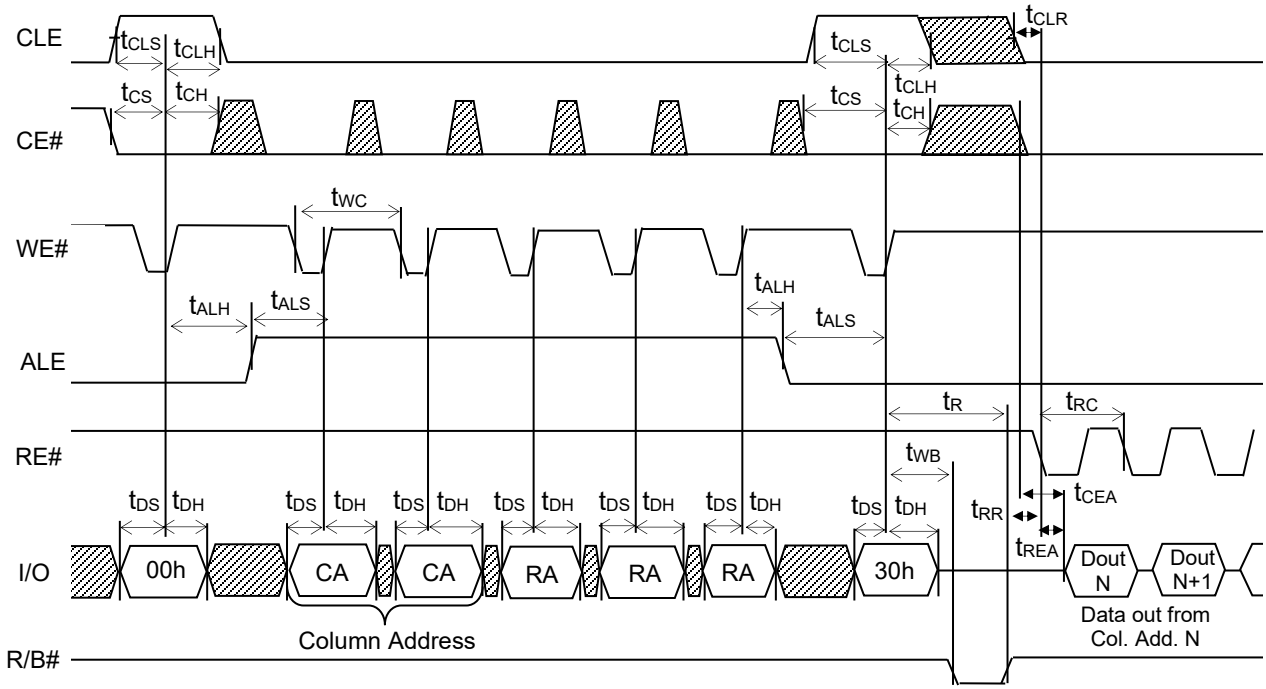


Figure 6.9 Page Read Operation Timing

6.10 PAGE PROGRAM OPERATION

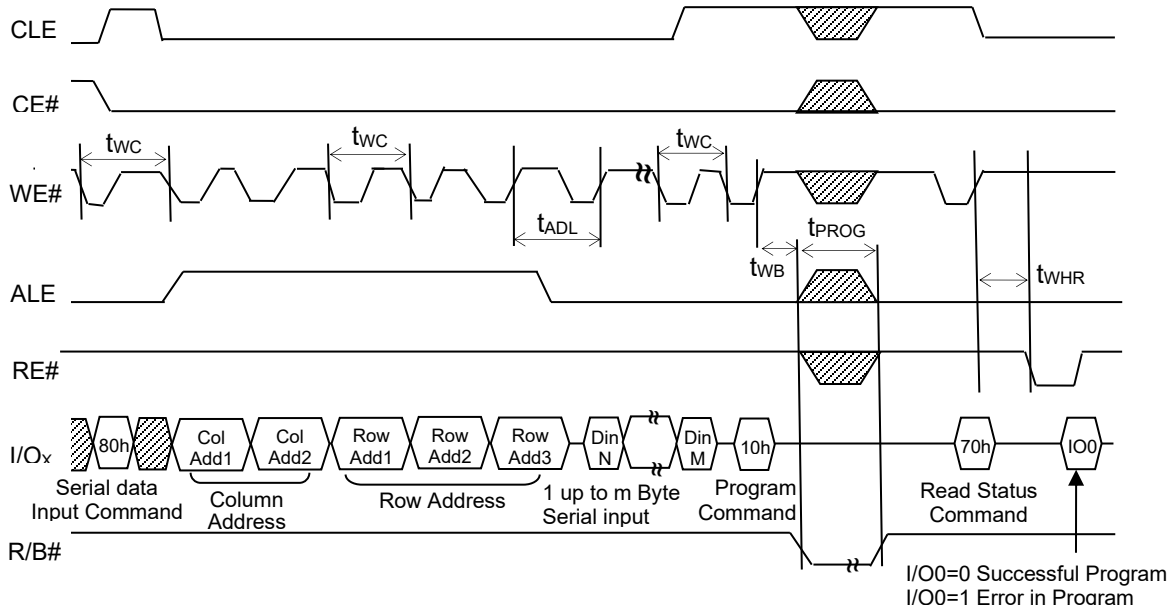


Figure 6.10 Page Program Operation

7. ID Definition Table and Parameter Data Structure

7.1 ID Definition Table

The READ ID (90h) command is used to read identifier codes programmed into the target. This command is accepted by the target only when the target is idle.

Writing 90h to the command register puts the target in read ID mode. The target stays in this mode until another valid command is issued.

When the 90h command is followed by a 00h address cycle, the target returns a 5-byte identification code that includes the manufacturer ID, device code and architecture information of the target.

When the 90h command is followed by a 20h address cycle, the target returns a 4-byte **ONFI** identification code.

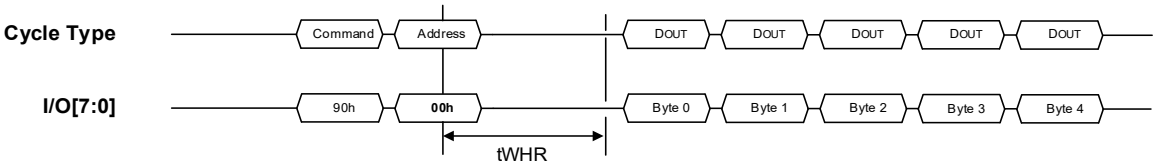


Figure 7.1 Read ID Operation (00h Address)

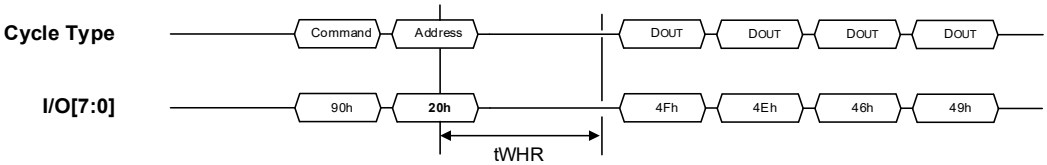


Figure 7.2 Read ID Operation (20h Address)

Table 7.1 ID Table (00h Address)

	Description	X8	X16
1st Byte	Maker Code	9Dh	9Dh
2nd Byte	Device Code	6Ch	ACh
3rd Byte	Internal Chip Number, Cell Type, etc	80h	80h
4th Byte	Page Size, Block Size, etc	19h	19h
5th Byte	Plane Number, ECC Level	30h	30h
6th Byte	Technology Code	40h	40h
7th Byte	JEDEC Maker Code Continuation Code	7Fh	7Fh
8th Byte	JEDEC Maker Code Continuation Code	7Fh	7Fh
9th Byte	JEDEC Maker Code Continuation Code	7Fh	7Fh
10th Byte	JEDEC Maker Code Continuation Code	7Fh	7Fh

2nd ID Data

Item	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Density	1Gb					0	0	0	1
	2Gb					1	0	1	0
	4Gb					1	1	0	0
	8Gb					0	0	1	1
	16Gb					0	1	0	1
Voltage	1.8V			0	1				
	3.3V			1	0				
Interface	SPI	0	0						
	X8	0	1						
	X16	1	0						

3rd ID Data

Item	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Internal Chip Number	1 2 4 8							0 0 1 1	0 1 0 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell					0 0 1 1	0 1 0 1		
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 1 1	0 1 0 1				
Interleave Program Between Multiple Chips	Not Support Support		0 1						
Cache Program	Not Support Support	0 1							

4th ID Data

Item	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Page Size	2KB							0	0
(w/o redundant area)	4KB							0	1
	8KB							1	0
	Reserved							1	1
Block Size	128KB	0		0	0				
(w/o redundant area)	256KB	0		0	1				
	512KB	0		1	0				
	1MB	0		1	1				
	Reserved	1		0	0				
	Reserved	1		0	1				
	Reserved	1		1	0				
	Reserved	1		1	1				
Redundant Area Size	Reserved		0			0	0		
(Byte / Page Size)	128B		0			0	1		
	256B		0			1	0		
	400B		0			1	1		
	436B		1			0	0		
	512B		1			0	1		
	640B		1			1	0		
	1KB		1			1	1		

5th ID Data

Item	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Plane Number	1					0	0	0	
	2					0	1	0	
	4					1	0	0	
	8					1	1	0	
	16					1	1	1	
ECC Level	1bit		0	0	0				
	2bit		0	0	1				
	4bit		0	1	0				
	8bit		0	1	1				
	12bit		1	0	0				
	24bit		1	0	1				
	40bit		1	1	0				
	60bit		1	1	1				
Reserved	Reserved	0							0

6th ID Data

Item	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Reserved	Reserved			0	0	0	0	0	0
	Reserved			0	0	0	0	0	1
	Reserved			0	0	0	0	1	0
	Reserved			0	0	0	0	1	1
	Reserved			0	0	0	1	0	0
	Reserved			0	0	0	1	0	1
	Reserved			0	0	0	1	1	0
	Reserved			0	0	0	1	1	1
EDO	Not Support		0						
	Support		1						
Interface	Conventional	0							
	Toggle	1							

7th ~ 10th ID Data

Item	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
JEDEC Maker Code Continuation Code	7Fh	0	1	1	1	1	1	1	1

Table 7.2 ID Table (20h Address)

The Users can read 4-byte **ONFI** identification code by command 90h followed by 20h address.

Item	Description	Value	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
1st Cycle	”O”	4Fh	0	1	0	0	1	1	1	1
2nd Cycle	”N”	4Eh	0	1	0	0	1	1	1	0
3rd Cycle	”F”	46h	0	1	0	0	0	1	1	0
4th Cycle	”I”	49h	0	1	0	0	1	0	0	1

7.2 Parameter Table

Read Parameter Page (ECh) command is used to read the ONFI parameter page programmed into the target. This command is accepted by the target only when the die(s) on the target is idle. Writing ECh to the command register puts the target in read parameter page mode. The target stays in this mode until another valid command is issued.

When ECh command is followed by one 00h address cycle, the target goes busy for tR. If the Read Status (70h) command is used to monitor for command completion, the Read mode (00h) command must be used to re-enable data output mode.

A minimum of three copies of the parameter page are stored in the device. Each parameter page is 256 bytes. Random Data Output (05h-E0h) can be used to change the location of data output.

The upper eight I/Os on X16 device are not used and are a “Don’t care” for X16 devices.

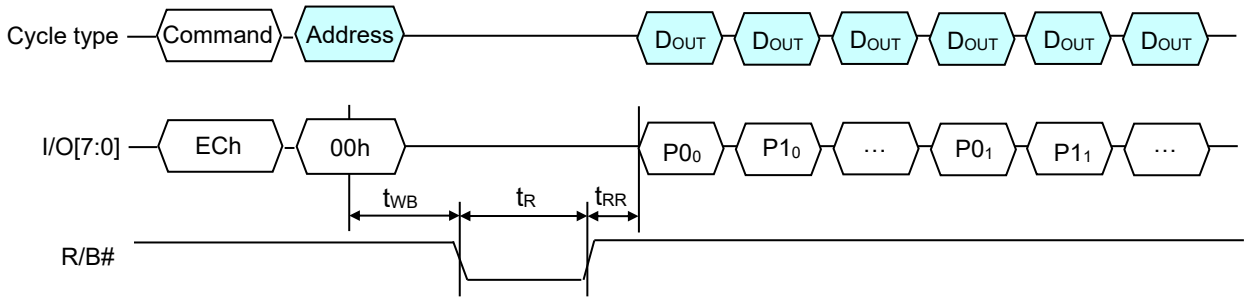


Figure 7.3 Read Parameter Operation Timing

Table 7.3 Parameter Table

Byte	Description		Value
0-3	Parameter page signature ("O", "N", "F", "I")		4Fh, 4Eh, 46h, 49h
4-5	Revision number		02h, 00h
6-7	Features supported	IS34/35ML04G088	10h, 00h
		IS34/35ML04G168	11h, 00h
8-9	Optional commands supported		33h, 00h
10-31	Reserved		All 00h
32-43	Device manufacturer (ISSI)		49h, 53h, 53h, 49h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
44-63	Device model	IS34ML04G088	49h, 53h, 33h, 34h, 4Dh, 4Ch, 30h, 34h, 47h, 30h, 38h, 38h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		IS34ML04G168	49h, 53h, 33h, 34h, 4Dh, 4Ch, 30h, 34h, 47h, 31h, 36h, 38h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID		9Dh
65-66	Date code		00h, 00h
67-79	Reserved		All 00h
80-83	Number of data bytes per page		00h, 10h, 00h, 00h
84-85	Number of spare bytes per page		00h, 01h
86-89	Number of data bytes per partial page		00h, 04h, 00h, 00h
90-91	Number of spare bytes per partial page		40h, 00h
92-95	Number of pages per block		40h, 00h, 00h, 00h
96-99	Number of blocks per unit		00h, 08h, 00h, 00h
100	Number of logical units		01h
101	Number of address cycles		23h
102	Number of bits per cell		01h
103-104	Number of maximum bad blocks per unit		28h, 00h
105-106	Block endurance		06h, 04h
107	Guaranteed valid blocks at beginning of target		01h
108-109	Block endurance of guaranteed valid blocks		00h, 00h
110	Number of partial programs per page		04h
111	Partial programming attributes		00h
112	Number of bits ECC		08h

Byte	Description	Value
113	Number of Interleaved address bits	00h
114	Interleaved operation attributes	00h
115-127	Reserved	All 00h
128	I/O pin capacitance	0Ah
129-130	Timing mode support (Reserved)	1Fh, 00h
131-132	Program cache timing mode support (Reserved)	1Fh, 00h
133-134	tPROG (max)	BCh, 02h
135-136	tBERS (max)	10h, 27h
137-138	tR (max)	19h, 00h
139-140	tCCS (min)	46h, 00h
141-163	Reserved	All 00h
164-165	Vendor-specific revision number	00h, 00h
166	Two-Plane Page Read support Bit[7:1]: Reserved (0) Bit 0: 0= Doesn't support Two Plane Page Read	00h
167	Read cache support Bit[7:1]: Reserved (0) Bit 0: 0= Doesn't support ONFI-specific read cache	01h
168	Read Unique ID support Bit[7:1]: Reserved (0) Bit 0: 0= Doesn't support ONFI-specific Read Unique ID	01h
169	Programmable output impedance support Bit[7:1]: Reserved (0) Bit 0: 0= Doesn't support programmable output impedance support	00h
170	Number of programmable output impedance support settings Bit[7:3]: Reserved (0) Bit[2:0]: Number of programmable IO output impedance settings	00h
171	Reserved	00h
172	Programmable R/B# pull-down strength support Bit[7:1]: Reserved (0) Bit 0: 0= Doesn't support programmable R/B# pull-down strength	00h
173	Reserved	00h

Byte	Description	Value
174	Number of programmable R/B# pull-down strength support Bit[7:3]: Reserved (0) Bit[2:0]: Number of programmable R/B# pull-down strength settings	00h
175	OTP mode support Bit[7:2]: Reserved (0) Bit 1: 0= Doesn't support Get/Set Feature command set Bit 0: 1= support OTP mode	01h
176	OTP page start Bit[7:0] = Page where OTP page space begins	00h
177	OTP Data Protect address Bit[7:0] = Page address to use when issuing OTP Data Protect command	00h
178	Number of OTP pages Bit[15:5]: Reserved (0) Bit[4:0] = Number of OTP pages	1Eh
179	OTP Feature Address	90h
180-253	Reserved	All 00h
254-255	Integrity CRC	Set at test
256-511	Values of bytes 0-255	Values of bytes 0-255
512-767	Values of bytes 0-255	Values of bytes 0-255
768+	Additional redundant parameter pages	

8. DEVICE OPERATION

8.1 PAGE READ OPERATION

The Page Read function reads a page of data identified by row address for the selected LUN. The page of data is made available to be read from the page register starting at the specified column address. Figure below defines the Page Read behavior and timings. Reading beyond the end of a page results in indeterminate values being returned to the host.

The Random Data Output function changes the column address from which data is being read in the page register for the selected LUN. The Random Data Output command shall only be issued when LUN is in a read idle condition. Figure below defines the Random Data Output behavior and timings. The host shall not read data from the LUN until t_{WHR}(ns) after the second command (i.e. E0h) is written to the LUN.

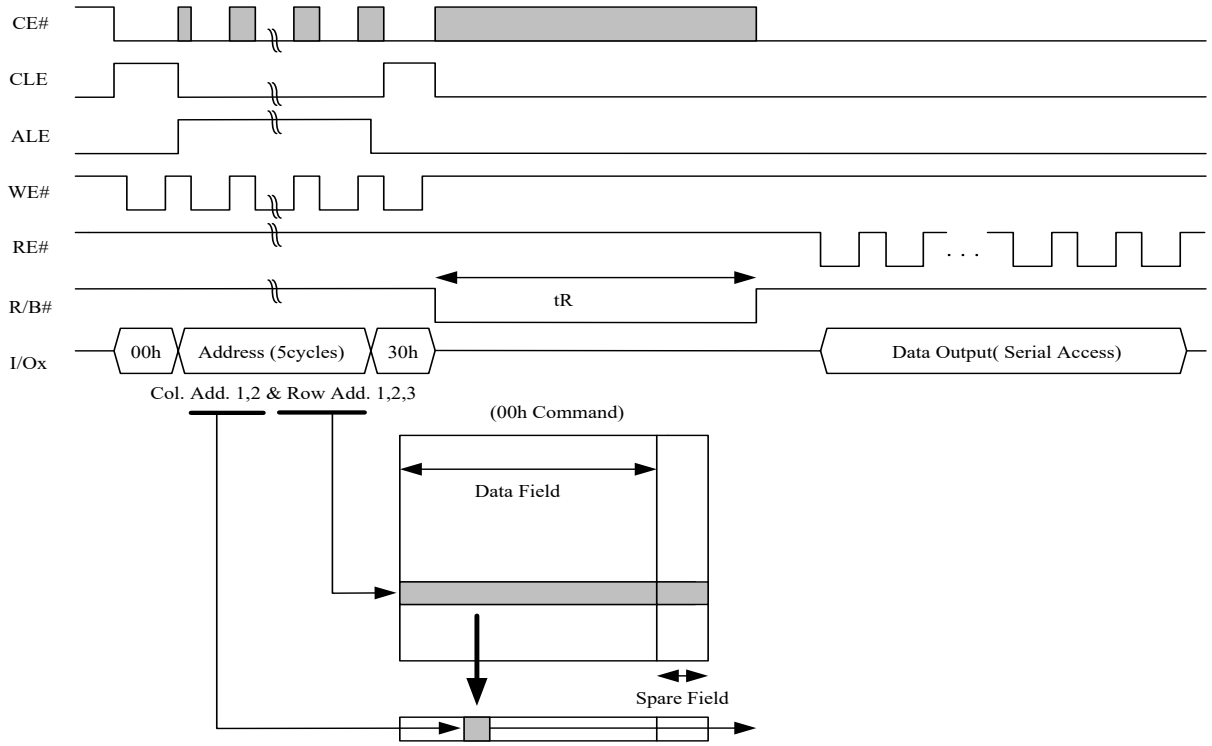


Figure 8.1 Read Operation

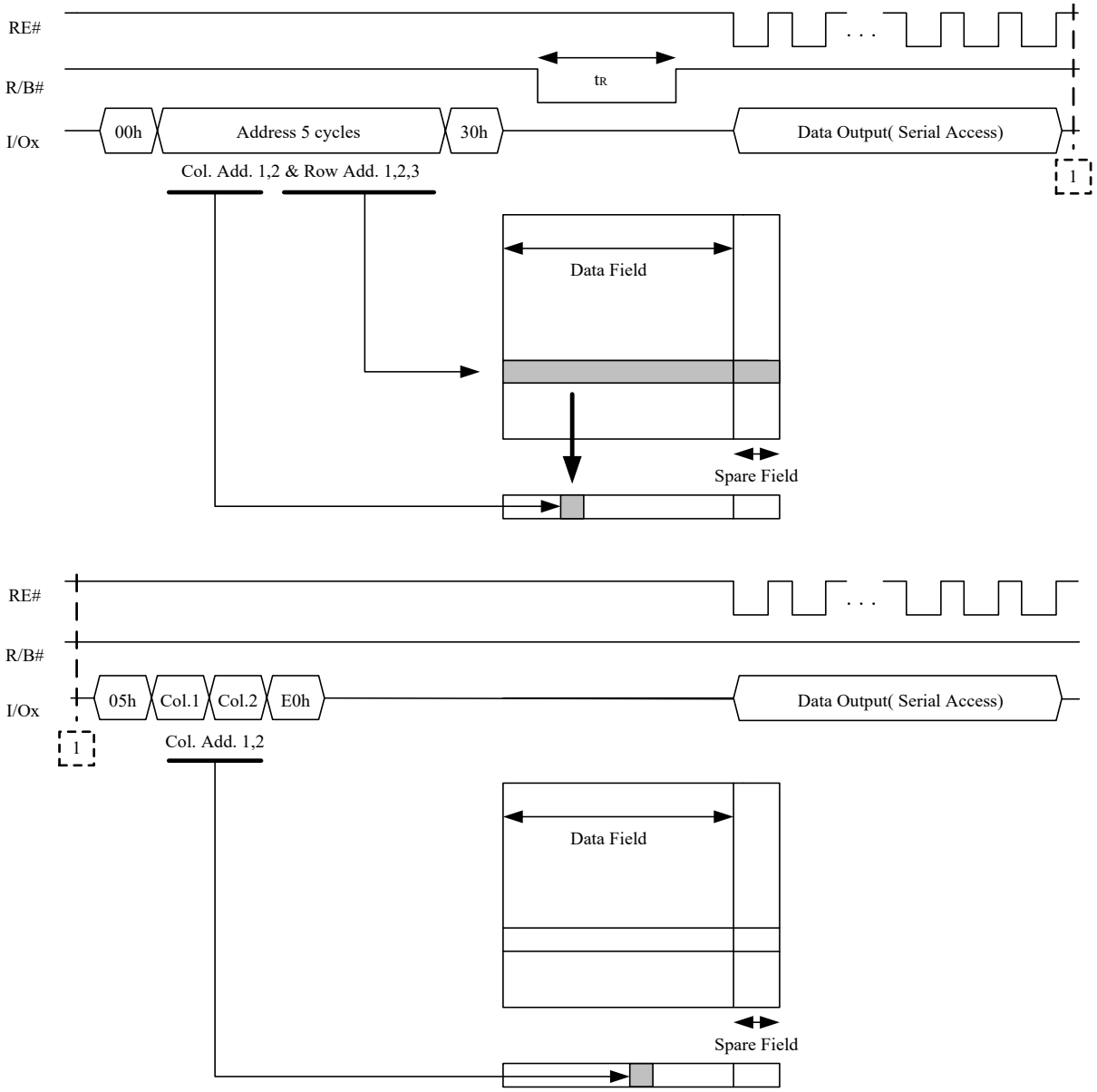
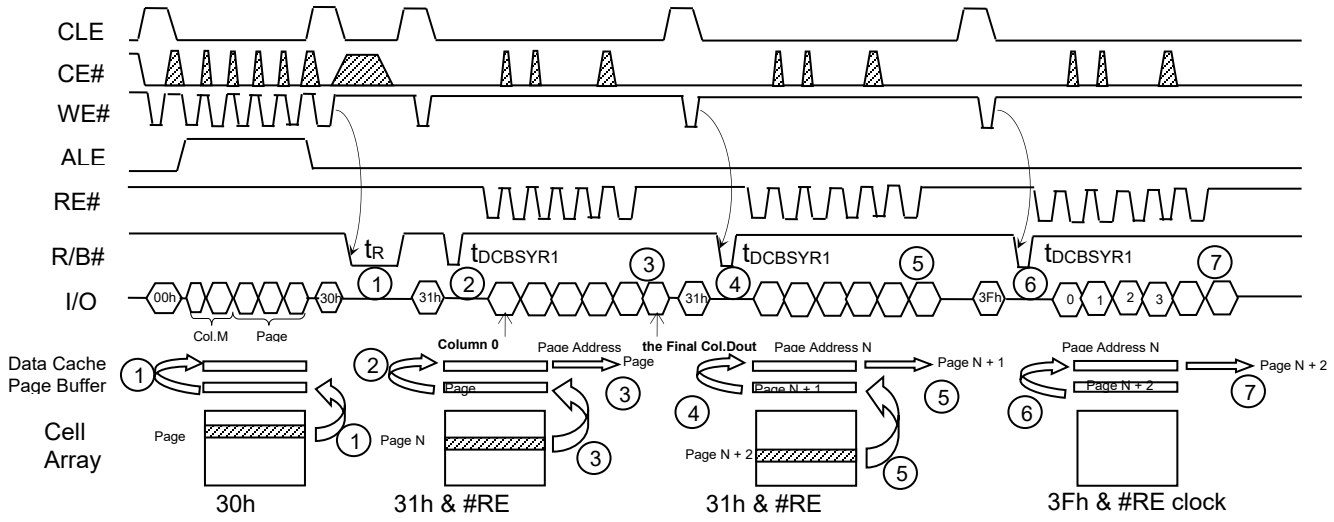


Figure 8.2 Random Page Operation

8.2 CACHE READ OPERATION

Cache Read is an extension of Page Read, and is available only within a block. The normal Page Read command (00h-30h) is always issued before invoking Cache Read. After issuing the Cache Read command (31h), read data of the designated page (page N) are transferred from data registers to cache registers in a short time period of t_{DCBSYR}, and then data of the next page (page N+1) is transferred to data registers while the data in the cache registers are being read out. Host controller can retrieve continuous data and achieve fast read performance by iterating Cache Read operation. The Read Start for Last Page Cache Read command (3Fh) is used to complete data transfer from memory cells to data registers.



If the 31th command is issued to the device, the data content of the next page is transferred to the Page Buffer during serial data out from the Data Cache, and therefore the tR (Data transfer from memory cell to data register) will be reduced.

1. Normal read. Data is transferred from Page N to Data cache through Page Buffer. During this time period, the device outputs Busy state for tR max.
2. After the Ready/Busy returns to Ready, 31h command is issued and data is transferred to Data Cache from Page Buffer again. This data transfer takes TDCBSYR1 max and the completion of this time period can be deleted by Ready/Busy signal.
3. Data of Page N + 1 is transferred to Page Buffer from cell while the data of Page N in Data Cache can be read out by /RE clock simultaneously.
4. The 31h command makes data of Page N + 1 transfer to Data Cache from Page Buffer after the completion of the transfer from cell to Page Buffer. The device outputs Busy state for tDCBSYR1 max.. This Busy period depends on the combination of the internal data transfer time from cell to Page Buffer and the serial data out time.
5. Data of Page N + 2 is transferred to Page Buffer from cell while the data of Page N + 1 in Data Cache can be read out by /RE clock simultaneously.
6. The 3Fh command makes the data of Page N + 2 transfer to the Data Cache from the Page Buffer after the completion of the transfer from cell to Page Buffer. The device outputs Busy state for tDCBSYR1 max.. This Busy period depends on the combination of the internal data transfer time from cell to Page Buffer and the serial data out time.
7. Data of Page N + 2 in Data Cache can be read out, but since the 3Fh command dose not transfer the data from the memory cell to Page Buffer, the device can accept new command input immediately after the completion of serial data out.

Figure 8.3 Cache Read Operation Timing

8.3 PAGE PROGRAM

The device is programmed basically on a page basis, and each page shall be programmed only one before being erased. The addressing order shall be sequential within a block. The contents of the page register are programmed into the Flash array specified by row address. After tPROG program time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after 10h.Figure below defines the Page Program behavior and timings. Writing beyond the end of the page register is undefined.

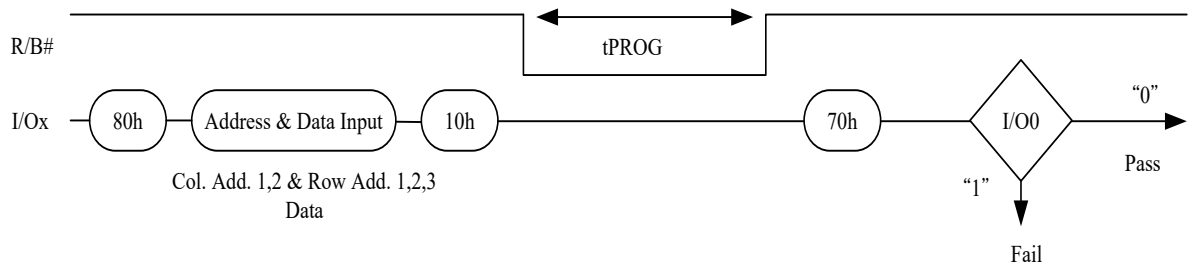


Figure 8.5 Program and Read Status Operation

The device supports random data input in a page. The column address for the next data, which will be written, may be changed to the address using Random Data Input command (i.e. 85h). Random data input may be operated multiple times without limitation.

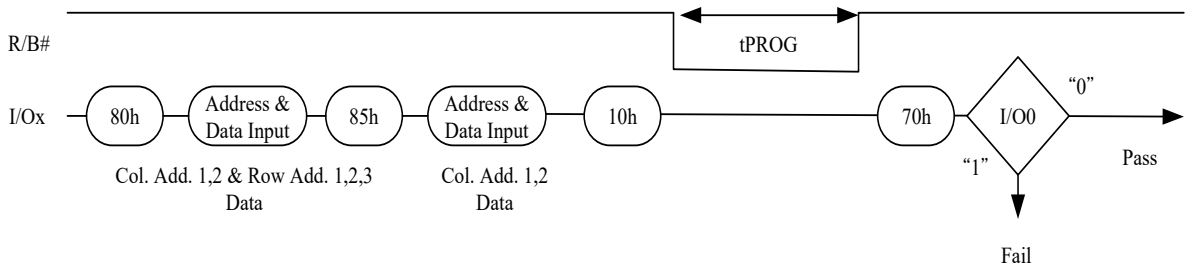


Figure 8.6 Random Data Input In a Page

8.4 CACHE PROGRAM

The Cache Program function allows the host to write the next data for another page to the page register while a page of data to be programmed to the Flash array for the selected LUN. When command 15h is issued, R/B# returns high (i.e. ready) when a cache register is ready to be written after data in the cache register is transferred to a page register. However, when command 10h is issued for the final page, R/B# turns to high after outstanding program operation performed by previous Cache Program command and the program operation for the final page is completed. SR[0] is valid for this command after SR[5] transitions from zero to one until the next transition. SR[1] is valid for this command after SR[6] transitions from zero to one, and it is invalid after the first Cache Program command completion since there is no previous Cache Program operation. Cache Program operation shall work only within a block. Figure below defines the Cache Program behavior and timings. Note that tPROG at the end of the caching operation may be longer than typical as this time also includes completing the programming operation for the previous page. Writing beyond the end of the page register is undefined.

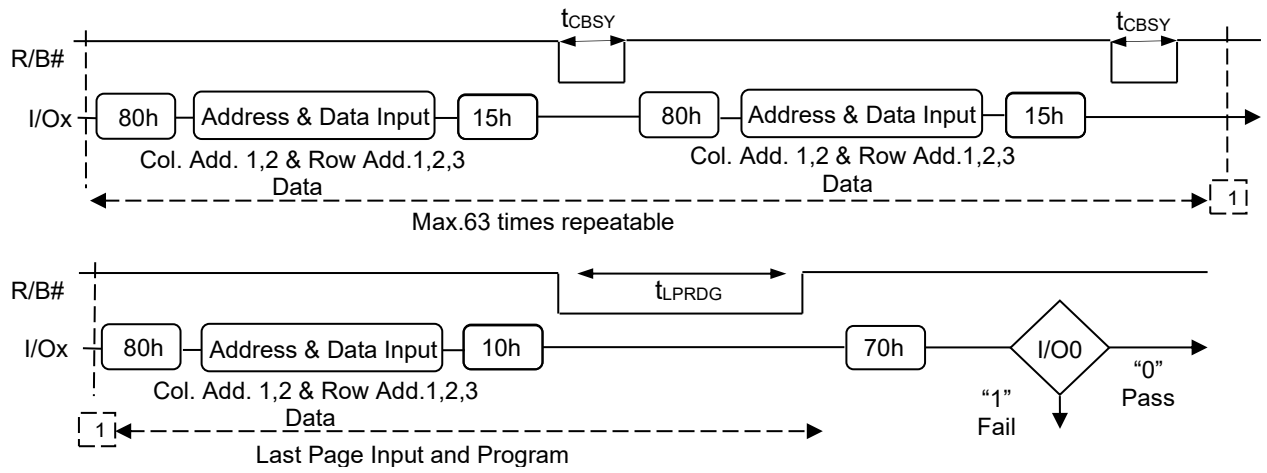


Figure 8.7 Cache Program

8.5 COPY-BACK PROGRAM

The Copy-Back Program with Read for Copy-Back is configured to efficiently rewrite data stored in a page without data re-loading when no error within the page is found. Since the time consuming re-loading cycles are removed, copy-back operation helps the system performance improve. The benefit is especially obvious when a part of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. A read operation with "35h" command and the address of the source page moves the whole 4,352-byte data into the internal data buffer. A bit error is checked by sequential reading the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register. When the Copy-Back Program is complete, the Write Status bit(I/O 0) may be checked. The Copy-Back operation consists of Read for Copy-Back and Copy-Back Program. A host reads a page of data from a source page using Read for Copy-Back and copies read data back to a destination page on the same LUN by Copy-Back Program command.

After a host completes to read data from a page register, the host may modify data using Random Data Input command if required. Figure below defines Copy-Back Program with Random Data Input behavior and timings.

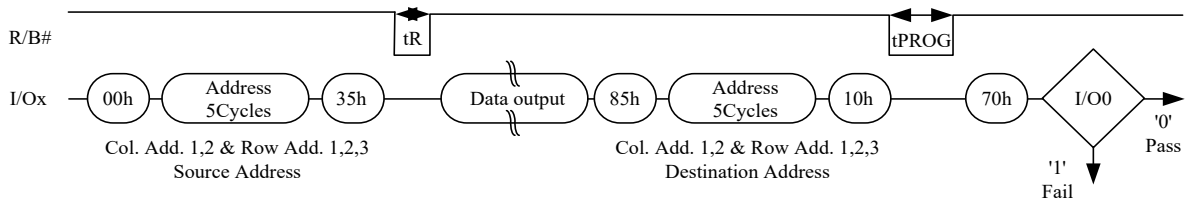


Figure 8.8 Page Copy-Back Program Operation

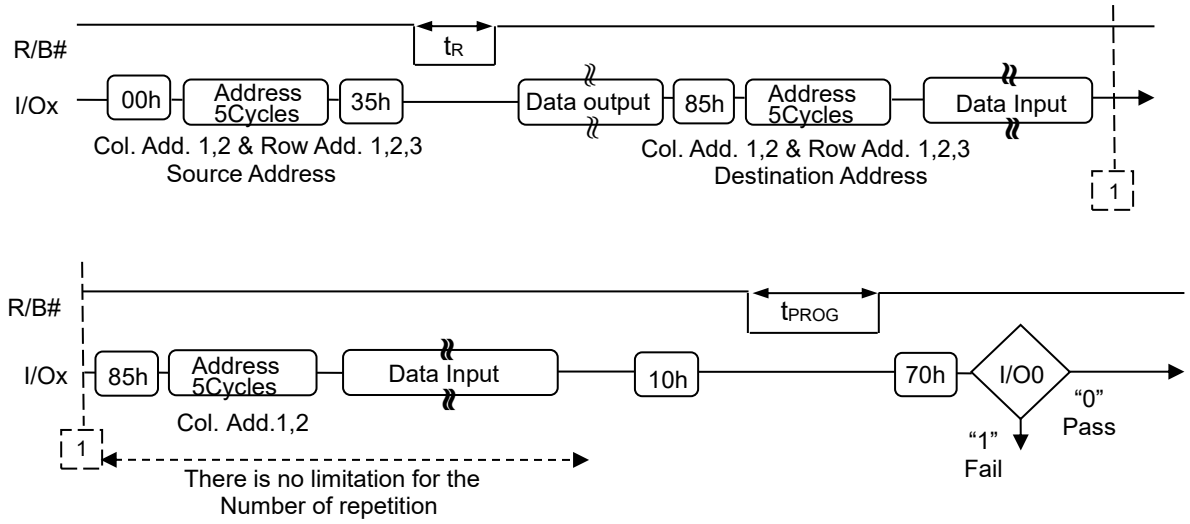


Figure 8.9 Page Copy-Back Program Operation with Random Data Input

8.6 BLOCK ERASE

The Block Erase operation is done on a block basis. Only three cycles of row addresses are required for Block Erase operation and a page address within the cycles is ignored while plane and block address are valid. After Block Erase operation passes, all bits in the block shall be set to one. SR[0] is valid for this command after SR[6] transitions from zero to one (i.e. the selected LUN is ready) until the LUN goes in busy state by a next command. Figure below defines the Block Erase behavior and timings.

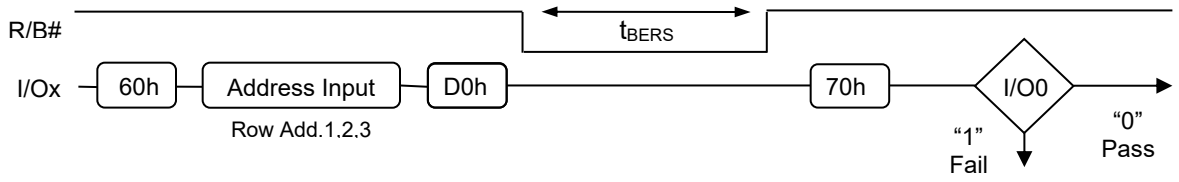


Figure 8.10 Block Erase Operation

8.7 READ STATUS

The Read Status function (command 70h) retrieves a status value for the last operation issued in the case of one-plane operations. 70h is followed without address setting. Specifically, Read Status return the combined status values of the independent status register bits according to Table below.

Table 8.1 Status Register Definition

	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
Definition	Pass: 0 Fail: 1	Pass: 0 Fail: 1	Reserved	Reserved	Reserved	Busy: 0 Ready: 1	Busy: 0 Ready: 1	Protected: 0 Not Protected: 1
Read	NA	NA	NA	NA	NA	NA	Busy/Ready	Write Protect
Cache Read	NA	NA	NA	NA	NA	Flash array Busy/Ready	Host Busy/Ready	Write Protect
Page Program	Pass/Fail	NA	NA	NA	NA	NA	Busy/Ready	Write Protect
Cache Program	Pass/Fail	(N-1) Pass/Fail	NA	NA	NA	Flash array Busy/Ready	Host Busy/Ready	Write Protect
Block Erase	Pass/Fail	NA	NA	NA	NA	NA	Busy/Ready	Write Protect

Notes:

1. During Block Erase, Page Program or Copy-Back operation, I/O0 is only valid when I/O6 shows the Ready state.
2. During Cache Program operation, I/O0 is only valid when I/O5 shows the Ready state, and I/O1 is only valid when I/O6 shows the Ready state.

8.8 RESET

The device offers a reset function by command FFh. When the device is in 'Busy' state during any operation, the Reset operation will abort these operations except during power-on when Reset shall not be issued until R/B# is set to one (i.e. ready). The contents of memory cells being programmed are no longer valid, as the data will be partially programmed or erased. Although the device is already in process of reset operation, a new Reset command will be accepted.

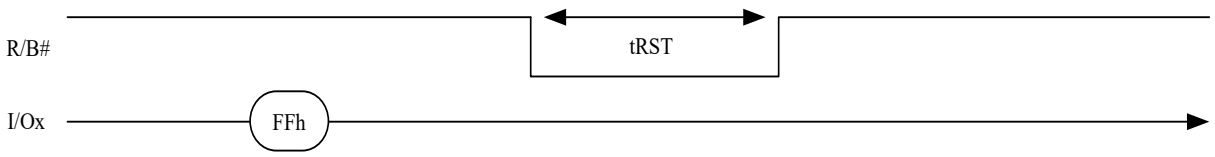


Figure 8.11 Reset Operation

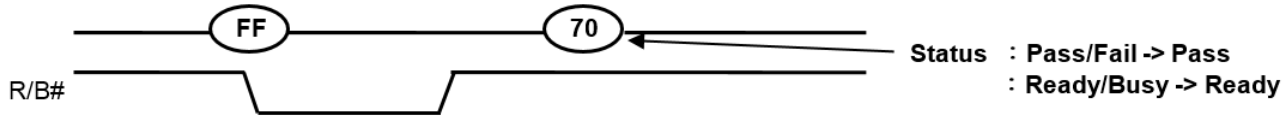


Figure 8.12 Status Read after Reset Operation

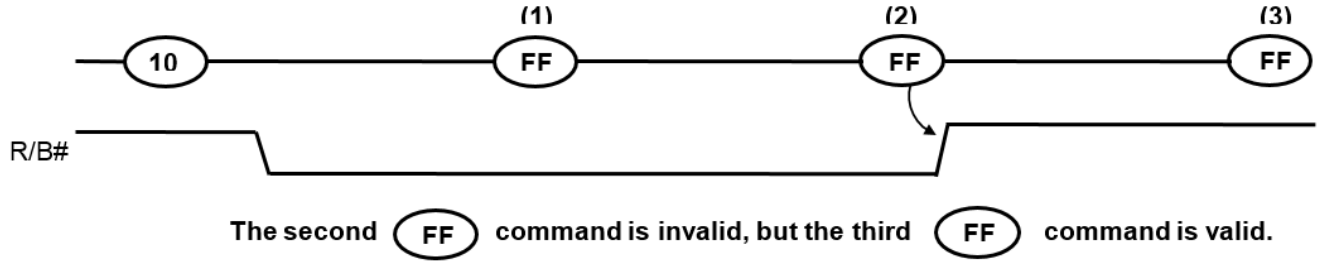
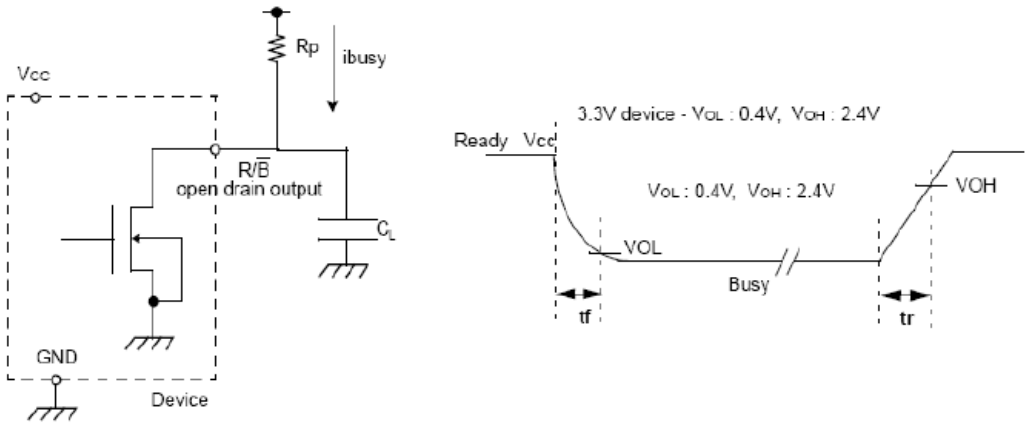


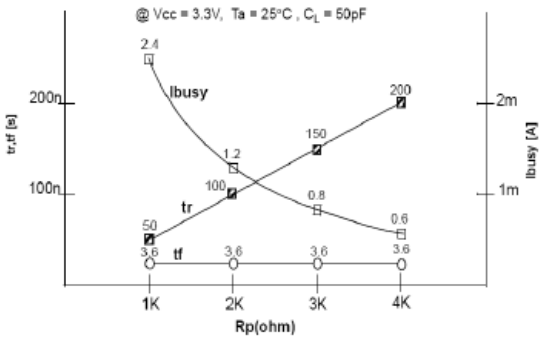
Figure 8.13 Successive Reset Operation

8.9 READY/BUSY#

The device has a R/B# output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/B# pin is normally high but transition to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because pull-up resistor value is related to tr(R/B#) and current drain during busy (ibusy), an appropriate value can be obtained with the following reference chart. Its value can be determined by the following guidance



R_P vs t_{RHOH} vs C_L



R_P value guidance

$$Rp(min, 3.3V\ part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

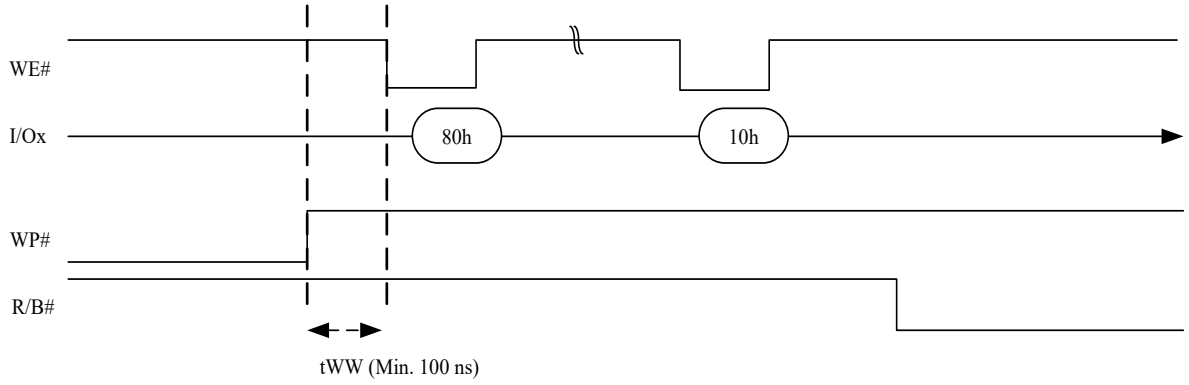
where I_L is the sum of the input currents of all devices tied to the R/B# pin.
R_P (max) is determined by maximum permissible limit of tr

Figure 8.14 Ready/Busy# Pin Electrical Specifications

8.10 WRITE PROTECT OPERATION

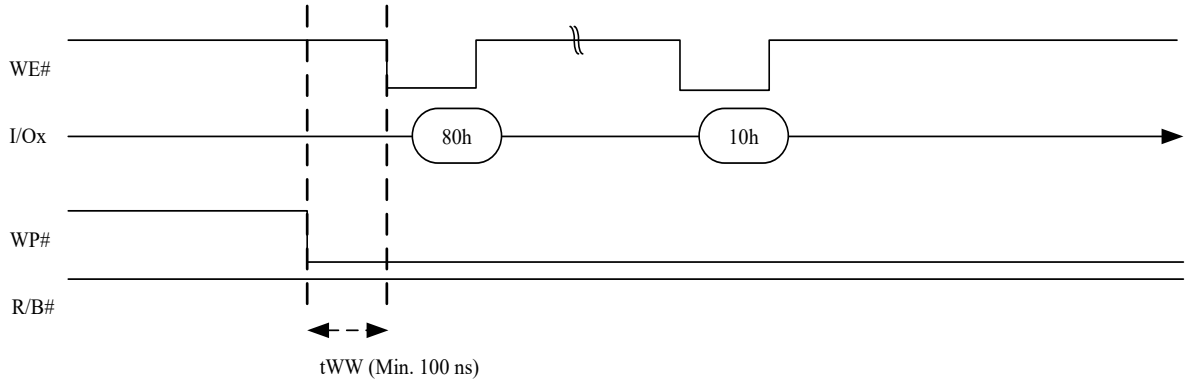
Enabling WP# during erase and program busy is prohibited. The erase and program operations are enabled and disabled as follows:

Enable Programming

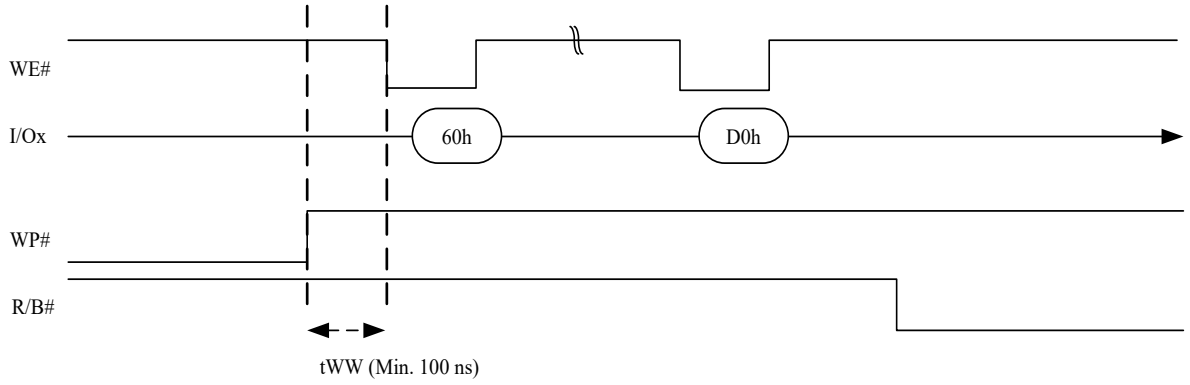


Note: WP# keeps “High” until programming finish

Disable Programming



Enable Erasing



NOTE: WP# keeps “High” until erasing finish

Disable Erasing

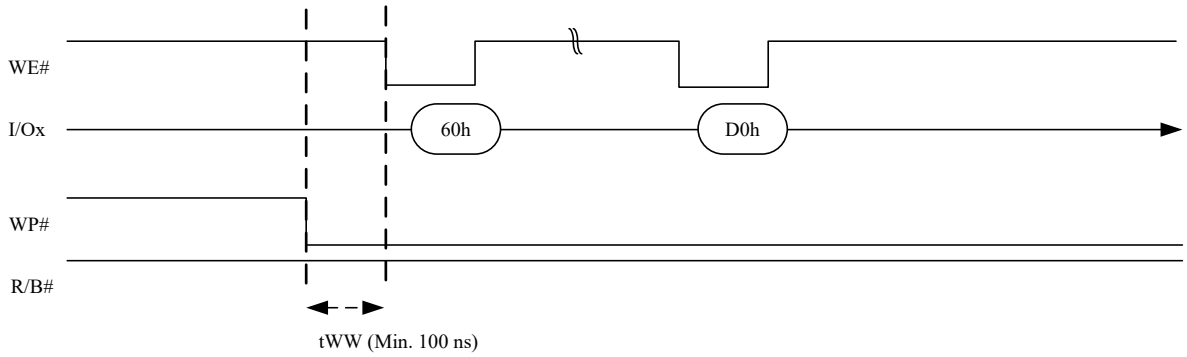


Figure 8.15 Enable/Disable Programming and Enable Erasing

8.11 READ PARAMETER PAGE OPERATION

Read Parameter Page (ECh) command is used to read the ONFI parameter page programmed into the target. This command is accepted by the target only when the die(s) on the target is idle. Writing ECh to the command register puts the target in read parameter page mode. The target stays in this mode until another valid command is issued.

When ECh command is followed by one 00h address cycle, the target goes busy for tR. If the Read Status (70h) command is used to monitor for command completion, the Read mode (00h) command must be used to re-enable data output mode.

A minimum of three copies of the parameter page are stored in the device. Each parameter page is 256 bytes. Random Data Output (05h-E0h) can be used to change the location of data output.

The upper eight I/Os on X16 device are not used and are a “Don’t care” for X16 devices.

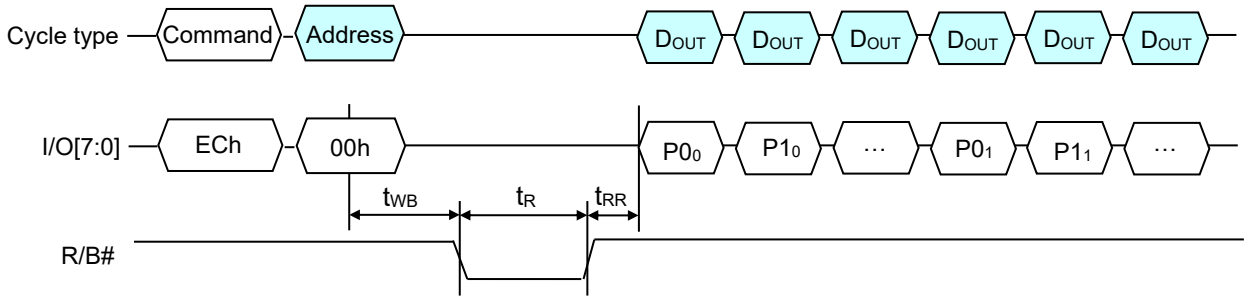


Figure 8.16 Enable/Disable Programming and Enable Erasing

8.12 READ UNIQUE ID OPERATION

Read Unique ID (EDh) command is used to read a unique identifier programmed into the target. This command is accepted by the target only when the die(s) on the target is idle. Writing EDh to the command register puts the target in read unique ID mode. The target stays in this mode until another valid command is issued.

When EDh command is followed by one 00h address cycle, the target goes busy for tR. If the Read Status (70h) command is used to monitor for command completion, the Read mode (00h) command must be used to re-enable data output mode. After tR completes, the host enables data output mode to read the unique ID.

Sixteen copies of the unique ID data are store in the device. Each copy is 32 bytes. The first 16 bytes of a 32-byte copy are unique ID data, and the second 16 bytes are the complement of the first 16 bytes of FFh, then that copy of the unique ID data is correct. In the event that a non-FFh result is returned, the host can repeat the XOR operation on a subsequent copy of the unique ID data. Random Data Output (05h-E0h) can be used to change the location of data output.

The upper eight I/Os on a X16 device are not used and are a “Don’t care” for X16 device

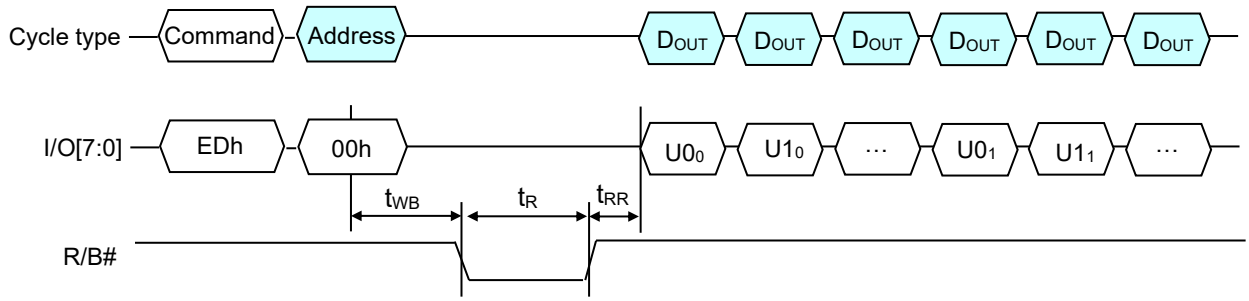


Figure 8.17 Read Unique ID Operation

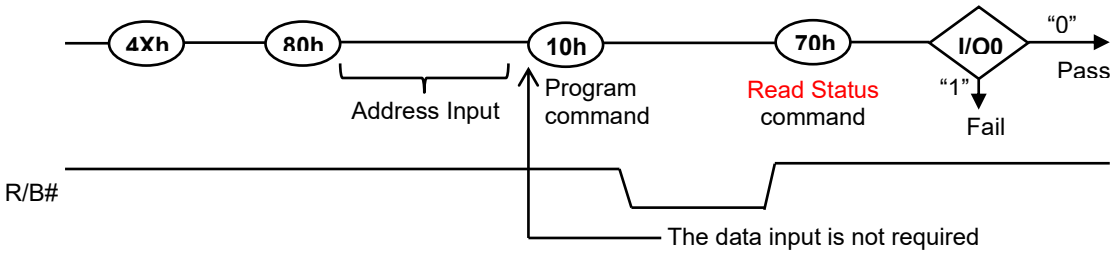
8.13 BLOCK PROTECTION

Block protection command prohibits both or one operation of programing and erasing for user blocks. Once set a prohibition of operation, setting is permanent. However, in the case of issuing the block erase command after the 41h command sequence, programming is no longer inhibited.

Table 8.2 Block Protection Command Set

Function	1st Set	Address cycles	2nd Set	Status read
Block protection - Prohibit both programming and erasing	43h – 80h	5	10h	70h
Block protection - Prohibit erasing	42h – 80h	5	10h	70h
Block protection - Prohibit programming	41h – 80h	5	10h	70h
Block protection status read	00h	5	34h	74h

Notes:
1) In the case of issuing 41h command sequence after 42h command sequence, both programming and erasing are prohibited.
2) In the case of issuing 42h command sequence after 41h command sequence, both programming and erasing are prohibited.
3) In the case of issuing 41h or 42h command sequence after 43h command sequence, both programming and erasing are prohibited.
4) In the case of issuing the block erase command after the 41h command sequence, programming is no longer inhibited.
5) One block protection command issue is counted as one partial program cycle in the block.



Notes:
1) 43h, 42h or 41h is issue in 4xh in the sequence
2) Block address is required for address input. 00h is required for column address and page address.

Figure 8.18 Block Protection Command Sequence

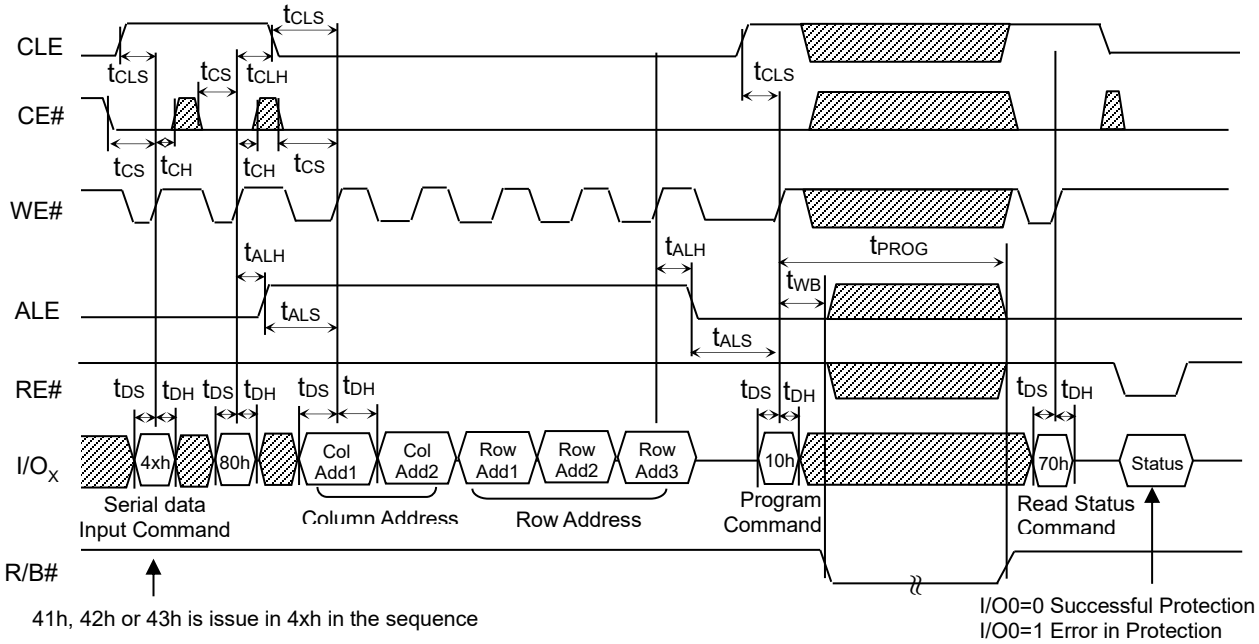


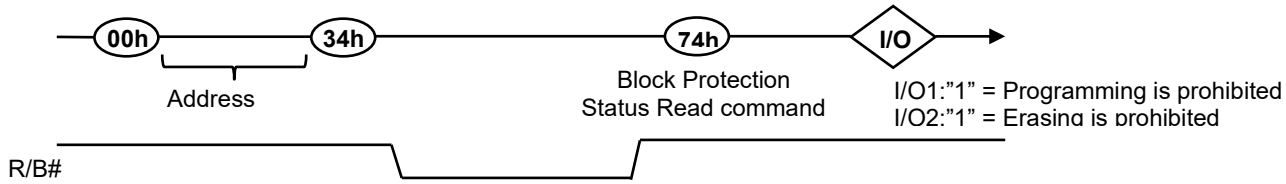
Figure 8.19 Block Protection Operation Timing

8.14 BLOCK PROTECTION STATUS READ

The block protection status for each block is output via the I/O port using after a “74h” command input. The resulting information is outlined in below table.

Table 8.3 Status Block Protection Status Output

	Definition	Block Protection
I/O0	Programming Permission: 0 Prohibition: 1	Permission / Prohibition
I/O1	Erasing Permission: 0 Prohibition: 1	Permission / Prohibition
I/O2	Not Used	Invalid
I/O3	Not Used	Invalid
I/O4	Not Used	Invalid
I/O5	Not Used	Invalid
I/O6	Not Used	Invalid
I/O7	Not Used	Invalid



Note:

1. Block address is required for address input. 00h is required for column address and page address cycle.

Figure 8.20 Block Protection Status Read Command Sequence

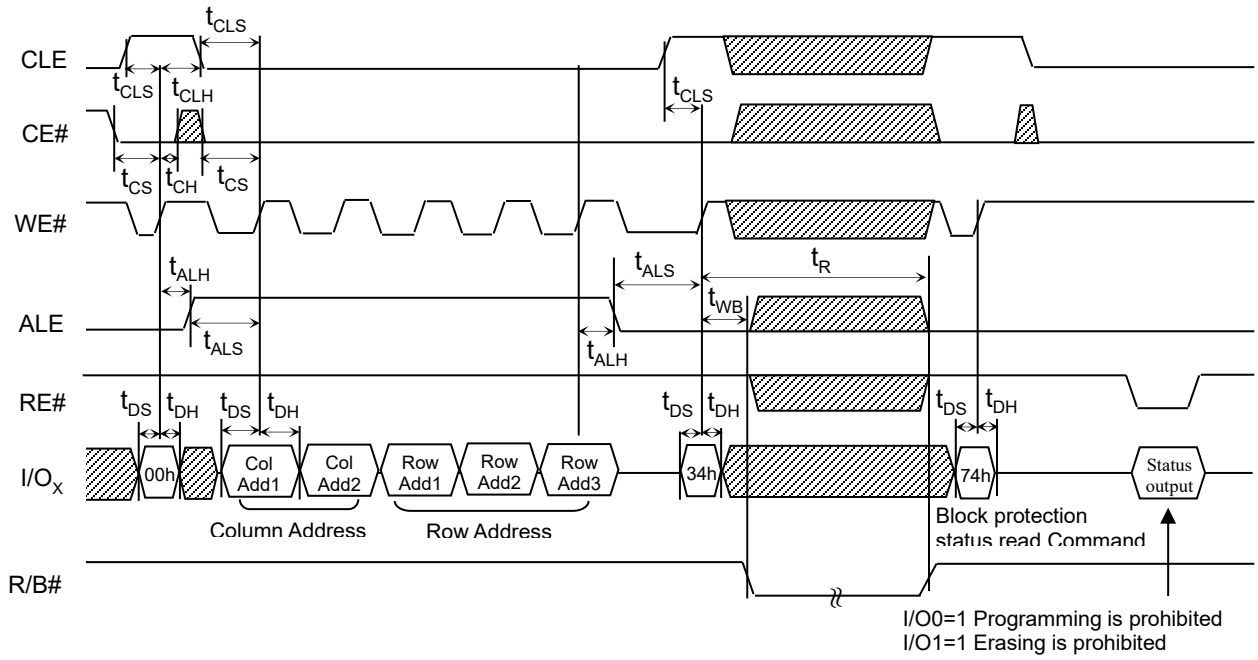
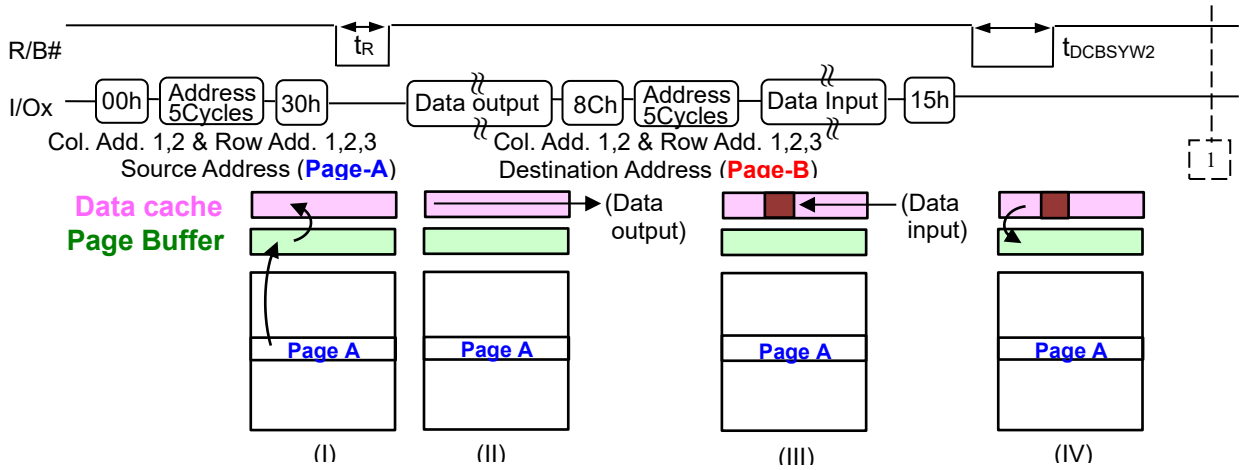


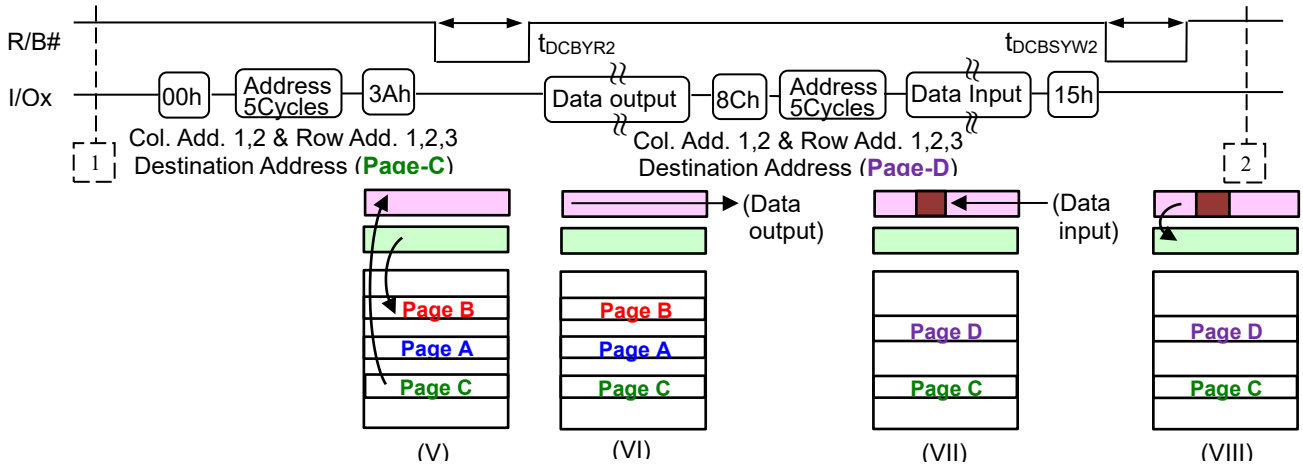
Figure 8.21 Block Protection Status Read Operation Timing

8.15 PAGE COPY

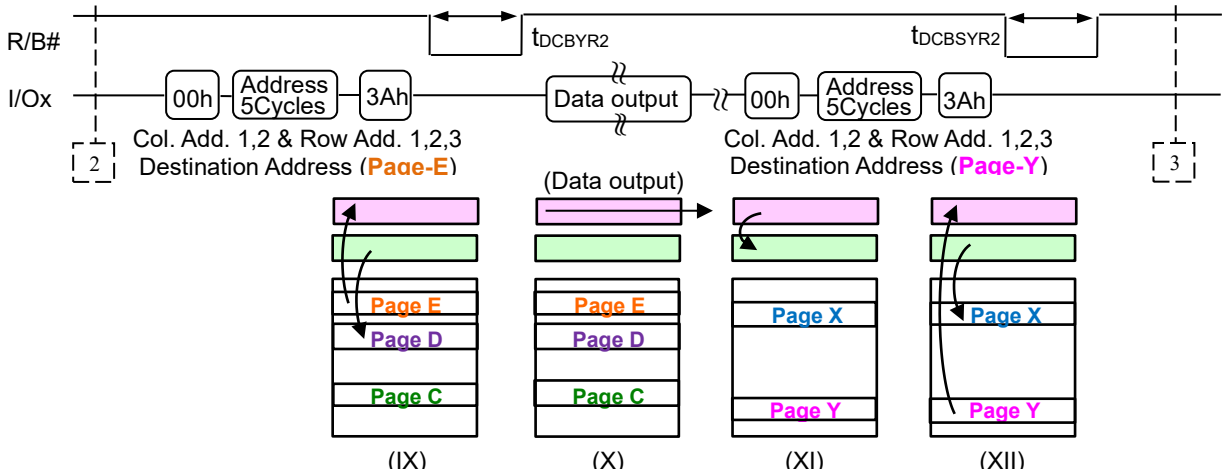
By using Page Copy, data in a page can be copied to another page after the data has been read out. When the block address changes (increments) this sequenced has to be started from the beginning.



I. Data for Page A is transferred to the Data Cache
II. Data for Page A is read out
III. Copy Page address B is input and if the data needs to be changed, changed data is input
IV. Data Cache for Page B is transferred to the Page Buffer



V. Data for Page C is transferred to Data Cache while the data of Page B is being programmed
VI. After the Ready state, Data for Page C is output from the Data Cache
VII. Copy Page address D is input and if the data needs to be changed, changed data is input
VIII. After programming of page B is completed, Data Cache for Page D is transferred to the Page Buffer

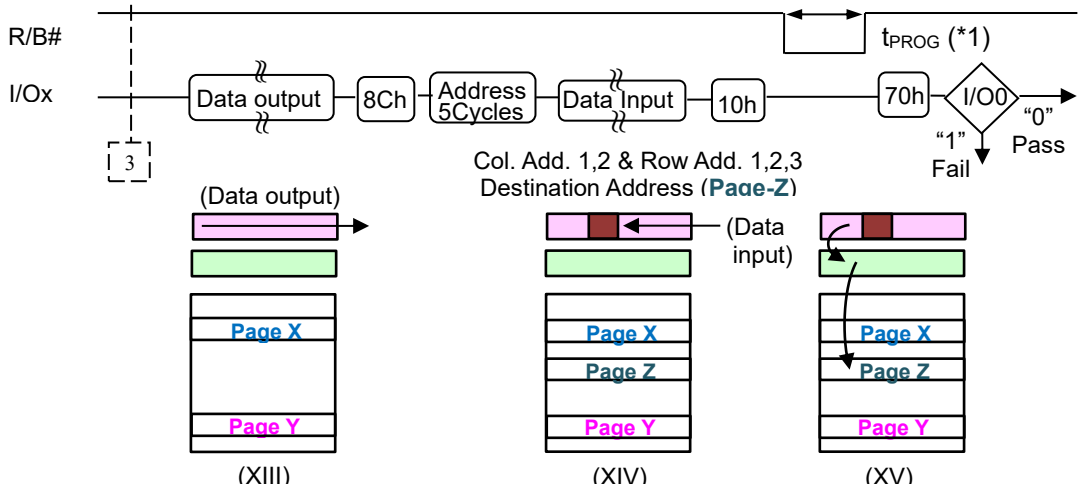


IX. By the 15h command, the data in the Page Buffer is programmed to Page D. Data for Page E is transferred to the Data cache

X. Data for Page E is read out

XI. Data Cache for Page X is transferred to the Page Buffer

XII. The data in the Page Buffer is programmed to Page X. Data for Page Y is transferred to the Data Cache



XIII. After the Ready state, Data for Page Y is output from the Data Cache

XIV. Copy Page address Z is input and if the data needs to be changed, changed data is input

XV. By issuing the 10h command, the data in the Page Buffer is programmed to Page Z

(*1) Since the last page programming by the 10h command is initiated after the previous cache program, the tLPROG here will be expected as the following, tLPROG = tLPROG of the last page + tLPROG of the previous page - (command input cycle + address input cycle + data output/input cycle time of the last page)

NOTE) This operation needs to be executed within Plane-0 or Plane-1.

Data input is required only if previous data output needs to be altered.
If the data has to be changed, locate the desired address with the column and page address input after the 8Ch command, and change only the data that needs be changed.
If the data does not have to be changed, data input cycles are not required.

Make sure WP is held to High level when Page Copy operation is performed.
Also make sure the Page Copy operation is terminated with 8Ch-10h command sequence

8.16 SET FEATURES FOR OTP OPERATION MODE SETTING

To set the device to OTP operation mode, issue SET FEATURE (EFh) command to the feature address of 90h and write 00h or 01h or 03h to the subfeature parameter W-B0, followed by three cycles of 00h to W-B1, W-B2 and W-B3.

Table 8.4 Feature Address 90h –OTP Operation Mode

Set Feature EFh-90h			W-B0 Data Bits								W-B0	W-B1	W-B2	W-B3	
OPT Mode	Option	Command Operation	7	6	5	4	3	2	1	0	Value				Command
	OTP Operation Mode	Read	0	0	0	0	0	0	0	1	01h	00h	00h	00h	00h-30h
		Page Porgram	0	0	0	0	0	0	0	1	01h	00h	00h	00h	80h-10h
		Data Program with Random Data Input	0	0	0	0	0	0	0	1	01h	00h	00h	00h	80h-85h-10h
	OTP Protection Mode	Program Protect	0	0	0	0	0	0	1	1	03h	00h	00h	00h	80h-10h
	OTP Release Mode	Leave OTP Mode	0	0	0	0	0	0	0	0	00h	00h	00h	00h	-

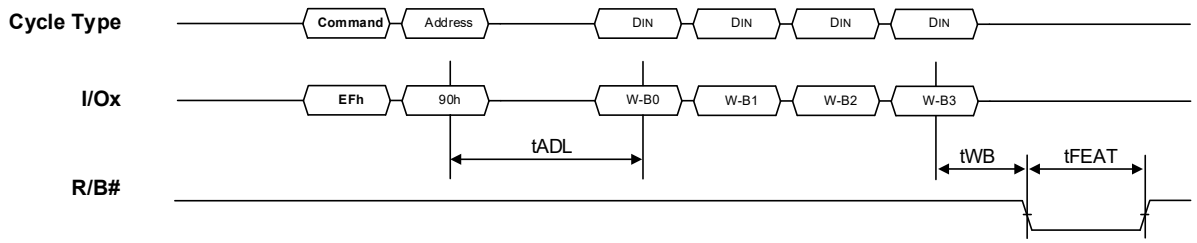


Figure 8.22 Set Features (EFh-90h) for OTP Mode Setting

8.17 ONE-TIME PROGRAMMABLE (OTP) OPERATIONS

The device offers one-time programmable memory area. Thirty full pages of OTP data are available on the device, and the entire range is guaranteed to be good.

The default values of OTP area are all “1” in the unwritten state (all bits are 1s). After the OTP programming, the written values in the OTP area cannot be erased, whether it is protected or not.

	Value
Number of OTP Pages	30
OTP Page Address	00h-1Dh
Number of Partial Page Program for each page in the OTP area	1

8.17.1 OTP PROGRAM (80h-10h)

To program an OTP page, issues the Serial Data Input (80h) command followed by 5 address cycles. The first two address cycles are column address. For the third cycle, select a page in the range of 00h through 1Dh. The fourth and fifth cycle is fixed at 00h. Next, in the sequential order and up to 4,352bytes of data can be loaded into data register. After data input is complete, issue the 10h command.
Read Status command (70h) can be issued to read the status register after 10h to monitor command completion. Please note that no partial-page program is allowed in the OTP area.

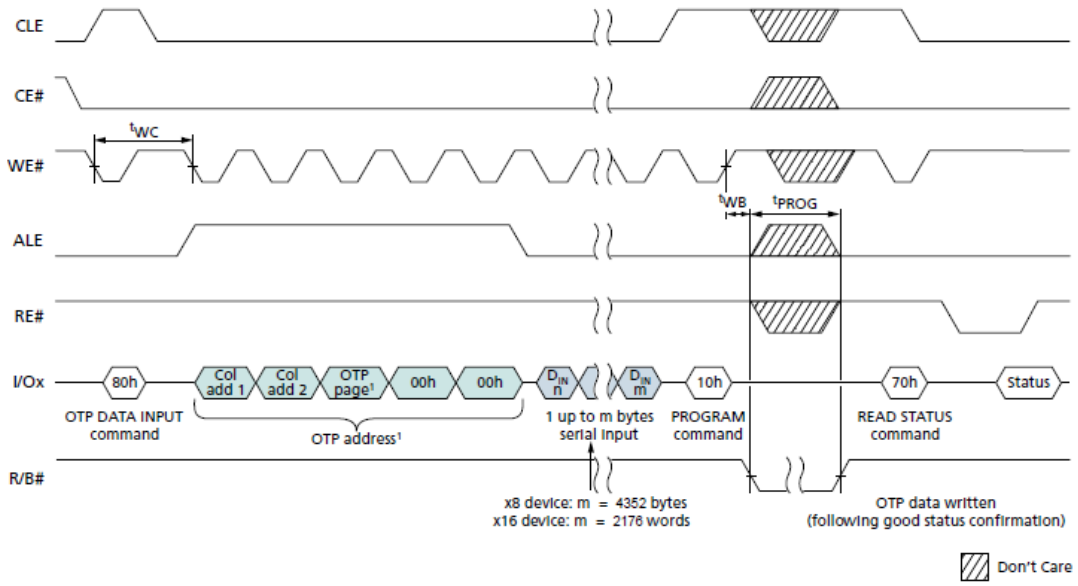


Figure 8.23 OTP Page Program (After Set Feature of OTP Operation Mode)

8.17.2 OTP Page PROGRAM with Random Data Input (85h)

The device supports Random Data Input (85h) command, which can be operated multiple times in a page. The column address for the next data to be entered may be changed to a new column address with the Random Data Input (85h) command.

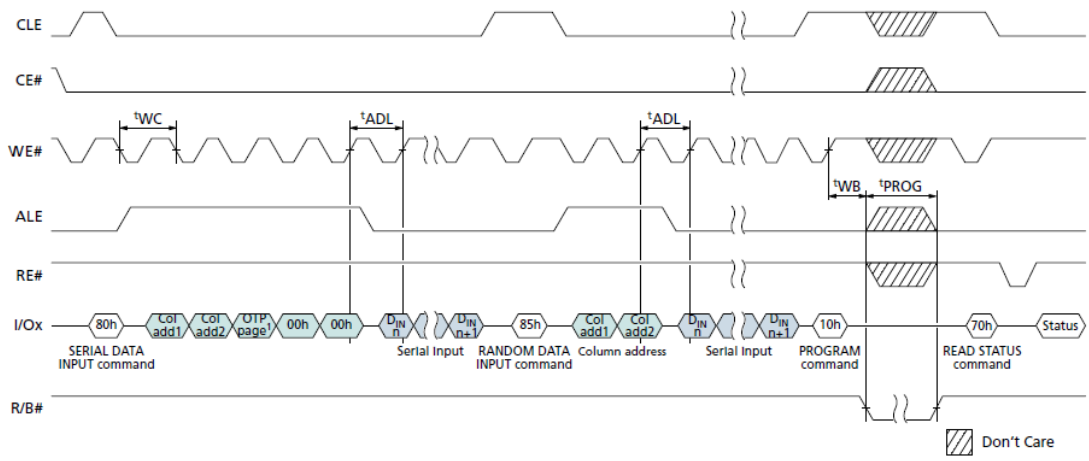


Figure 8.24 OTP Page Program with Random Data Input

8.17.3 OTP READ (00h-30h)

To read data from an OTP page, set the device to OTP operation mode and then issue the Read (00h-30h) command. After OTP operation mode is set, issue 00h command, and then issue five address cycles. The first two address cycles are column address. For the third cycle, select a page in the range of 00h through 1Dh. The fourth and fifth cycle are fixed at 00h.

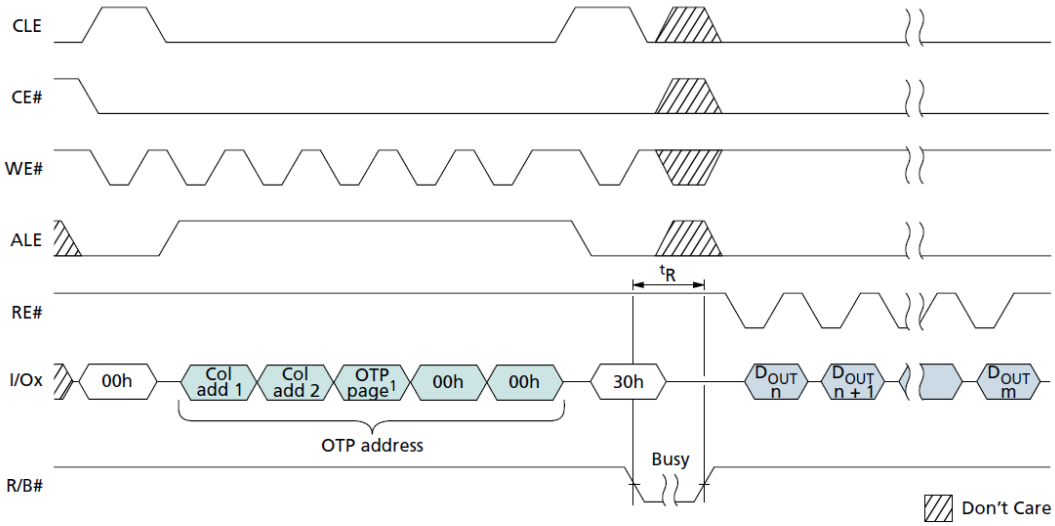


Figure 8.25 OTP Read

8.17.4 OTP Read with Random Data Output (05h-E0h)

The device may output random data (not in sequential order) in a page by writing Random Data Output (05h-E0h) command, which can be operated multiple times in a page. The column address for the next data to be output may be changed to a new column address with the Random Data Output command.

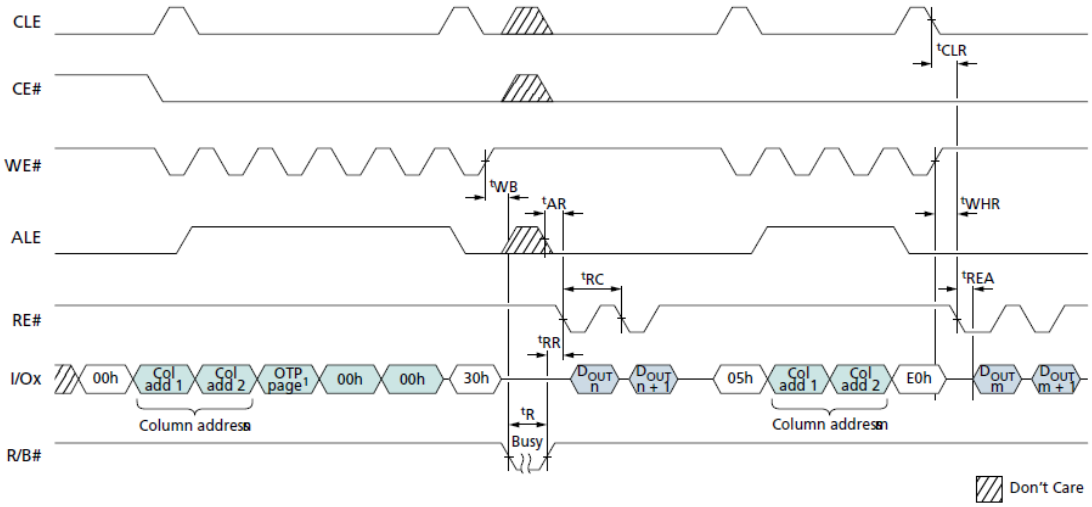


Figure 8.26 OTP Read with Random Data Output

8.17.5 OTP Program Protect (80h-10h)

All pages in the OTP area will be protected simultaneously by issuing the Set Feature (EFh-90h-00h-00h-00h) command to set the device to OTP protection mode. To protect all data in the OTP area, issue the 80h command, then issue 5 addresses 00h before issuing 10h command. After the OTP Program Protect is set, the whole OTP area is protected, no page in OTP area is programmable. The OTP area cannot be unprotected again.

9. INVALID BLOCK AND ERROR MANAGEMENT

9.1 MASK OUT INITIAL INVALID BLOCK(S)

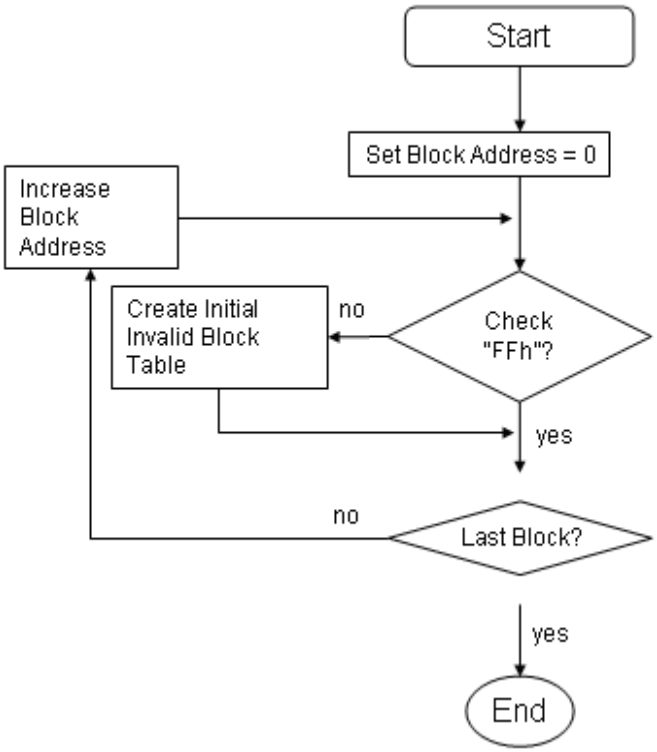
Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by ISSI. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping.

9.2 IDENTIFYING INITIAL INVALID BLOCK(S) AND BLOCK REPLACEMENT MANAGEMENT

If a block is defective, the manufacturer shall mark as defective by setting the Defective Block Marking, as shown in figure, of the first or second page of the defective block to a value of non-FFh. The Defective Block Marking is located on the first byte of user data area or the first byte of spare data area in the pages within a block.

The host shall not erase or program blocks marked as defective by the manufacturer, and any attempt to do so yields indeterminate results. Figure below outlines the flow chart how to create an initial invalid block table. It should be performed by the host to create the initial invalid block table prior to performing any erase or programming operations on the target. All pages in non-defective blocks are read FFh with ECC enabled on the controller. A defective block is indicated by the majority of bits being read non-FFh in the Defective Block Marking location of either the first page or second page of the block. The host shall check the Defective Block Marking location of both the first and second page of each block to verify the block is valid prior to any erase or program operations on that block.

Over the lifetime use of a NAND device, the Defective Block Marking of defective blocks may encounter read disturbs that cause bit changes. The initial defect marks by the manufacturer may change value over the lifetime of the device, and are expected to be read by the host and used to create a bad block table during initial use of the part.



Check “FFh” at “First Byte of Spare Area” at the first page and 2nd page in each block.

Figure 9.1 Algorithm for Bad Block Scanning

9.3 ERROR IN READ OR WRITE OPERATION

Within its lifetime, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The additional block failure rate does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure Sequence
Write	Erase failure	Read Status after Erase → Block Replacement
	Program failure	Read Status after Program → Block Replacement
Read	Up to 8 bit failure	Verify ECC → ECC Correction

Note: Error Correcting Code → RS Code or BCH Code etc.
Example: 8bit correction per 512 bytes of data.

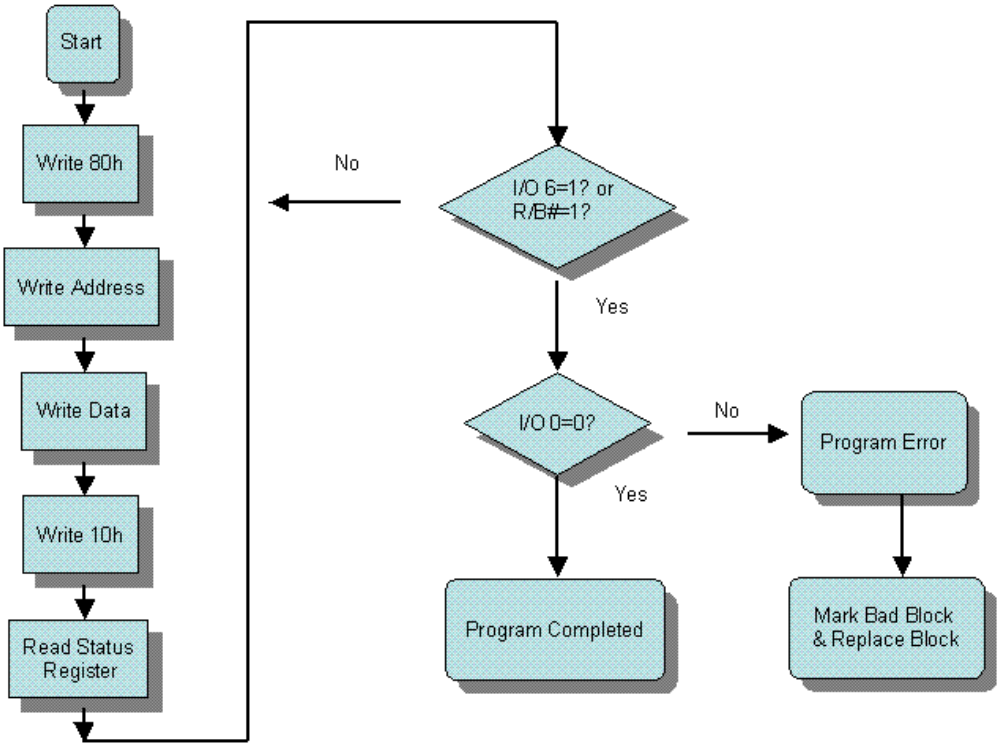


Figure 9.2 Program Flow Chart

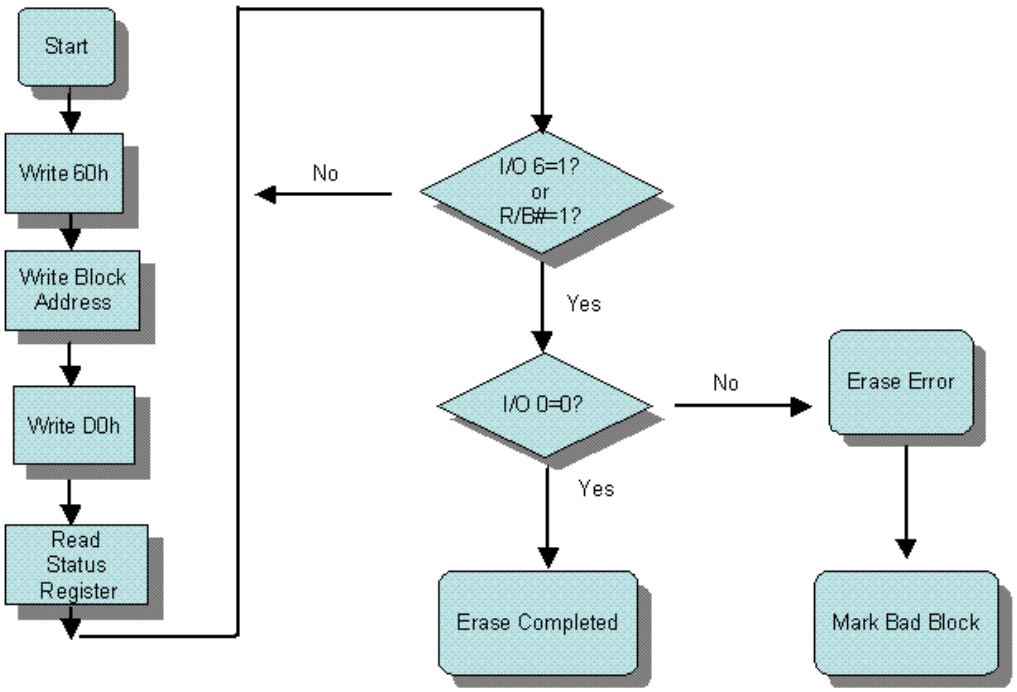


Figure 9.3 Erase Flow Chart

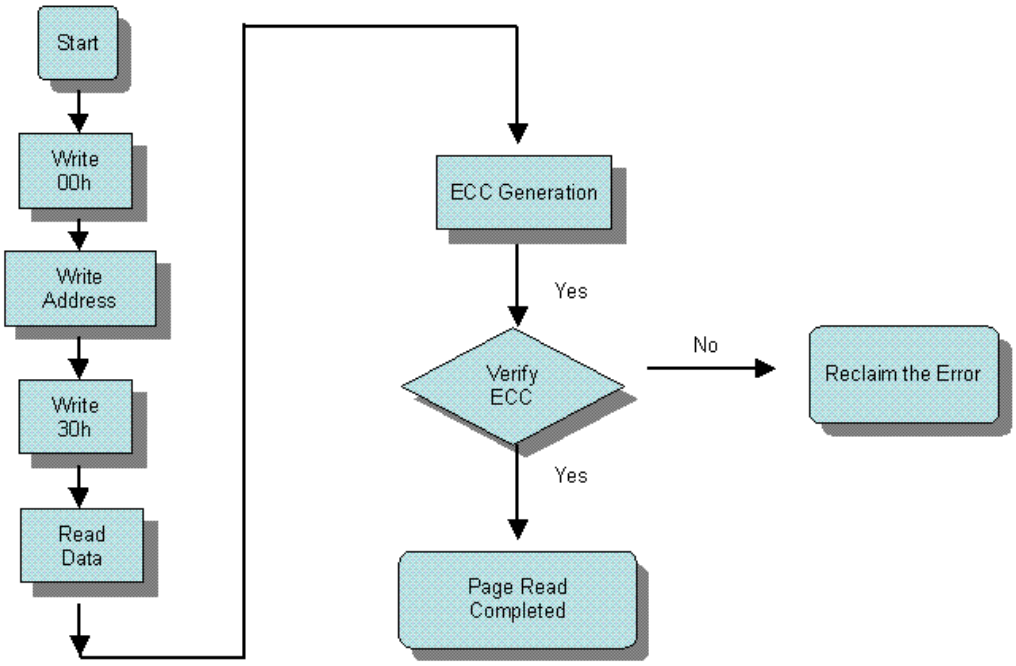


Figure 9.4 Read Flow Chart

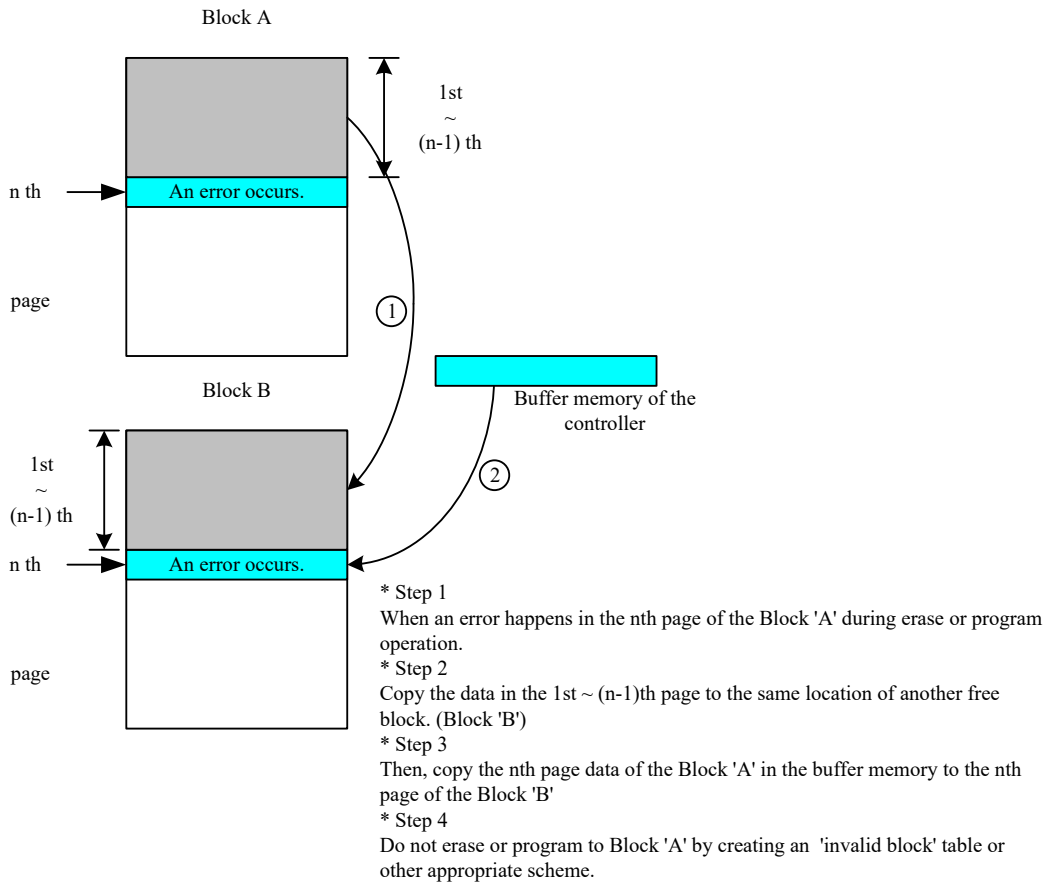
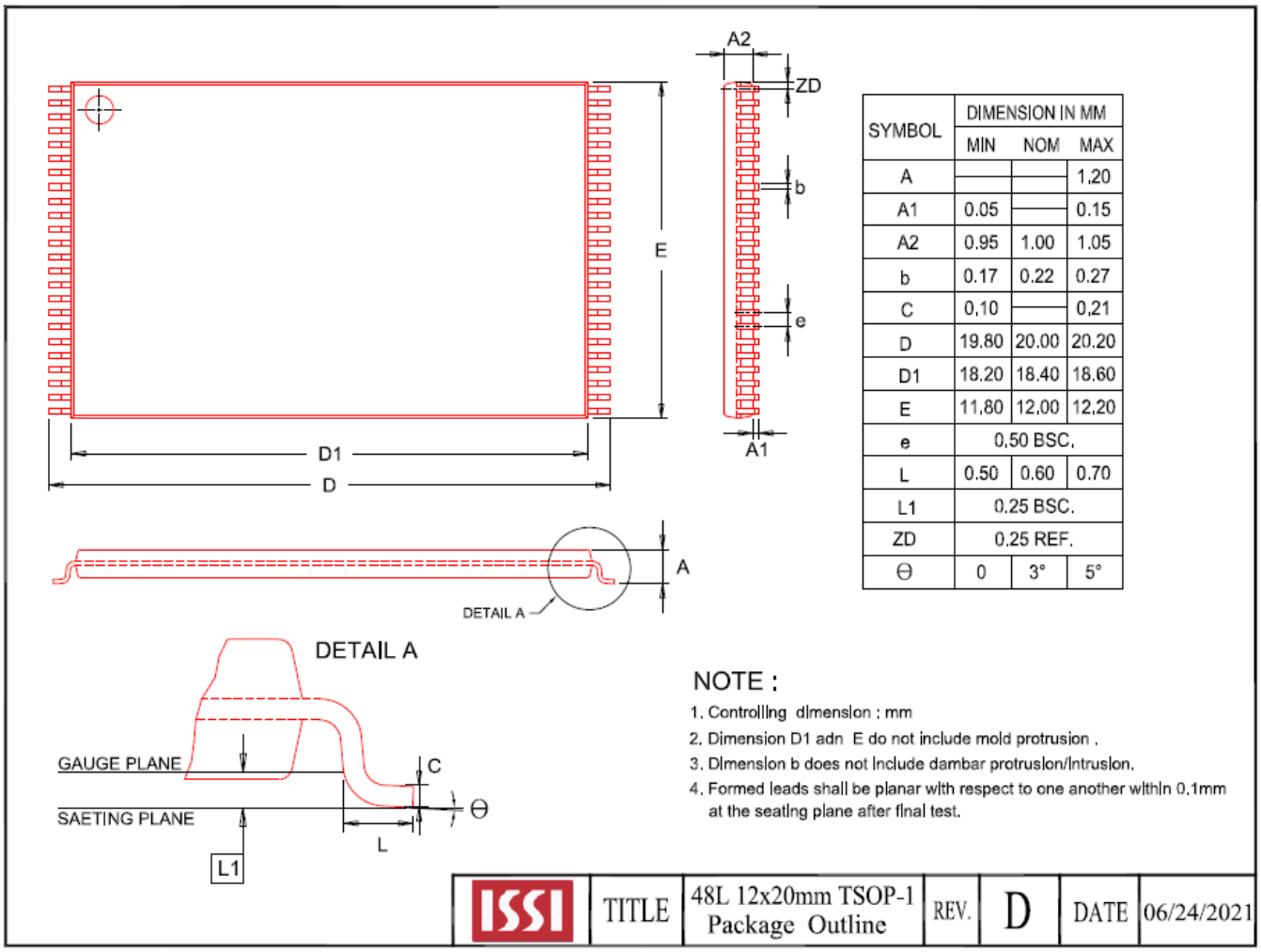


Figure 9.5 Block Replacement

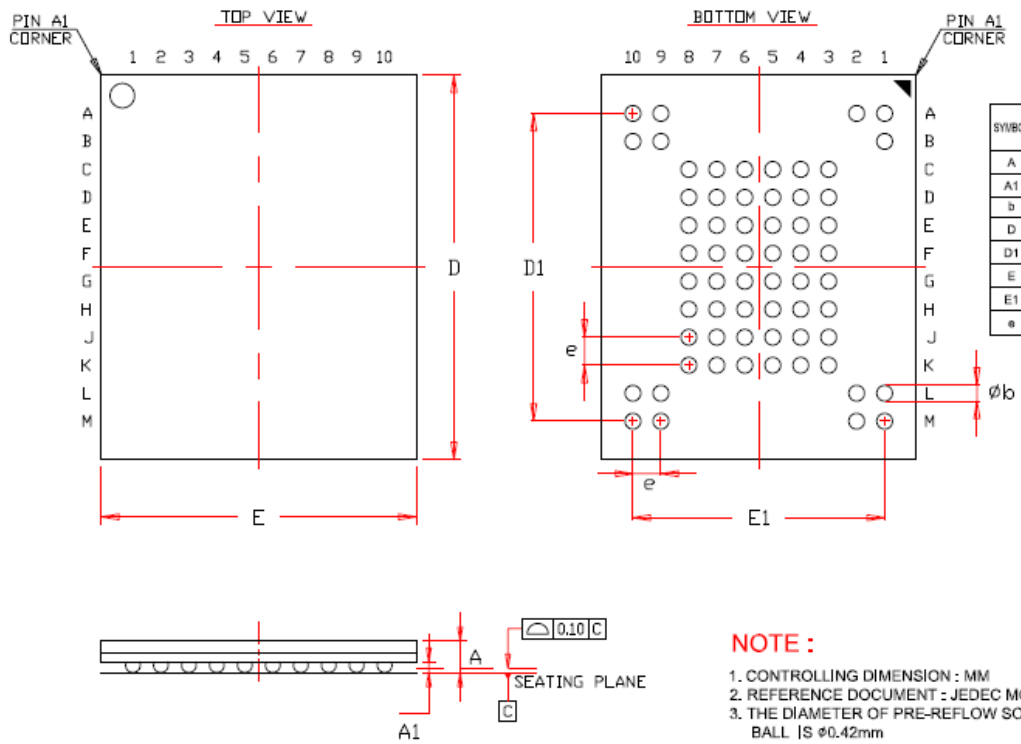
10. PACKAGE TYPE INFORMATION

10.1 48-PIN TSOP (TYPE I) PACKAGE (T)



SYMBOL	DIMENSION IN MM		
	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
C	0.10		0.21
D	19.80	20.00	20.20
D1	18.20	18.40	18.60
E	11.80	12.00	12.20
e	0.50 BSC.		
L	0.50	0.60	0.70
L1	0.25 BSC.		
ZD	0.25 REF.		
Θ	0	3°	5°

10.2 63-BALL VFBGA PACKAGE (B)



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.00	—	—	0.039
A1	0.25	0.30	0.35	0.010	0.012	0.014
b	0.40	0.45	0.50	0.016	0.018	0.020
D	10.90	11.00	11.10	0.429	0.433	0.437
D1	8.80 BSC			0.346 BSC		
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	7.20 BSC			0.283 BSC		
e	0.80 BSC.			0.031 BSC.		

NOTE :

1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT : JEDEC MO-207
3. THE DIAMETER OF PRE-REFLOW SOLDER BALL IS ø0.42mm

	TITLE	63L 9x11x1.0mm VF-BGA Package Outline	REV.	A	DATE	01/18/2016

11. ORDERING INFORMATION – Valid Part Numbers

IS 34 M L 04G 08 8 _ - T L I

TEMPERATURE RANGE
I = Industrial (-40°C to +85°C)
A2 = Automotive Grade (-40°C to +105°C)

PACKAGING CONTENT
L = **RoHS compliant**

PACKAGE Type
T = 48-pin TSOP (Type I)
B = 63-ball VFBGA

Die Revision
Blank = First Gen.

ECC Requirement
8 = 8-bit ECC

Bus Width
08 = x8 NAND
16 = x16 NAND

Density
04G = 4 Gigabit

VDD
L = 3.3V

Technology
M = Standard NAND (SLC)

Product Family
34 = NAND
35 = Automotive NAND

BASE PART NUMBER
IS = Integrated Silicon Solution Inc.

VDD	Density	Bus	Temp. Grade	Order Part Number	Package
3.3V	4Gb	X8	Industrial	IS34ML04G088-TLI	48-pin TSOP (Type I)
				IS34ML04G088-BLI	63-ball VFBGA
			Automotive (A2)	IS35ML04G088-TLA2	48-pin TSOP (Type I)
				IS35ML04G088-BLA2	63-ball VFBGA
		X16	Industrial	IS34ML04G168-BLI	63-ball VFBGA
			Automotive (A2)	IS35ML04G168-BLA2	63-ball VFBGA