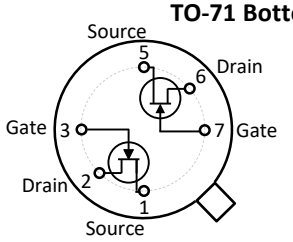
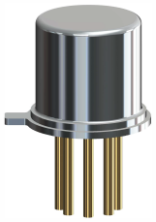
VCR11N Dual N-Channel Voltage Controlled Resistor JFET

Features

- InterFET N0026S Geometry
- Low Leakage: 10 pA Typical
- Low Input Capacitance: 6.0 pF Typical
- High Input Impedance
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

TO-71 Bottom View

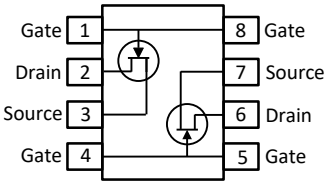




Applications

- Small Signal Attenuators
- Filters
- Amplifier Gain Control
- Oscillator Amplitude Control

SOIC8 Top View



Description

The -25V InterFET VCR11N Voltage Controlled Resistor JFET are targeted for high input impedance applications. Gate leakages are less than 10pA at room temperatures. The resistance range of the VCR11N is 70 Ohms to 200 Ohms. The TO-71 package is hermetically sealed and suitable for military applications.

Product Summary

Parameters		VCR11N Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	-25	V
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-8	V
$r_{ds(on)}$	Drain to Source ON Resistance	70	Ω

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
VCR11N	Through-Hole	TO-71	Bulk
SMPVCR11N	Surface Mount	SOIC8	Bulk
SMPVCR11NTR	7" Tape and Reel: Max 500 Pieces 13" Tape and Reel: Max 2500 Pieces	SOIC8	Minimum 500 Pieces Tape and Reel
VCR11NCOT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
VCR11NCFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-15	V
I_{FG}	Continuous Forward Gate Current	10	mA
P_D	Continuous Device Power Dissipation	300	mW
P	Power Derating	2.4	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 150	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

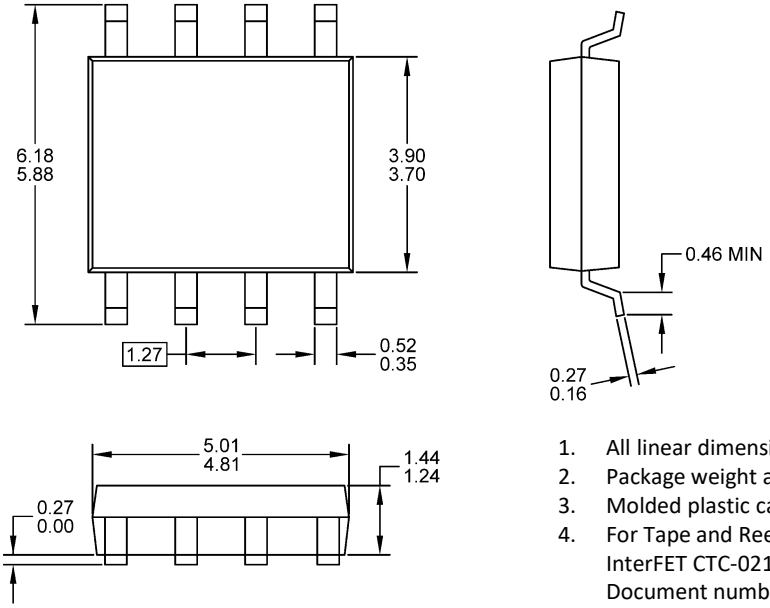
Parameters		Conditions	VCR11N		Unit
			Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	I_G = -1µA, V_{DS} = 0V	-25		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -15V, V_{DS} = 0V		-0.2	nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = -10V, I_D = 1µA	-8	-12	V
$\frac{r_{DS(MIN)}}{r_{DS(MAX)}}$	Static Drain to Source ON Resistance Ratio	Min: V_{DS} = 100mV, r_{DS1} = 200Ω Max: V_{GS1} = V_{GS2}, r_{DS2} = 2kΩ	0.95 0.95	1 1	-

Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

Parameters		Conditions	VCR11N		Unit
			Min	Max	
$r_{ds(on)}$	Drain to Source ON Resistance	I_D = 0A, V_{GS} = 0V, f = 1kHz	70	200	Ω
C_{dg}	Drain Gate Capacitance	V_{DG} = 10V, I_S = 0A, f = 1MHz		7.5	pF
C_{sg}	Source Gate Capacitance	V_{GS} = 10V, I_D = 0A, f = 1MHz		7.5	pF

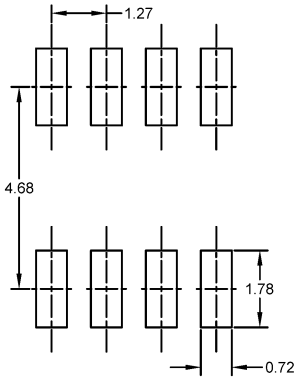
SOIC8 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.21 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

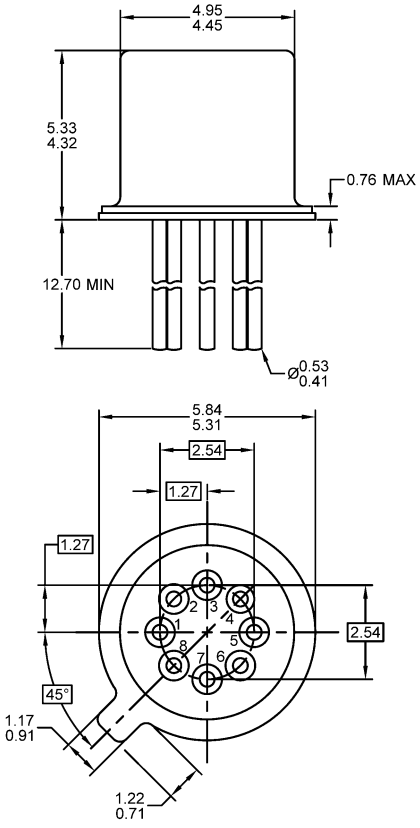
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

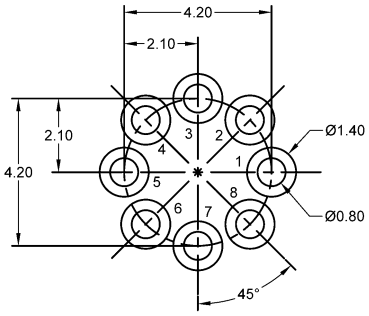
TO-71 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 4.
4. Package weight approximately 0.35 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Bent Lead Through-Hole Layout



1. All linear dimensions are in millimeters.
2. Pads 8 and/or pad 4 can be eliminated for devices with less pins.
3. The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.