Tempo Semiconductor, Inc.

Data Sheet

OCTAL PDM TO 24-BIT TDM CONVERTER

TSDP18xx

GENERAL DESCRIPTION

The TSDP18xx is an ultra low-power, high-performance, 8 channel PDM to Linear PCM converter. It supports Digital MEMS Microphone (DMIC) over sample rates up to 6.144MHz; and output sampling rates of 8KHz up to 384KHz enabling support for Ultrasonic capable DMICs.

TSDP18xx supports 2 channel I2S or Left-Justified (LJ) format output as well as up to 8 channels using the Time-Division Multiplexed (TDM) format. The device enables a wide variety of configurations 32-bit, 24-bit or 16-bit word lengths, clock polarity inversion, and more to maximize compatibility with almost any DSP, Audio Processor, Codec or SOC.

The supplied DMIC sources are driven by a configurable PDM clock ranging from 256kHz up to 6.144MHz, while the digital audio interface operates in slave mode with the supplied SCLK signal ranging from 256kHz up to 49.152MHz, and a LRCLK input providing a frame signal matched to the format, I2S or TDM.

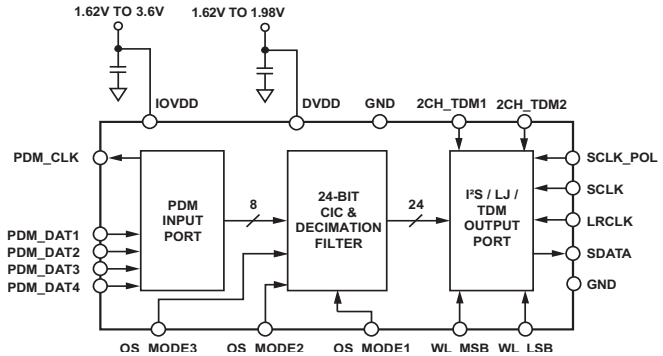
There is a wide range of support for SCLK to LRCLK / FRMCLK ratios ranging from 32Fs to 512Fs.

Configuration of the FIR and decimation filter coefficients are based on combination of SCLK to LRCLK / FRMCLK ratio and the three OS_MODE pins which impact the Oversampling Mode, supporting 8x to 256x.

APPLICATIONS

- **1~8 Channel Digital Microphone Arrays including:**
  - Smart Speakers / Smart Screens
  - Voice Assistance Enabled Devices
  - Audio / Video Conferencing Systems
  - Augmented / Virtual Reality Systems
  - Multi-Mic Beam Forming Applications
  - Far Field Voice Pickup Applications
  - Multichannel Audio Recording Applications
- **DSD to PCM Conversion**

BLOCK DIAGRAM



FEATURES

- **High-Fidelity Octal PDM to Linear PCM Converter**
  - Internal processing takes place at the DMIC clock rate
  - > 142dB SNR / DNR / THD+N Level (20Hz ~ 20kHz)
  - Output Fs supports 8kHz up to 384kHz
  - Configurable DMIC fixed output clock, based on Fs of supplied LRCLK and specified oversampling mode
  - Support for wide range of SLCK to LRCLK / FRMCLK ratios: 32x, 48x, 64x, 96x, 128x, 192x, 256x, 384x, and 512x with automatic detection of SCLK
  - Configurable downsampling rates ranging from 8 to 256 depending on configuration of OS_MODE3, OS_MODE_2, & OS_MODE1 pins as well as SCLK to LRCLK / FRMCLK ratio
- **Configurable I2S / LJ / TDM Output Format Engine**
  - Supports single-edge clocked, double-edge clocked PDM DMICs
  - Supports either 2 Channel I2S or LJ output format or TDM format capable of supporting from 2 up to 8 channels.
  - Supports configurable word lengths of 32-bits, 24-bits, or 16-bits
  - Supports SLCK polarity inversion
  - Supports FRMCLK widths from clock width to word-width Supports single-edge or double edge clocked PDM DMICs
- **Ultra low-power standby and operation**
  - Ultra-low standby (< 1uA) power consumption (when SCLK signal is stopped)
  - Single 1.8V (+/-5%) supply for both IOVDD and DVDD
  - IOVDD can also operate at 3.3V (+/-5%)
  - 2.68mA operating current for 8 Channel TDM mode, Fs = 48kHz, SLCK = 256Fs, IOVdd = 1.8V
- **3x3mm, 20-lead, 0.4mm pitch QFN**
- **Available in both Commercial (0C to 70C) and Industrial Temperature (-40C to 85C) Grades**

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1.0 Features & Description

The TSDP18xx is the solution of choice for applications that are employing 1 to 8 DMICs that must undergo 1-bit PDM to Linear PCM conversion. The TSDP18xx supports a wide number of data formats including I2S, LJ and TDM for 1 to 2 channel operation or up to 8 channels (in TDM mode).

The TSDP18xx ensures a long product life cycle by supporting the widest range of DMIC decimated sampling frequencies in the market, ranging from 8kHz up to 384kHz. The device also maximizes the dynamic range of 4th or 5th order DMIC used, while decreasing BOM cost, simplifying board layout, reducing pin count and reducing power consumption.

Fs is determined by the supplied LRCLK and SCLK signals as the digital audio output port only operates in slave mode.

Based on one of the following valid SCLK to LRCLK ratios (32x, 48x, 64x, 96x, 128x, 192x, 256x, 384x or 512x), as well as the settings of OS_MODE3, OS_MODE2, OS_MODE1 pins, the TSDP18xx automatically determines the oversampling rate, as well as the correct FIR decimation filter coefficients to be applied.

Valid input SCLK frequencies for the supported sampling frequencies range from 256kHz up to a maximum of 49.152MHz.

The device automatically powers down to use less than 1uA in standby mode and resets when the SCLK signal is removed.

The TSDP18xx comes in a 3x3mm, 20-lead, 0.4mm pitch QFN and requires a single 1.8V rail for both the IOVDD and DVDD supplies. IOVDD can also support 3.3V (+/-5%).

For the configuration options below, a logical “0” means that the pin should be grounded (connected to the same GND reference provided to pin 5), and a logical “1” means that the pin should be pulled-up with a 10kohm resistor to DVDD (connected to the same voltage reference provided to pin 19)

1.1 Configuring I2S, LJ & TDM Operation

The 2CH_TDM1 and 2CH_TDM2 pins enables the designer to be able to select between either 2 channel I2S, using a double-edge clocked stereo PDM source, or two mono single-edged clocked PDM sources. Support for Left-Justified 2 channel output using a double-edged clocked stereo PDM source or up to 8 channel TDM output (again using 4 stereo double-edge clocked PDM sources) is also possible. Please refer to Table 1 below for configuration of these two pins. Note: When in 2 channel mode, the *maximum* SCLK to LRCLK ratio is 256. When in TDM mode, the SCLK to LRCLK ratio must be at least enough to support the number of desired channels at the specified word width. Support for an odd number of words is possible, however, please note that unused channel / data frames may contain invalid data.

	2CH_TDM1 (Pin 4)	2CH_TDM2 (Pin 2)
I2S Mode 0, 1 Channel Output Mode, Double-Edged Clocking on PDM Sources	0	0
I2S Mode 1, 2 Channel Output Mode, Single-Edged Clocking on PDM Sources	0	1
Left-Justified, 2 Channel Output Mode, Double-Edged Clocking on PDM Source	1	0
TDM, up to 8 Channel Output Mode, Double-Edged Clocking on PDM Source	1	1

Table 1. Configuring the PCM Output Format using the 2CH_TDM1 and 2CH_TDM2 Pins

1.2 Configuring SCLK Polarity

If the SCLK_POL pin(Pin1) is held HIGH, the SCLK polarity is inverted from standard I2S or LJ modes, whereby the data is transmitted on the rising edge of SCLK. If the SCLK_POL pin is held LOW, data is transmitted on the falling edge of SCLK.

1.3 Configuring the PCM Word Width

The WL_MSB and WL_LSB pins configure the TSDP18xx PCM word length. For configurations where the PCM Word Length is < 32-bits, the rest of the data out to the 32-bit max word length is zero padded.The exact configuration for each PCM Word Width is shown in Table 2.

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	WL_MSB (Pin 16)	WL_LSB (Pin 15)
PCM Word Length = 32-bits	0	0
PCM Word Length = 24-bits	0	1
Reserved	1	0
PCM Word Length = 16-bits	1	1

Table 2. PCM Word Length Configuration using WL_MSB and WL_LSB Pins

1.4 Configuring the OS_MODE [3:1] pins

The OS_MODE3, OS_MODE2, OS_MODE1 pins configure the TSDP18xx FIR Decimation value for a Typical Fs range as shown in Table 3. In order to ensure valid output data, the designer must ensure that valid SCLK to LRCLK ratio is supplied to the TSDP18xx with valid WL_MSB and WL_LSB selection.

OS_ MODE3 (Pin7)	OS_ MODE2 (Pin6)	OS_ MODE1 (Pin8)	Oversample Rate	Bandwidth at -1dB (Normalized)	Typical Fs Range (kHz)	Valid SCLK / LRCLK Ratios for Corresponding OS_MODE Pin Selection
0	0	0	N/A	N/A	N/A	Reserved
0	0	1	N/A	N/A	N/A	Reserved
0	1	0	8	0.1189	256 to 384	32, 48, 64, 96, 128
0	1	1	16	0.2268	128 to 192	32, 48, 64, 96, 128, 192, 256
1	0	0	32	0.4536	64 to 96	32, 64, 96, 128, 192, 256, 384, 512
1	0	1	48	0.4536	48 to 64	48, 96
1	0	1	64	0.4536	32 to 48	64, 128, 192, 256, 384, 512
1	1	0	96	0.4536	24 to 32	96, 192
1	1	0	128	0.4536	16 to 24	128, 256, 384, 512
1	1	1	192	0.4536	8 to 16	192, 384
1	1	1	256	0.4536	8 to 12	256, 512

Table 3. Configuring the Oversampling Mode using OS_MODE3, OS_MODE2, OS_MODE1 Pins

1.5 Power Down and Reset

The TSDP18xx automatically powers down to use less than 1uA in standby mode and resets when the SCLK signal is removed/stopped. The TSDP18xx can be reconfigured by stopping the SCLK, changing and holding the configuration pins while it is stopped then restart the SCLK. The SCLK must remain stopped for at least 100uS to guarantee that the internal reset is asserted and device is reinitialized correctly.

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2.0 Device Characteristics

DVDD_IO = 1.8 V, T_A = 25°C, PDM BCLK Output = 3.072 MHz, LRCLK Input = 48 kHz, TDM format, OS Rate = 64x unless otherwise noted. The PDM audio stream used in the Table 4was generated by the APx525 PDM Module, with a 5th order noise shaper. Measurements are without A-Weighting or AES-17 filter unless otherwise noted. The performance results are limited by the measurement equipment and not the design. Please refer to the SNR / DNR / THD+N Level footnote and corresponding performance plots Figure 17, Figure 18 and Figure 19 as to how this measurement was captured.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Digital Input/Output						
Input High Level	V_{IH}		0.7x DVDD_IO			V
Input Low Level	V_{IL}				0.3x DVDD_IO	V
Output High Level	V_{OH}	I_{OH} = -1mA	0.9x DVDD_IO			V
Output Low Level	V_{OL}	I_{OH} = 1mA		0.1x DVDD_IO		V
Input Capacitance				5		pF
Input Leakage, High	I_{IH}	PDM_DAT, SCLK and LRCLK	-0.9		0.9	uA
Input Leakage, Low	I_{IL}	PDM_DAT, SCLK and LRCLK	-0.9		0.9	uA
SDATA Drive Strength				4.5		mA
PDM_CLK Drive Strength				9		mA
Internal Pull-Up Resistor	R_{PU} / R_{PD}	All Digital I/O pins with pull-up or pull-down		50		kΩ
ESD / Latchup						
IEC1000-4-2			1			Level
JESD22-A114-B			2			Class
JESD22-C101			4			Class
Performance						
SNR[2]		20Hz to 20kHz, Ref to 0dB	125.9		126.4	dB
SNR / DNR / THD+N Level[1]		20Hz to 20kHz	141.9		142.4	dB
SNR, A-Weighted[2]		20Hz to 20kHz, Ref to 0dB	130.6		131.5	dB
THD+N Level[2]		20Hz to 20kHz	123		125	dBFS
THD+N Ratio, A-Weighted[2]		20Hz to 20kHz, -60dBFS input	70.3		70.5	dBFS
Oversampling Rate		Depends on OS_MODE Settings	8		256	
Filter Ripple		DC to 0.437 output Fs	-0.15		+0.01	dBFS
Bandwidth		Rolloff at -1dB		0.4536		Fs
Stop-Band				0.566		Fs
Stop-Band Attenuation			79			dB
Gain		PDM to PCM		0		dB
Bit Width		Internal			24	Bits
Bit Width		Output	16		32	Bits
Interchannel Phase				0		Degrees

Table 4. TSDP18xx Device Characteristics

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Timing						
Minimum dV/dt	dV/dt_{MIN}	0.5x DVDD level must be achieved in at least in 5ms or less	0.18	0.36		V/ms
Start Up	T_{SU}	From 0.9x DVDD and valid SCLK is presented to TSDP18xx to valid PDM_CLK signal is output from TSDP18xx		3		LRCK Cycles
Clocking						
PDM_CLK Output Range	F_{PDM_CLK}	Depends on OS_MODE Settings	0.256		6.144	MHz
LRCLK Input Range	F_{LRCLK}	Depends on OS_MODE Settings	8		384	kHz
SCLK Input Range	F_{SCLK}	Depends on OS_MODE Settings	0.256	3.072	49.152	MHz
SCLK / LRCLK Ratio		Depends on OS_MODE Settings	32		512	

Table 4. TSDP18xx Device Characteristics

1. The > 142dB SNR / DNR / THD+N Level performance number was generated using a generated PDM data source. Please refer to Figure 17, Figure 18, and Figure 19 and the associated Figure text descriptions to learn more about how the PDM data source was generated and also how these measurements were taken.
2 Performance limited by measurement equipment

OS_MODE [3:1]	Decimation Factor	Group (Fixed) Delay	Typical Fs
010	8	4.5 Samples	384kHz
011	16	9.75 Samples	192kHz
1xx	32+	18.375 Samples	< = 96kHz

Table 5. TSDP18xx Group (Fixed) Delay

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3.0 Typical Performance Characteristics (from APx525)

DVDD_IO = 1.8 V, T_A = 25°C, PDM BCLK Output = 3.072 MHz, LRCLK Input = 48 kHz, TDM format, OS Rate = 64x unless otherwise noted. PDM Generator is APx525 PDM Module, 5th order noise shaper, without A-Weighting or AES-17 filter unless otherwise noted.

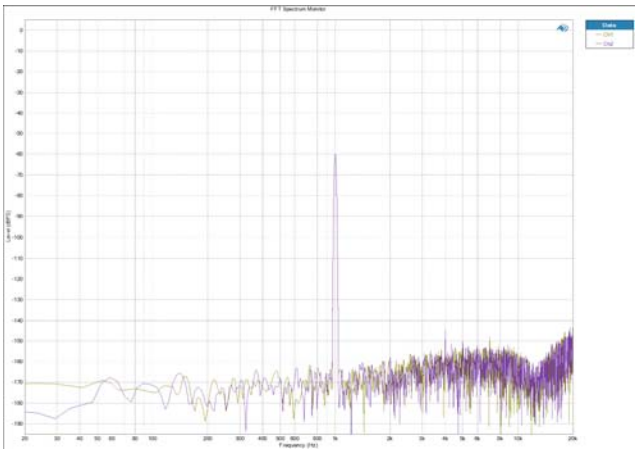

Figure 1. FFT, Fs = 48kHz, -60dBFS Input

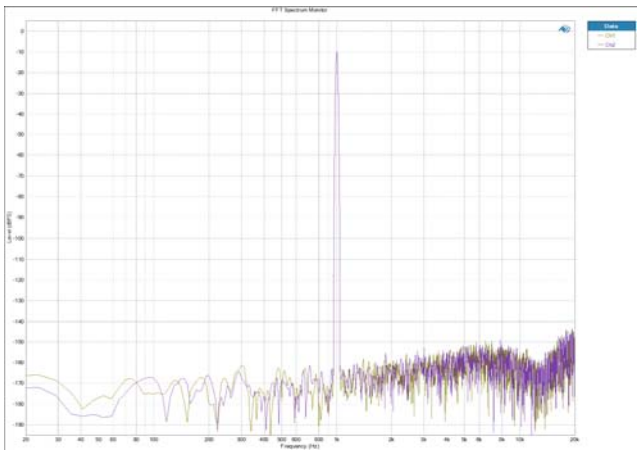

Figure 2. FFT, Fs = 48kHz, -10dBFS Input

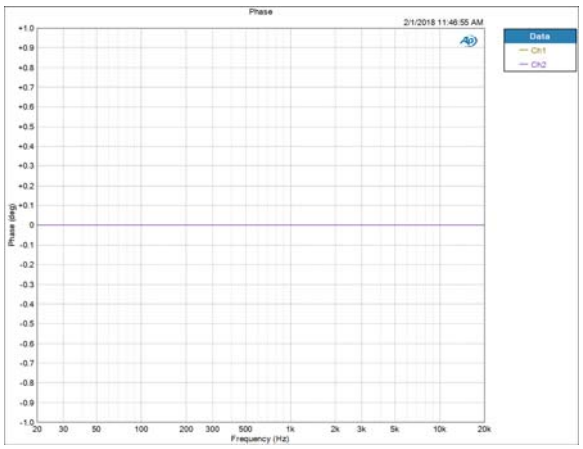

Figure 3. Filter Phase Response, Fs = 48kHz, -10dBFS

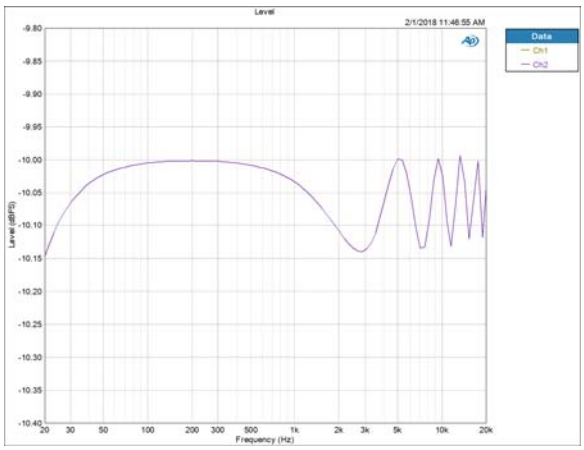

Figure 4. Filter Ripple, Fs = 48kHz, -10dBFS Input

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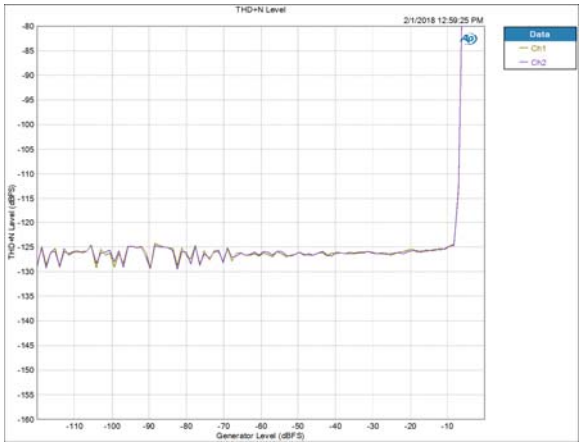

Figure 5. THD+N vs Level, Fs = 48kHz, -120 to 0dBFS

Figure Note: Please note that the reason THD+N vs. Level plot shows a spike in THD+N starting around -7dBFS is due to the fact that the Noise Shaper of the 5th 5th Order PDM Generator module in the APx525 goes unstable above -7dBFS and is not a reflection of the performance of the TSDP18xx.

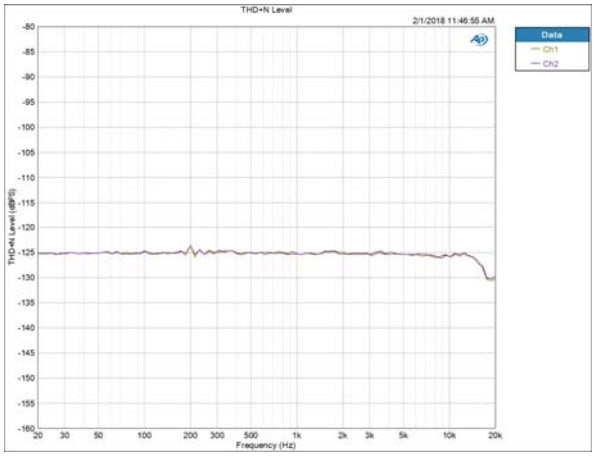

Figure 6. THD+N vs. Frequency, Fs = 48kHz, -10dBFS

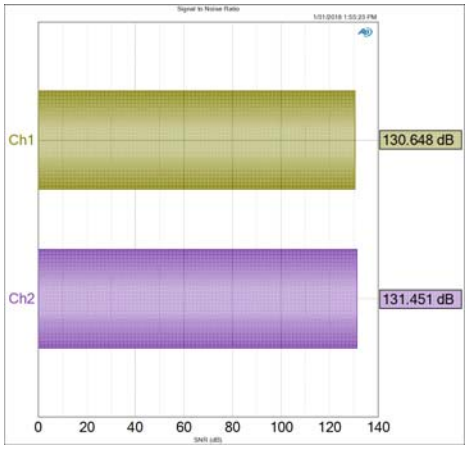

Figure 7. SNR, A-Weighted, Fs = 48kHz, Ref to 0dB

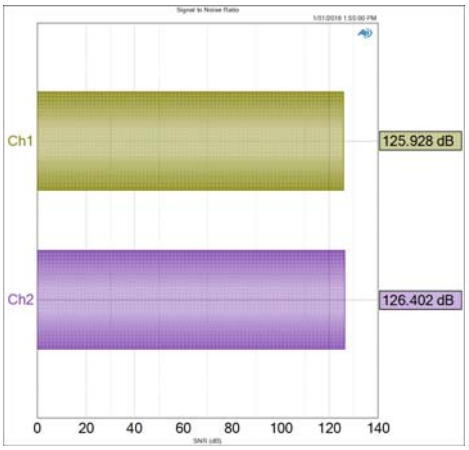

Figure 8. SNR, Unweighted, Fs = 48kHz, Ref to 0dB

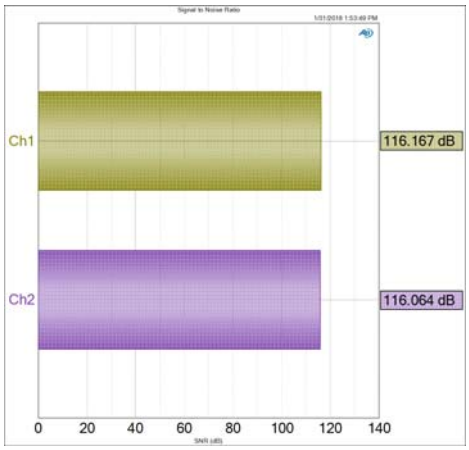

Figure 9. SNR, Unweighted, Fs = 48kHz, -10dBFS Input

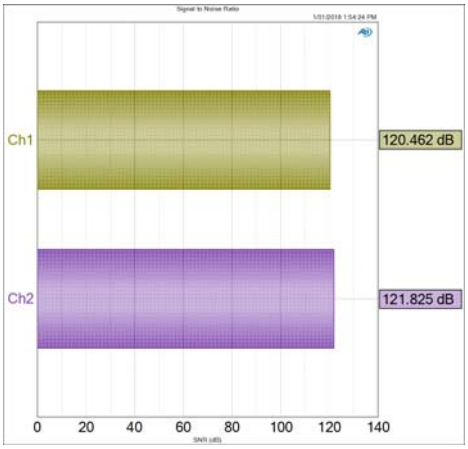

Figure 10. SNR, A-Weighted, Fs = 48kHz, -10dBFS Input

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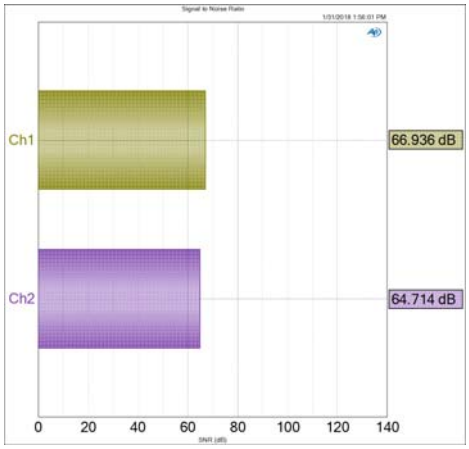

Figure 11. SNR, Unweighted, Fs = 48kHz, -60dBFS Input

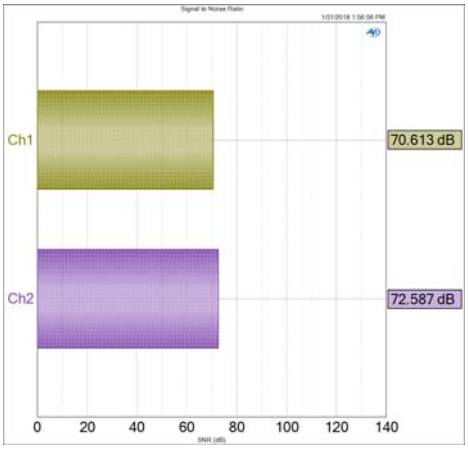

Figure 12. SNR, A-Weighted, Fs = 48kHz, -60dBFS Input

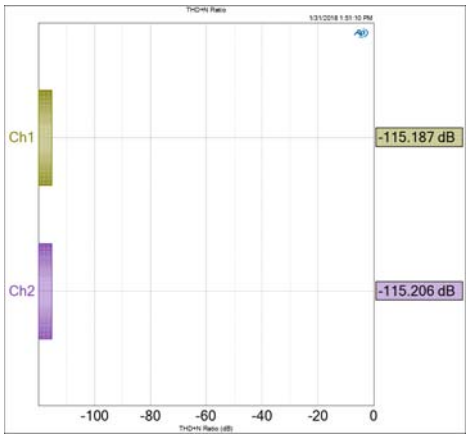

Figure 13. THD+N, Unweighted, Fs = 48kHz, -10dBFS Input

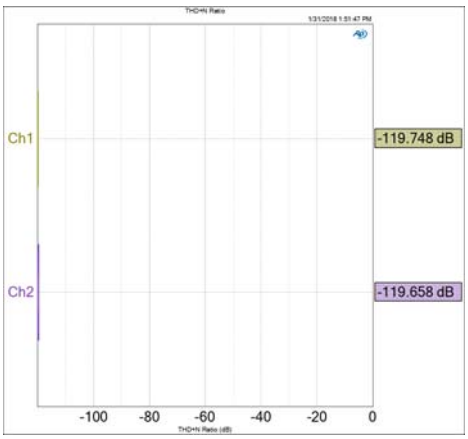

Figure 14. THD+N, A-Weighted, Fs = 48kHz, -10dBFS Input

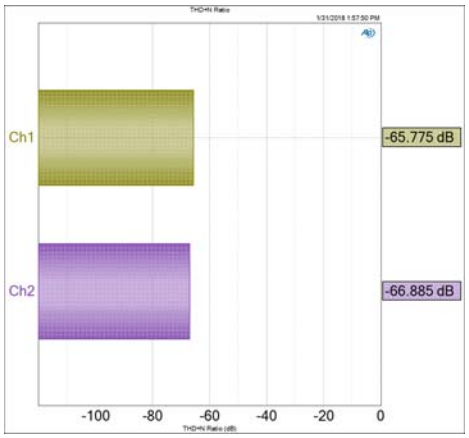

Figure 15. THD+N, Unweighted, Fs = 48kHz, -60dBFS Input

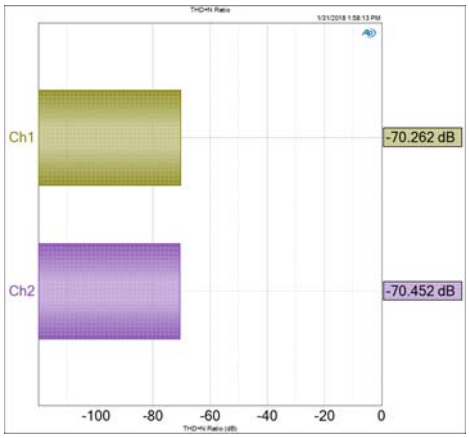

Figure 16. THD+N, A-Weighted, Fs = 48kHz, -60dBFS Input

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3.1 Typical Performance Characteristics (from Generated PDM Source)

DVDD_IO = 1.8 V, T_A = 25°C, PDM BCLK Output = 3.072 MHz, LRCLK Input = 48 kHz, I2S format, OS Rate = 64x.

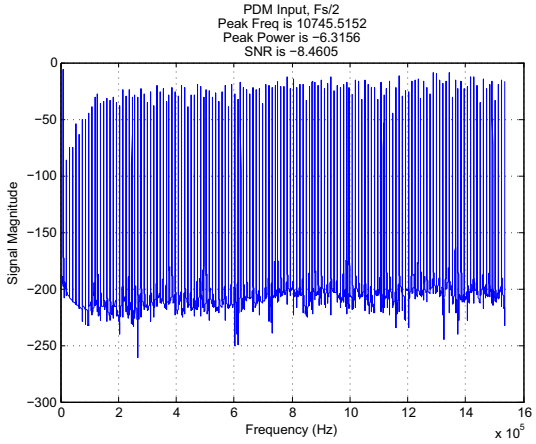

Figure 17. Specialized PDM test signal carrying a 10.745kHz sine wave

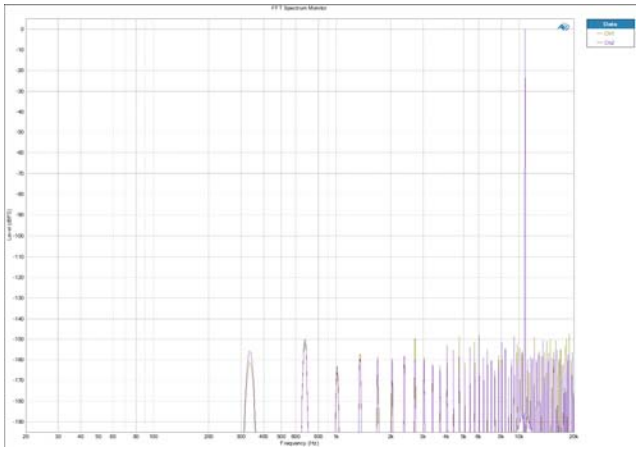

Figure 18. FFT, Fs = 48kHz, 0dBFS, 10.745kHz sine wave, Converted Linear PCM I2S Output from TSDP18xx

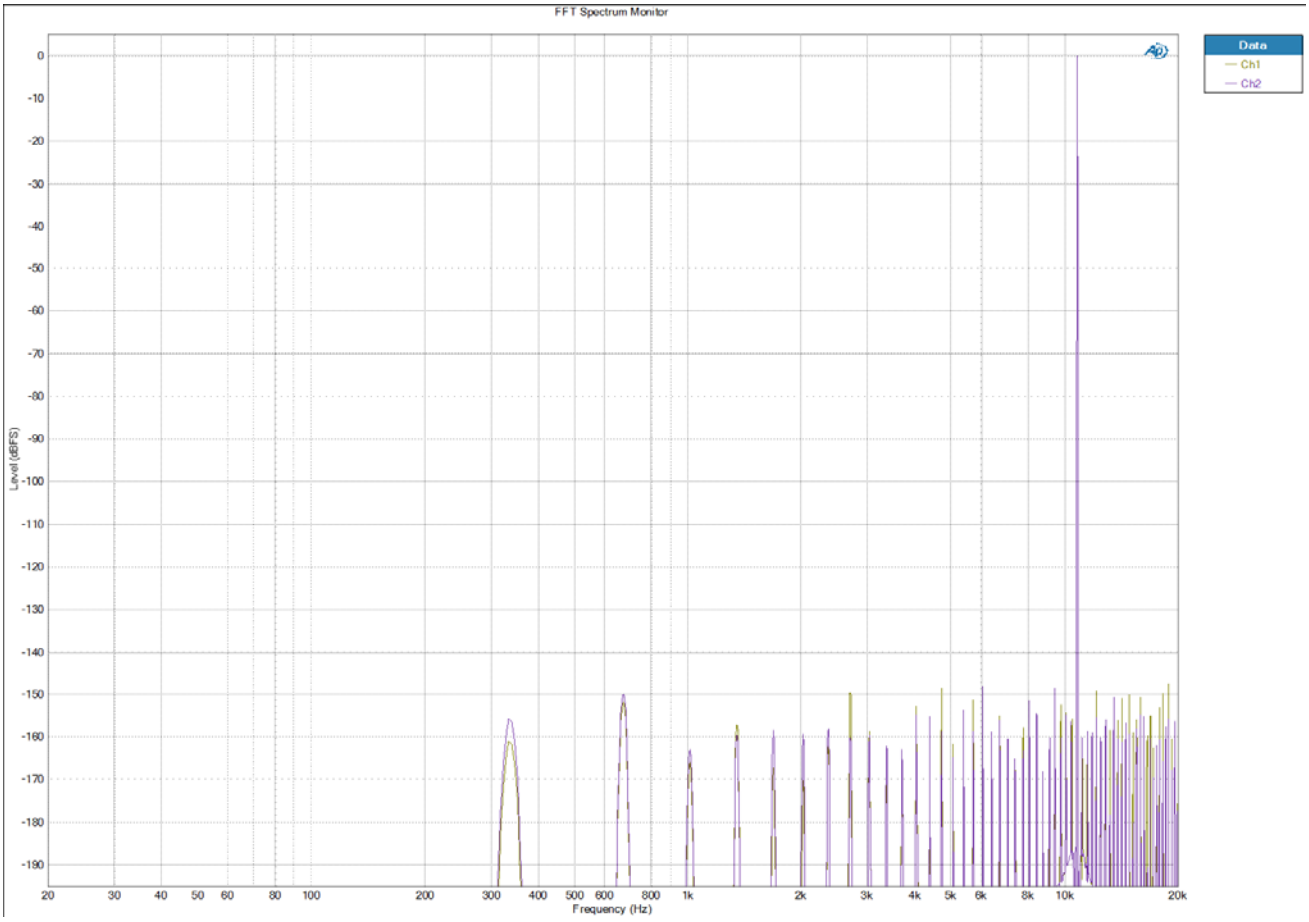

Figure 19. Zoom In of Figure 18

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4.0 QFN Package Lead Configuration and Function Descriptions

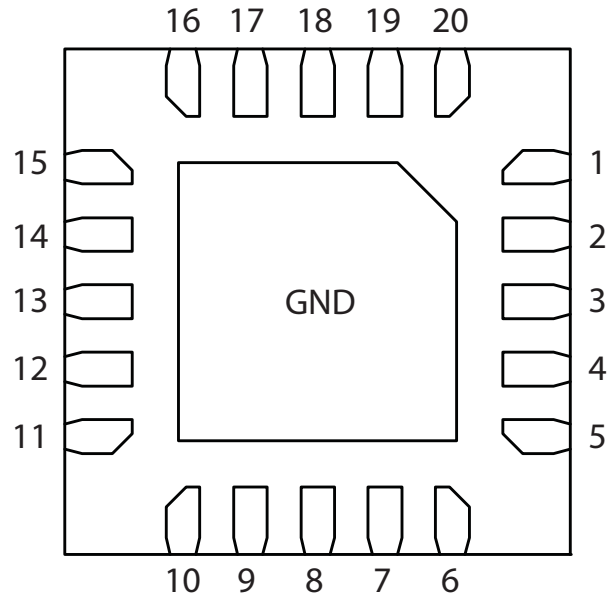

Figure 20. TSDP18xx QFN Package Lead Configuration

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Lead Count	Signal Name	Type	Description
1	SCLK_POL	Input	If HIGH, the data is transmitted on the rising edge of SCLK and sampled on the falling edge of SCLK. If LOW, the data is transmitted on the falling edge of SCLK and sampled on the rising edge of SCLK.
2	2CH_TDM2	Input	2CH_TDM2 input pin used to configure the output PCM mode. Refer to Table 1. Note: If the output format is 2-Channel, then the maximum SCLK to LRCLK ratio supported is 256.
3	GND	Ground	Ground
4	2CH_TDM1	Input	2CH_TDM1 input pin used to configure the output PCM mode. Refer to Table 1. Note: If the output format is 2-Channel, then the maximum SCLK to LRCLK ratio supported is 256.
5	GND	Ground	Ground
6	OS_MODE2	Input	Input pin used to configure the oversampling mode. Refer to Table 3.
7	OS_MODE3	Input	Input pin used to configure the oversampling mode. Refer to the Table 3.
8	OS_MODE1	Input	Input pin used to configure the oversampling mode. Refer to Table 3.
9	PDM_DAT4	Input	PDM Data Input for stereo or mono DMICs
10	PDM_DAT3	Input	PDM Data Input for stereo or mono DMICs
11	PDM_DAT2	Input	PDM Data Input for stereo or mono DMICs
12	IOVDD	Supply	IO Supply
13	PDM_DAT1	Input	PDM Data Input for stereo or mono DMICs
14	PDM_CLK	Output	PDM Clock Output for all DMICs
15	WL_LSB	Input	LSB in the Word Length configuration. Refer to Table 2.
16	WL_MSB	Input	MSB in the Word Length configuration. Refer to Table 2.
17	SCLK	Input	Serial Bit Clock for I2S/TDM
18	SDATA	Output	Serial Data Output for High Fs I2S/TDM
19	DVDD	Supply	Core Supply
20	LRCLK	Input	Left/Right Clock for I2S/Frame Sync for TDM

Table 6. QFN Package Lead Function Descriptions

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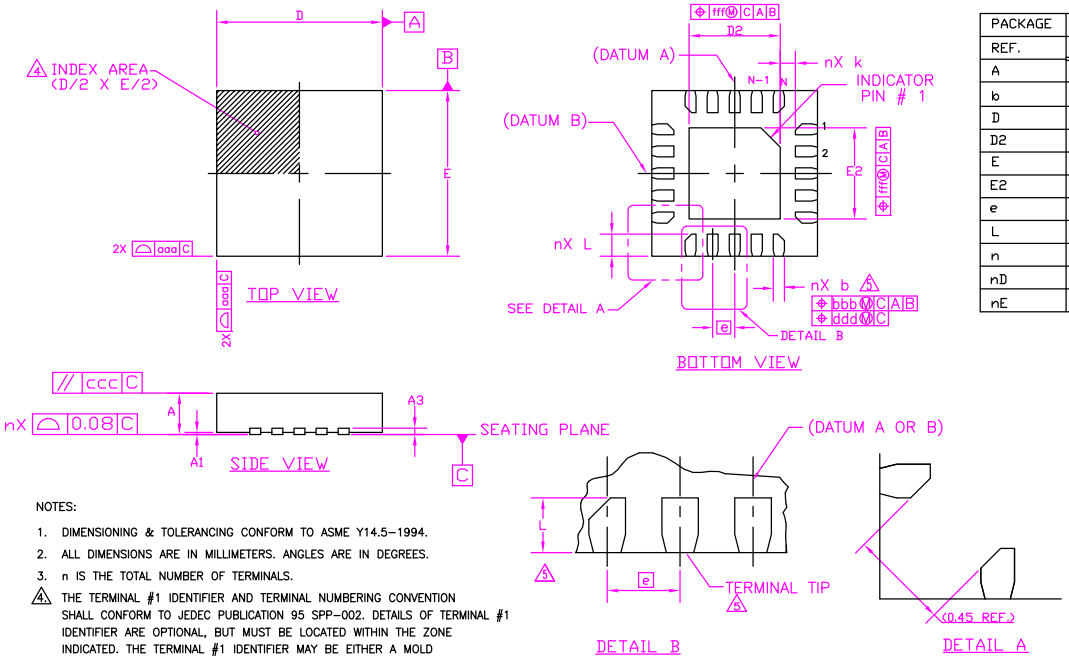
5.0 QFN Package Mechanical Specifications



PACKAGE	20L 3X3 - 0.4		
REF.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
b	0.15	0.20	0.25
D		3.00 BSC.	
D2	1.55	1.65	1.75
E		3.00 BSC.	
E2	1.55	1.65	1.75
e		0.40 BSC.	
L	0.30	0.40	0.50
n		20	
nD		5	
nE		5	

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A1	0	0.02	0.05	
A3		0.203 REF.		
k	0.20	–	–	
TOLERANCES OF FORM AND POSITION				
aaa		0.10		
bbb		0.07		
ccc		0.10		
ddd		0.05		

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. n IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC PUBLICATION 95 SPP-002. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. nD AND nE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. DETAIL A; AS REQUIRED TO MAINTAIN MINIMUM SPACING BETWEEN LEADS.
9. DRAWING DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OR CUTTING BURR

Figure 21. 3mm x 3mm, 20-lead, 0.4mm pitch QFN Package Mechanical Drawing (Note: Drawing Not to Scale)

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6.0 Audio Data Formats

The TSDP18xx supports single bit PDM input sources with wide range of frequencies and a comprehensive output format and bit width

6.1 Audio Input Format

The versatile TSDP18xx supports both double edge clocked PDM input as well as single edge PDM input. The details of the timing are shown in sections 6.1.1 and 6.1.2.

6.1.1 Double-Edge Clocked PDM Input Timing

The PDM_CLK signals to the DMIC are provided at an Fs determined by OS_MODE1, 2, 3 pins, provided valid LRCLK and SCLK signals are made available. For I2S Mode 1, Left-Justified and TDM modes, the TSDP18xx supports the industry standard double clock-edge latching as shown in Figure 22 and corresponding Table 7

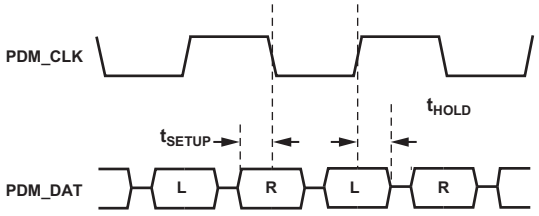

Figure 1. Doubled-edged Clocked PDM Timing Diagram

Parameter	t_{MIN}	t_{MAX}	Unit
Data Setup Time, t_{SETUP}	7		ns
Data Setup Time, t_{HOLD}	4		ns

Table 1. Double-Edge Clocked PDM Input Timing

Please note that the Right Channel PDM data is latched into the TSDP18xx on the falling edge of the PDM_CLK while the Left Channel of the PDM data is latched into the TSDP18xx on the rising edge of the PDM_CLK. Also note that this mode is only applicable to 3 out of the 4 possible PCM output modes (I^2S Mode 1, LJ and TDM). I^2S Mode 2 employs the singled-edge clocked PDM timing as shown in Figure 23.

6.1.2 Single-Edge Clocked PDM Input Timing

When the 2CH_TDM1 and 2CH_TDM2 pins are configured for I2S Mode 2, the PDM_CLK signals to the DMIC are provided at an Fs determined by OS_MODE1, 2, 3 pins, provided valid LRCLK and SCLK signals are available. The TSDP18xx also supports the lesser used industry standard single clock-edge latching as shown in Figure 23 and corresponding Table 8:

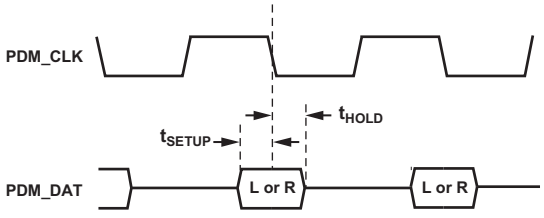

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Figure 2. Single-Edged Clocked PDM Timing Diagram

Parameter	t_{MIN}	t_{MAX}	Unit
Data Setup Time, t_{SETUP}	7		ns
Data Setup Time, t_{HOLD}	4		ns

Table 2. Single-Edge Clocked PDM Input Timing

When the single edge PDM clock mode is selected, the left channel will be taken from PDM_DAT2 and the right channel from PDM_DAT1.

6.2 Audio Output Formats

For the Digital Audio Output, the TSDP18xx supports 3 standard audio interface formats, with a broad level of configuration via pin strappings, which enhances compatibility to meet most audio DSP or SOC based systems.

6.2.1 Left Justified Audio Output

The TSDP18xx Left Justified mode is conformant with the standard specification as shown in Figure 24. In particular, the MSB is available on the first rising edge of SCLK following a LRCLK transition. The other bits are then transmitted in order. The LRCLK signal is high when left channel data is present and low when right channel data is present. In Figure 24, the SCLK_POL pin is LOW, showing standard polarity of the SCLK signal for the LJ format.

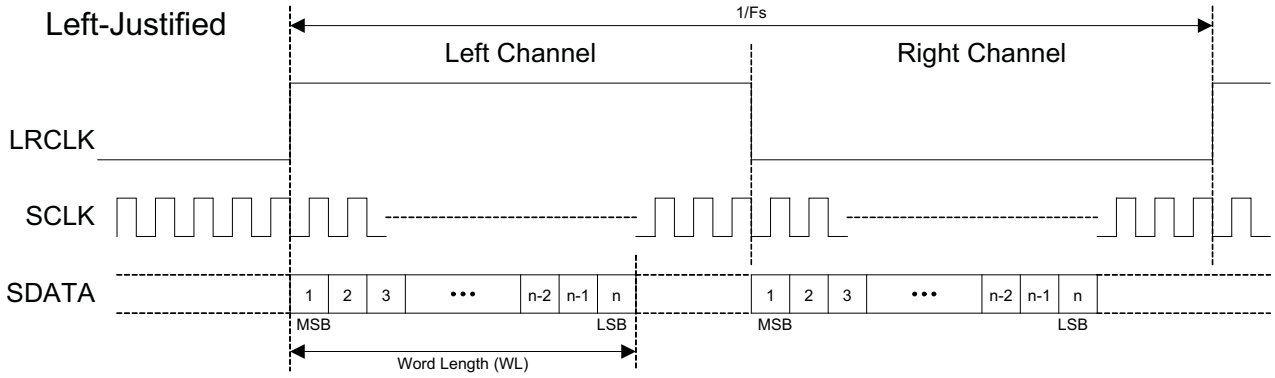

Figure 3. Left-Justified Audio Interface (assuming n-bit word lengths)

6.2.2 I²S Format Audio Output

The TSDP18xx I²S mode is conformant with the standard specification as shown in Figure 25. In particular, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted

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in order. In Figure 25, the SCLK_POL pin is LOW, showing standard polarity of the SCLK signal for the I^2S format.

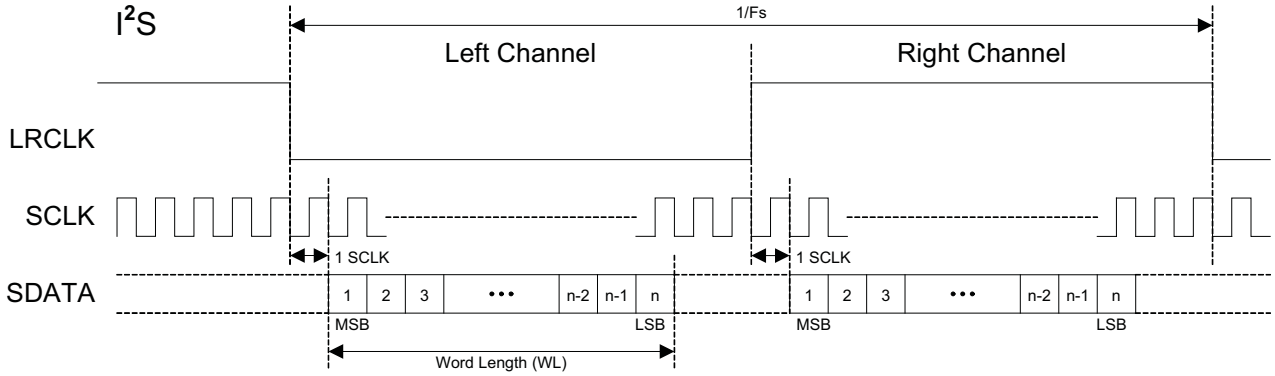

Figure 4. I^2S Justified Audio Interface (assuming n-bit word length)

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6.2.3 TDM Format Audio Output

TDM is a mechanism for transmitting or receiving multiple channels of audio information over a single data connection. When the TSDP18xx is in TDM mode, the SDOUT pin is used to output TDM data.

TDM data is transferred MSB first and the SCLK to FRMCLK (serial bit clock / frame clock) ratio can be any supported rate from 32Fs up to 512Fs, provided that SCLK <= 49.152MHz and the word-length set by WL_MSB and WL_LSB does not exceed the total number of SCLKs available to clock out the total number of data bits desired. The digital audio output port supports up to eight, 32-bit, 24-bit or 16-bit time slots (MSB justified within a slot).

The audio data is left-justified within the time slot by padding the unused bits with zeros, when the word length is < 32-bits. Valid audio data word lengths are 32, 24, or 16 bits.

Either short or word-length frame syncs can be accepted.

If SCLK_POL is LOW, data is transmitted on the rising edge of SCLK, otherwise, data is transmitted on the falling edge of SCLK. Data should be sampled on the opposite clock edge by the receiver.

The LRCLK signal provides the frame sync pulse and will be a single bit clock in length to start the frame when configured for TDM modes, otherwise it defaults to I2S format and frames the left and right channels.

6.2.3.1 SCLK, LRCK, Word Length & PCM Word Slot Availability

For certain applications there may be a need for an uneven number of DMICs (7, 5, 3 or 1) and/or the PCM output word widths is 24-bits. The following shows how the TSDP18xx operates for uneven DMICs and/or 24bit word width:

After a maximum of 8 slots have been output from the TSDP18xx when in TDM mode or 2 slots when in I2S or LJ mode, the device just continues to clock out zeros.

If the slot count is not an integer value, as indicated in Table 9 below by the numbers with an “*” next to them, the device will automatically sync back up once all SCLKs have taken place within that TDM frame.

A valid configuration for 5 DMICs with a 24-bit word length is one that offers a 128 SCLK to LRCLK ratio. In this case, there will be 5 24-bit word slots plus 8 extra cycles, however, please note that the data in the extra 8 cycles may be undefined.

Ignoring the right frame data when in I2S or LJ mode, or all other word slots other than the first in TDM mode can support systems that have less than 2 DMICs.

Using multiple TSDP18xx devices, each with their own TDM bus can support systems that have more then 8 DMICs.

	Valid PCM Word Slots in TDM Mode SCLK to LRCLK Ratio								
Word Length	**512**	**384**	**256**	**192**	**128**	**96**	**64**	**48**	**32**
32	**8**	**8**	**8**	**6**	**4**	**3**	**2**	**N/A**	**N/A**
24	**8**	**8**	**8**	**8**	**5***	**4**	**2***	**2**	**N/A**
16	**8**	**8**	**8**	**8**	**8**	**6**	**4**	**3**	**2**

Table 3. TDM Mode PCM Word Slot Availability based on SCLK to LRCLK Ratio and Word Length

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6.2.4 Standard SCLK Polarity, TDM Audio Output

In TDM mode, the MSB is available on the first rising edge of SCLK following a FRMCLK transition. The other bits up to the LSB are then transmitted in order. The frame sync pulse must be present for at least one SCLK cycle, or may be continue for up to the duration of a word length, as shown by the dashed line in Figure 26.

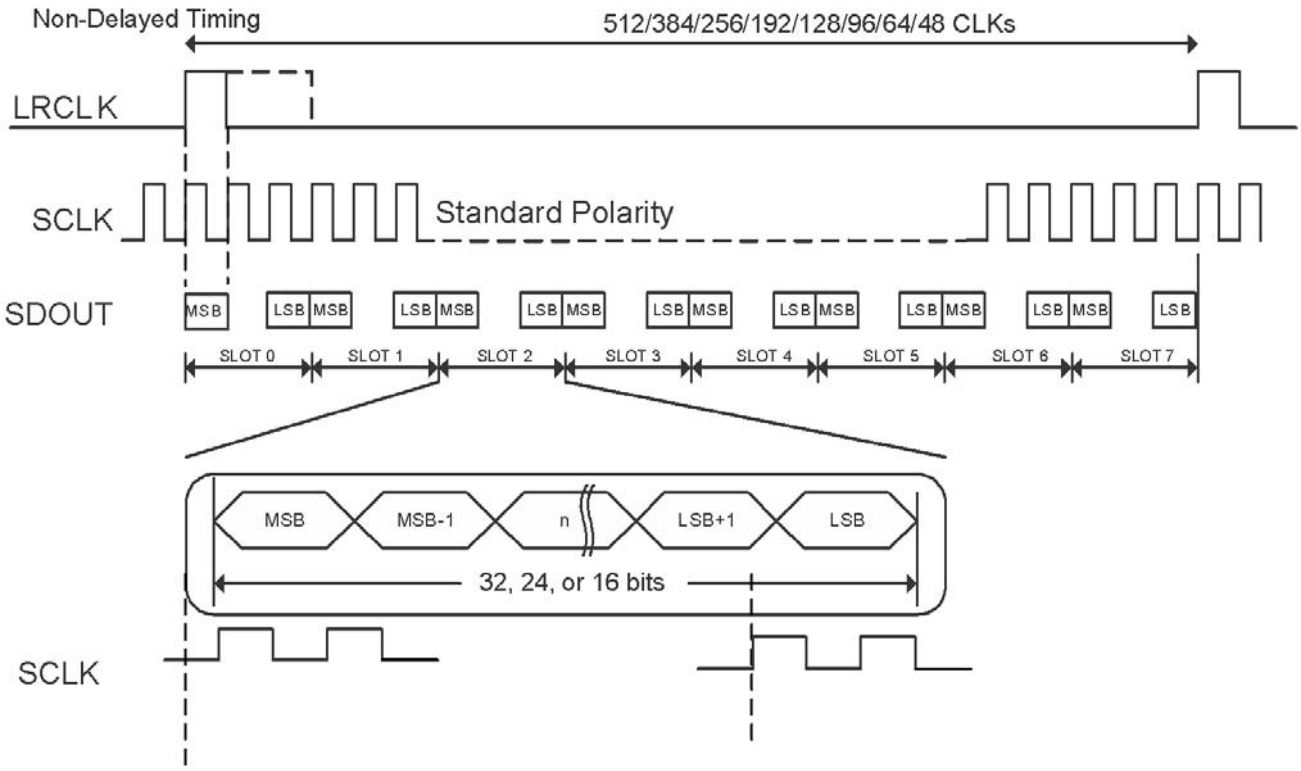

Figure 5. TDM Audio Output (Standard Polarity)

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6.2.5 Inverted SCLK Polarity, TDM Audio Output

In TDM mode, the MSB is available on the first falling edge of BCLK following a FRMCLK transition. The other bits up to the LSB are then transmitted in order.The frame sync pulse must be present for at least one SCLK cycle, or may be continue for up to the duration of a word length, as shown by the dashed line in Figure 27.

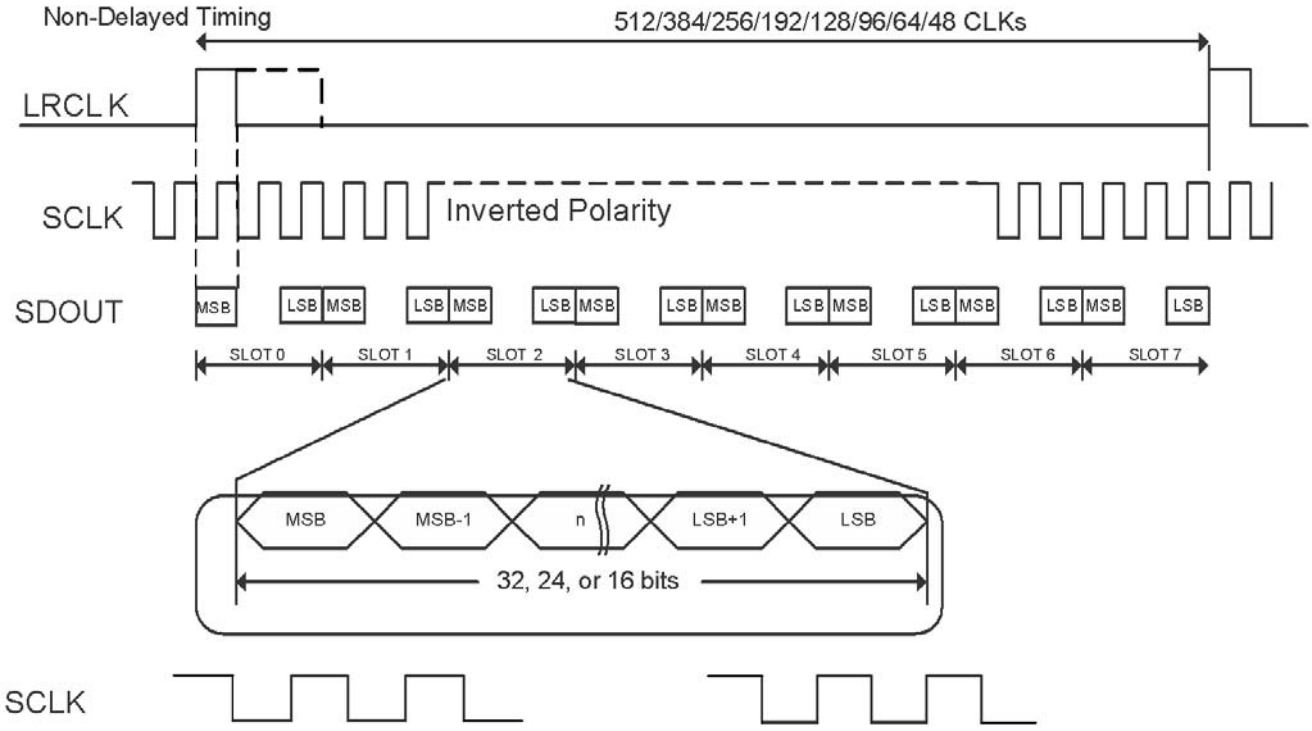

Figure 6. TDM Audio Output (Inverted Polarity)

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7.0 Ordering Information

TSDP1808X1NEGXZAX8	Commercial Temp (0C ~ 70C), 3x3mm, 20-lead, 0.4mm pitch QFN package, Tape & Reel
TSDP1808X1NEGIZAX8	Industrial Temp (-40C ~ 85C), 3x3mm, 20-lead, 0.4mm pitch QFN package, Tape & Reel
TSDP18xx -EVAL	TSDP18xx Evaluation Board using 20-lead QFN, Commercial Temp
TSDP1808X1NEGXZAX	Commercial Temp (0C ~ 70C), 3x3mm, 20-lead, 0.4mm pitch QFN package, Tray
TSDP1808X1NEGIZAX	Industrial Temp (-40C ~ 85C), 3x3mm, 20-lead, 0.4mm pitch QFN package, Tray

Please contact sales@temposemi.com for more information on lead times.

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8.0 Revision History

REV	DATE	PAGES	DESCRIPTION
0.96	8/6/2019	18,19	Edited diagrams
0.95	5/22/2019	pages 1 ,3, 4, 5, 16,17,18	Edited text and diagrams
0.86	4/10/2019	page 19	edited text and description on section 1 and
0.85	10/3/2018	page 19	added parts in ordering and removed confidential.
0.84	9/26/2018	page 19	Updated part number
0.83	7/6/2018	Pages 1, 3.	Updated text on pages 1, 3, 4, and 16. Updated page number on TOC (should have been page 2).
0.82	6/26/2018	Pages 9, 10.	Added Section 3.1 to page 9 along with 3 new figures and text showing supporting measurements for the > 142dB SNR / DNR / THD+N Level performance numbers. Added “GND” text indicator to landing pad in Figure 20, “TSDP18xx QFN Package Lead Configuration,” on page 11.
0.81	6/20/2018	Page 1	Updated first page formatting. Updated max SNR number to > 142dB based on latest performance measurements.
0.8	3/29/2018	Added 1 new page: 17	Added three pages to support new 3mm x 3mm, 20-lead, 0.4mm pitch QFN package pinout diagram, function description table, and mechanical drawing. Added ordering information page. Shortened Revision History table, removing details about revisions 0.1 to 0.4. Removed 2mm x 2mm, 20-ball, 0.4mm pitch BGA package pinout disgram, function description table, and mechanical drawing. Fixed date year typo on 0.5 rev history.
0.7	3/9/2018	Updated 9,10, 12 Added page 11	Updated Package Pin Diargram & Pin Function Description Table to reflect finalized A0 design. Added mechanical package drawing to page 11. Updated maximum SCLK to LRCLK ratio when in I2S or LJ modes to be 128 instead of 256 on page 12. Added additional valid SCLK to FRMCLK ratios for TDM modes of 96, 64 and 48 to Figures 24 and 25.
0.6	2/20/2017	Various	DVDD IO voltage is now limited to operating at either 1.8V (+/- 5%) or 3.3V (+/-5%). Replaced t_{POR} row in table with dV/dt_{MIN} as this data was deemed more important to the board designer. In order for device to reset as well as go into standby mode, the SCLK signal must not be present. In previous versions of the data sheet, supplying an SLCK with a frequency of < 256kHz triggered this event.

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