Data Sheet

TQP4M9071

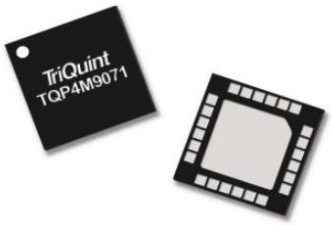
High Linearity 6-Bit 31.5dB Digital Step Attenuator

1. Product Overview and Benefits

The Qorvo® TQP4M9071 is a high linearity, low insertion loss, 6-bit, 31.5dB Digital Step Attenuator (DSA) operating over 0.04-4GHz frequency range. The DSA uses a single positive 3.3V or 5V supply and is with a parallel control interface to control attenuation states. This product maintains high attenuation accuracy over frequency and temperature. No external matching required. This product also comes with an added feature of not requiring external AC ground capacitors for operation above 700MHz.

The TQP4M9071 is available in a standard Lead-Free Green RoHS compliant 24-pin 4x4mm QFN package.

There is also a footprint and pin compatible DSA part available with a serial control interface. Which is Qorvo® TQP4M9072.

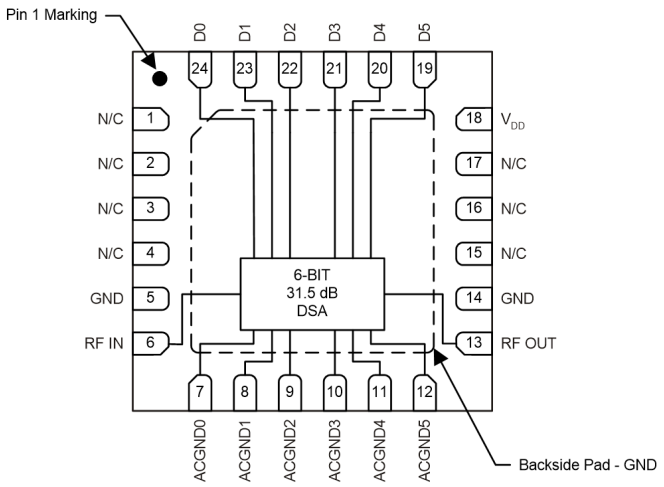


24 Pin 4 x 4 mm leadless QFN Package

3. Key Features

- 0.04-4.0GHz frequency range
- 0.5dB LSB Steps to 31.5dB
- +57dBm Input IP3
- 1.7dB Insertion Loss at 2.2GHz
- TTL Compatible Parallel Control Interface
- No external bypass capacitors required for ≥700MHz Apps
- 50Ω Impedance
- +3.3 or +5V operational voltage

2. Functional Block Diagram



Top View

4. Applications

- Mobile Infrastructure
- LTE/WCDMA/CDMA/EDGE
- Test Equipment and Sensors
- IF and RF Applications
- General Purpose Wireless

5. Ordering Information

Part Number	Description
TQP4M9071TR13	13” T&R with 2500 pieces
TQP4M9071-PCB_IF	40–500MHz Evaluation Board
TQP4M9071-PCB_RF	0.7–4GHz Evaluation Board

Note: EVB comes with USB control interface board

6. Electrical Characteristics

6.1. Absolute Maximum Ratings

Parameter	Conditions	Rating
Storage Temperature		-55 to +150 °C
RF Input Power	50Ω, Temperature +85°C	+28dBm
V_{DD} Supply Voltage		+7.0V
Control Bit Input Voltage		V_{DD}+1V

Operation of this device outside the parameter ranges given above may cause permanent damage.

6.2. Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
V_{DD} Voltage	+3.3	+5.00	+5.25	V
T_{CASE}	-40	-	+105	°C

Electrical specifications are measured at specified test conditions. Performances are not guaranteed over all recommended operating conditions.

6.3. Electrical Specifications

Parameter	Conditions (1)(2)	Min.	Typ.	Max.	Units
Operational Frequency Range		40		4000	MHz
Insertion Loss	1.0GHz		1.3		dB
	2.0GHz		1.6		dB
	2.2GHz		1.7	2.2	dB
	3.5GHz		2.1		dB
Return Loss	All States		17		dB
Attenuation Accuracy	0.04-2.7GHz, All States, Mode 2	± (0.3+3%of Atten. Setting), Max			dB
	0.7-2.7GHz, All States, Mode 1 & 2	± (0.3+3%of Atten. Setting), Max			dB
	2.7-3.5GHz, All States, Mode 1 & 2	± (0.4+4%of Atten. Setting), Max			dB
Attenuation Step	To be monotonic, step attenuation ≥0 required	0	0.5		dB
Input IP3	Input Power +15dBm/tone, All States		+57		dBm
Input P0.1dB	All States, 0.04-4GHz		+30		dBm
Rise or Fall Time	10% ⇆ 90% RF		90		ns
Attenuation Settling Time	50% of Control to 10%/90% between any two states		100		ns
Supply Voltage, V_{DD} (3)			+5		V
Supply Current, I_{DD}			1.4		mA
Control Logic Low Voltage	Pin 19-24, 6-bit TTL compatible parallel control inputs	0		0.8	V
Control Logic High Voltage		2		V_{DD}	V
Control Logic Low Current			5		µA
Control Logic High Current			50		µA

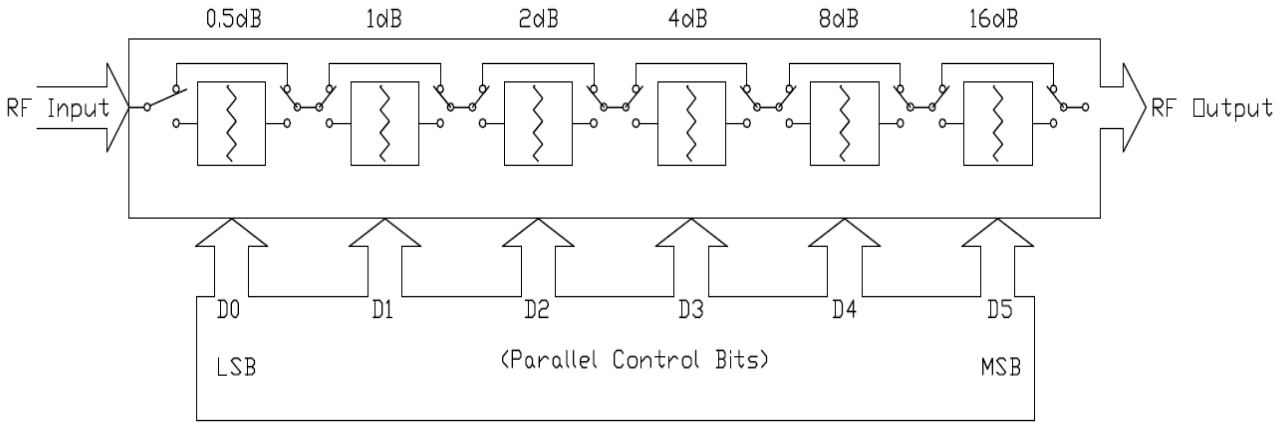
Notes:
1. Test conditions otherwise noted: V_{DD} +5V, Temperature +25C, Mode 1, on Qorvo EVB
2. Mode 1 No external bypass capacitors on Pin 7-12 for 0.7-4GHz applications; Mode 2 with external bypass capacitors for 0.04-4GHz applications
3. This product can be operated at V_{DD} +3.3V with reduced performance.

7. Control Logic Truth Table

LSB	Control Bits			MSB		Attenuation
D0	D1	D2	D3	D4	D5	**Major State**
1	1	1	1	1	1	0dB Reference: IL
0	1	1	1	1	1	0.5dB
1	0	1	1	1	1	1.0dB
1	1	0	1	1	1	2.0dB
1	1	1	0	1	1	4.0dB
1	1	1	1	0	1	8.0dB
1	1	1	1	1	0	16.0dB
0	0	0	0	0	0	31.5dB

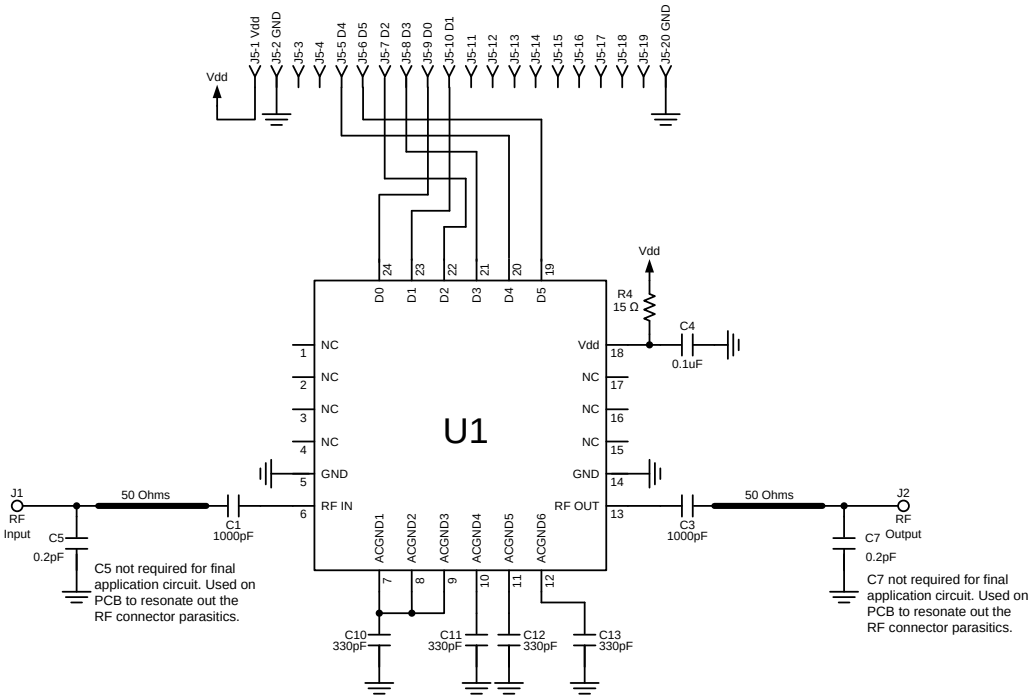
Any combination of the possible 64 states will provide an attenuation of approximately the sum of bit states selected

8. Detail Functional Diagram



9. TQP4M9071-PCB_RF/IF Evaluation Board

9.1. Application Evaluation Board Schematic



Mode 1: 0.7-4.0GHz Operation (TQP4M9071-PCB_RF); No external bypass capacitors required. There are 0.2 pF shunt capacitors (C5 and C7) next to RF connectors, on the application board, to resonate out the RF connector parasitic. These shunt capacitors (C5. C7) are not required in the final application circuit.

Mode 2: 0.04-4.0GHz Operation (TQP4M9071-PCB_IF); For improved operation below 0.1 GHz, the DC blocking and AC bypass capacitors values can be increased to 10 nF. There are 0.2 pF shunt capacitors (C5 and C7) next to RF connectors are not required in the final application circuit.

9.2. Bill of Material: TQP4M9071-PCB_RF

Reference Des.	Value	Description	Manuf.	Part Number
-	-	Printed Circuit Board	Qorvo	-
U1	-	DSA, High Linearity 6-Bit, 31.5dB, 0.5dB Step	Qorvo	TQP4M9071
C1, C3, C8, C9	1000pF	CAP, 1000pF, 10%, 50V, C0G, 0402	various	-
C4	0.1µF	CAP, 0.1µF, 20%, 16V, 0402	various	-
R1	15Ω	RES, 15Ω, 5%, 1/16W, 0402	various	-
C10, C11, C12, C13	-	Not Installed	-	-

9.3. Bill of Material: TQP4M9071-PCB_IF

Reference Des.	Value	Description	Manuf.	Part Number
-	-	Printed Circuit Board	Qorvo	-
U1	-	DSA, High Linearity 6-Bit, 31.5dB, 0.5dB Step	Qorvo	TQP4M9071
C1, C3, C8, C9	1000pF	CAP, 1000pF, 10%, 50V, C0G, 0402	various	-
C4	0.1µF	CAP, 0.1µF, 20%, 16V, 0402	various	-
R1	15Ω	RES, 15Ω, 5%, 1/16W, 0402	various	-
C10, C11, C12, C13	330pF	CAP, 330pF, 10%, 50V, 0402Not Installed	various	-

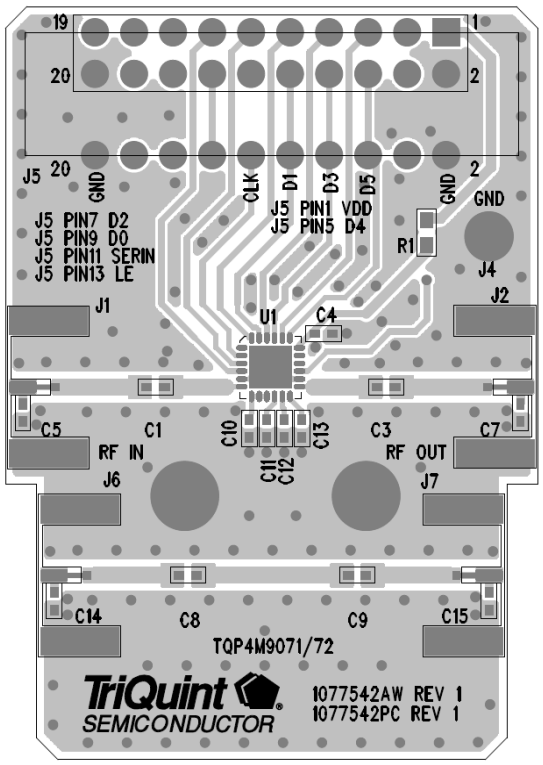
9.4. TQP4M9071-PCB_RF/IF EVB Layout

Top RF layer is .020" Rogers-4003, ϵ_r = 3.45, 4 layers total 0.062" for mechanical rigidity. Metal layers are 1-oz copper. RF trace: width = .040", spacing = .020".

External DC blocking capacitors are required on RF IN and RF OUT pins of the device. The supply voltage for the DSA is supplied externally through pin V_{DD}. Frequency bypassing for this pin is supplied by surface mount capacitor 0.1µF (C4). This capacitor is placed close to the device pin in the board layout. To ensure application circuit is compatible with different standard power supplies, 15Ω (R1) dropping resistor is highly recommended on V_{DD} supply line.

RF layout is critical for getting the best performance RF trace impedance needs to be 50Ω. For measuring the actual device performance on connectorized PC board, losses due to RF traces need could be subtracted from the data measured through SMA connectors. The RF through line between J6 & J7 estimates the PCB trace loss for removal from the evaluation board measured data. All data shown on the data sheet is with trace losses deducted.

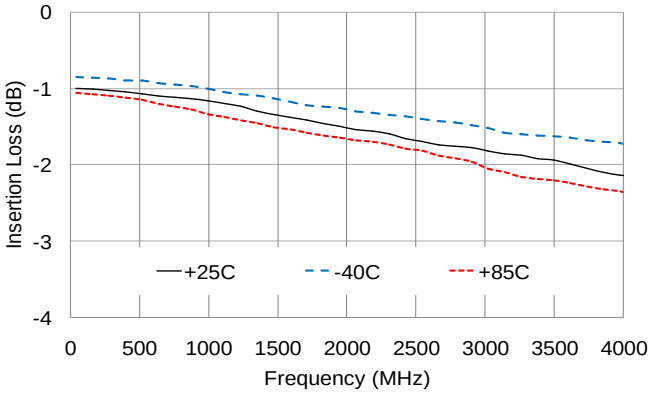
The PC board is designed with the connector for the USB control interface board, Evaluation Board Host (EVH). Each TQP4M9071 evaluation board is supplied with the EVH board and USB cable. The graphical user interface (GUI) for attenuation state setting, User Manual are available on Qorvo website.



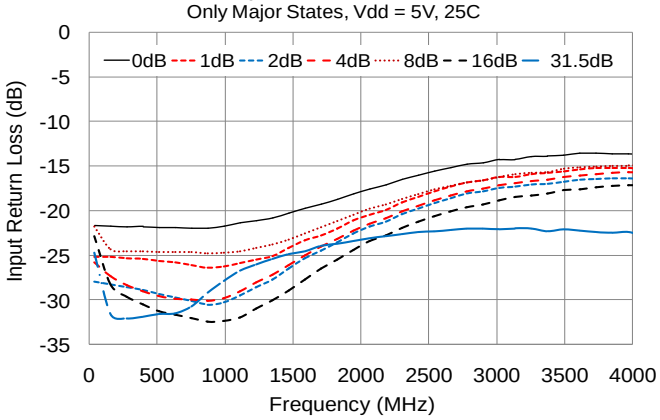
10. Typical Performance Plots

Performance plots data is measured using Bias Tee on RF ports in Mode 2 configuration. Mode 2 operation is required to obtain performance at frequencies lower than 0.7 GHz. For frequency range 0.7 – 4.0 GHz, data is identical in Mode 1 and Mode 2.

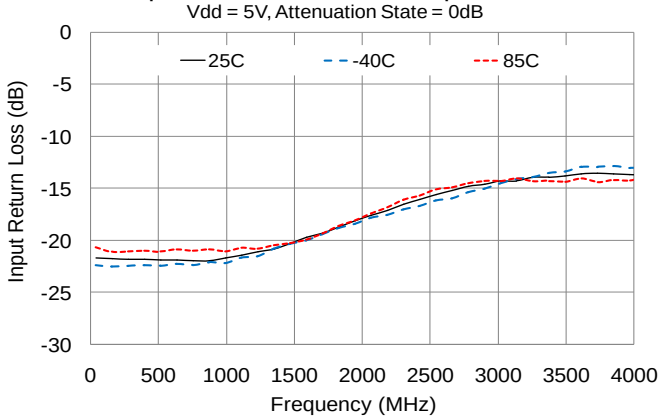
Insertion Loss
Vdd = 5V



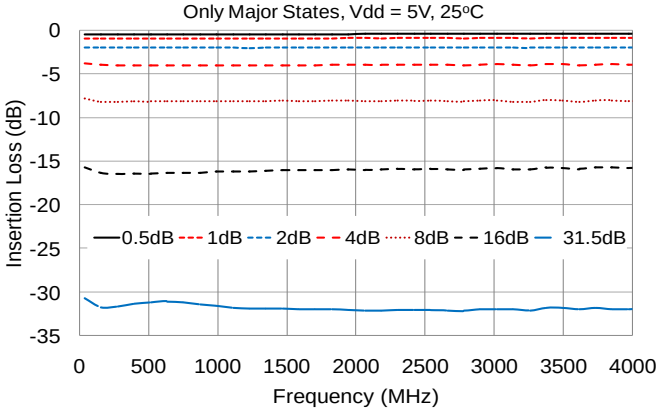
Input Return Loss
Only Major States, Vdd = 5V, 25C



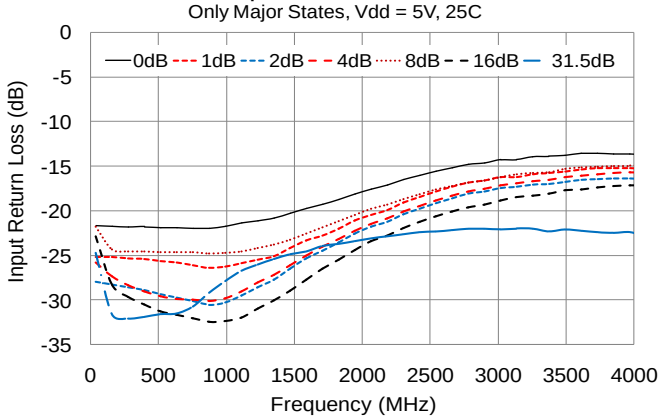
Input Return Loss vs. Temperature
Vdd = 5V, Attenuation State = 0dB



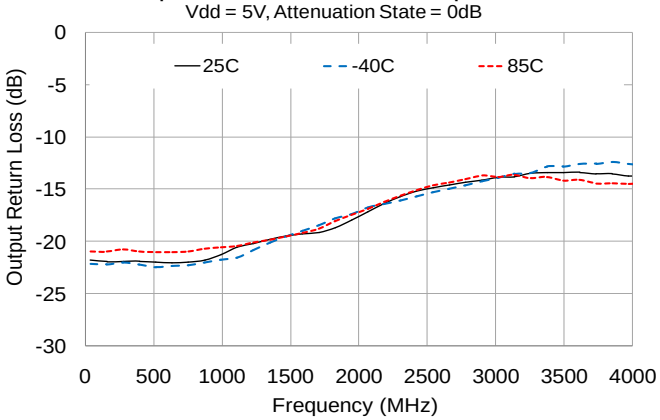
Attenuation
Only Major States, Vdd = 5V, 25°C



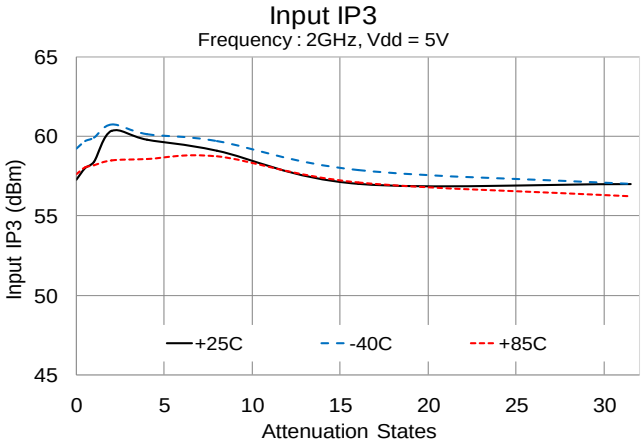
Input Return Loss
Only Major States, Vdd = 5V, 25C

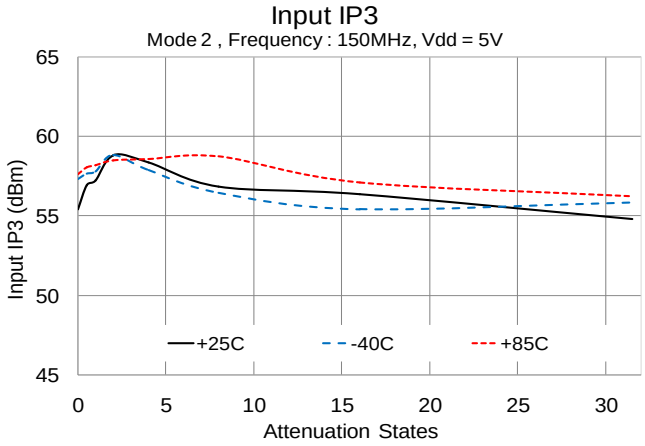


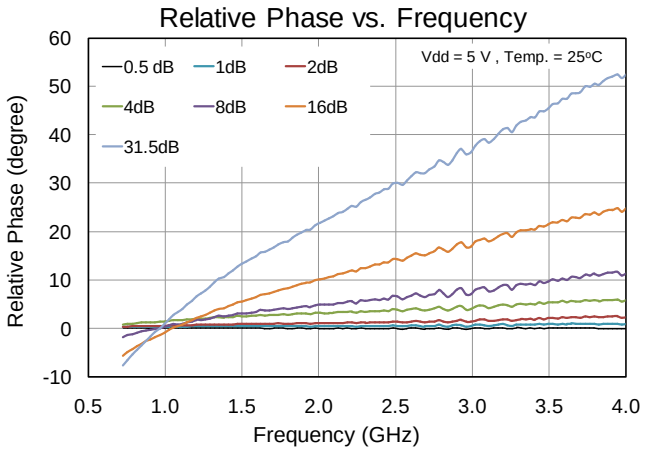
Output Return Loss vs. Temperature
Vdd = 5V, Attenuation State = 0dB

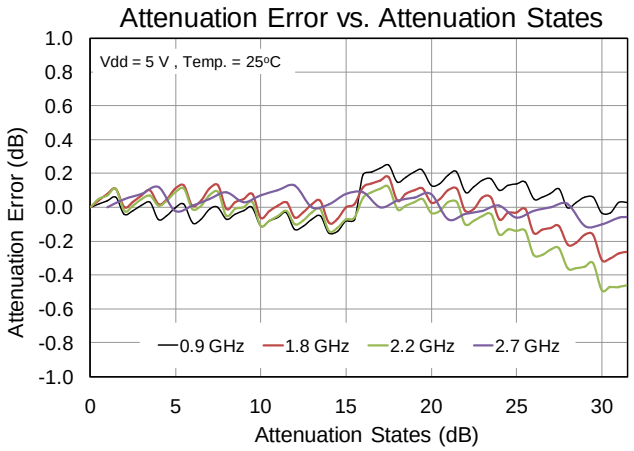


Performance plots data is measured using Bias Tee on RF ports in Mode 2 configuration. Mode 2 operation is required to obtain performance at frequencies lower than 0.7 GHz. For frequency range 0.7 – 4.0 GHz, data is identical in Mode 1 and Mode 2.

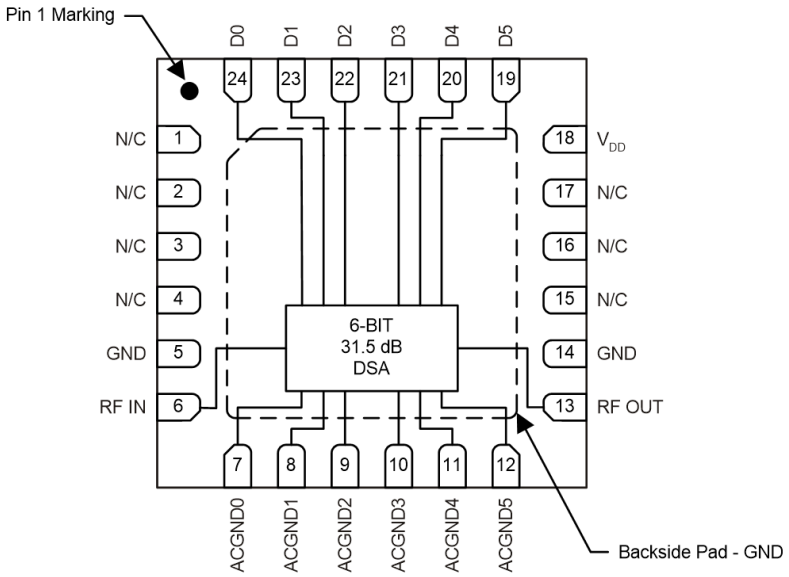








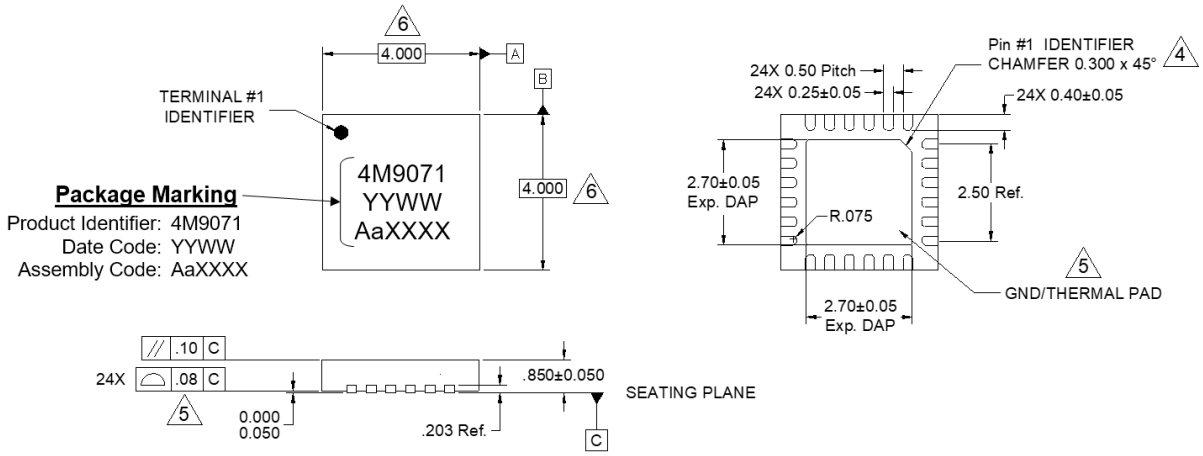
11. Pin Configuration and Description



Pin Number	Label	Description
1, 2, 3, 4, 15, 16, 17	N/C	No electrical connection. Land pads should be provided on PCB for mounting integrity.
5,14	GND	Ground connection pads must be connected to RF/DC ground
6	RF IN	RF Input, DC voltage present, blocking capacitor required
7	ACGND0	AC grounding for low frequency operation
8	ACGND1	AC grounding for low frequency operation
9	ACGND2	AC grounding for low frequency operation
10	ACGND3	AC grounding for low frequency operation
11	ACGND4	AC grounding for low frequency operation
12	ACGND5	AC grounding for low frequency operation
13	RF OUT	RF Output, DC voltage present, blocking capacitor required
18	VDD	DC Voltage Supply input, bypass capacitor close to pin required
19	D5	Logic Control bit 5, 16dB step attenuator
20	D4	Logic Control bit 4, 8dB step attenuator
21	D3	Logic Control bit 3, 4dB step attenuator
22	D2	Logic Control bit 2, 2dB step attenuator
23	D1	Logic Control bit 1, 1dB step attenuator
24	D0	Logic Control bit 0, 0.5dB step attenuator
Backside Pad	Ground	Ground connection. The back side of the package should be connected to the ground plane though as short of a connection as possible. PCB via holes under the device are required.

12. Packaging Information

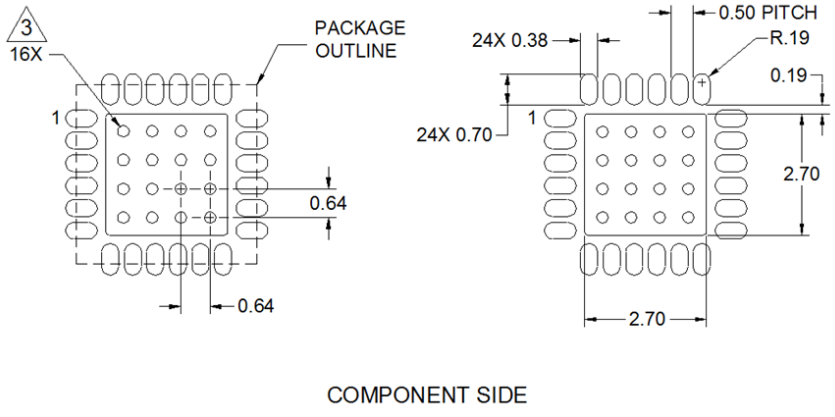
12.1. Device Marking and Package Dimensions



Notes:

1. All dimensions are in mm. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
5. Co-planarity applies to the exposed ground/thermal pad as well as the contact pins.
6. Package body length/width does not include plastic flash protrusion across mold parting line.

12.2. PCB Footprint Recommendations



Notes:

1. All dimensions are in mm. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. Via holes should use a 0.35mm (#80 / .0135") diameter drill and have a final plated through diameter of 0.25 mm (.010").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

13. Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	ESDA/JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

14. Solderability

Compatible with both lead-free (260 °C max. reflows temperature) and tin/lead (245 °C max. reflow temperature) soldering processes. Solder profiles available upon request.

Package lead plating: Annealed Matte Tin

15. Environmental Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- SVHC Free
- PFOS Free
- Lead Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: +1 844-890-8163

Email: customer.support@qorvo.com

Important Notices

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