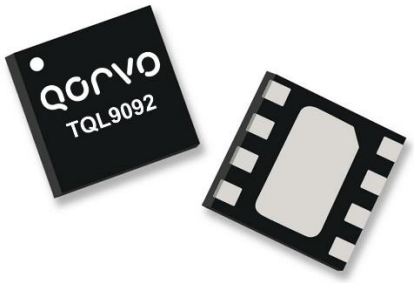
TQL9092

Ultra-Low Noise, Flat Gain LNA



8 Pin 2X2 mm DFN Package

General Description

The TQL9092 is a flat-gain, high-linearity, ultra-low noise amplifier in a small 2 x 2 mm surface-mount package. The LNA provides a gain flatness of 2 dB (peak-to-peak) over a wide bandwidth from 1.5 to 3.6GHz. At 2.6 GHz, the amplifier typically provides 22.6 dB gain, +39.5 dBm OIP3 at a 65 mA bias setting, and 0.6 dB noise figure. The LNA can be biased from a single positive supply ranging from 3.3 to 5 volts. The device is housed in a green/RoHS-compliant industry-standard 2x2 mm package.

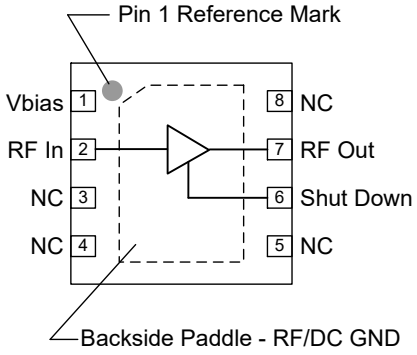
The TQL9092 is internally matched using a high-performance E-pHEMT process and only requires five external components for operation from a single positive supply: an external RF choke and blocking/bypass capacitors and a bias resistor going to pin 1. This LNA integrates a shut-down biasing capability to allow for operation in TDD applications.

The TQL9092 is optimized for linear performance across the 1.5 to 4.2 GHz frequency band but can operate down to 600 MHz.

Product Features

- 0.6-4.2 GHz Operational Bandwidth
- Ultra-low noise figure, 0.6 dB NF @ 2.6 GHz
- >20 dB gain across 1.5 to 3.8 GHz
- Flat 2 dB gain variation across 1.5 to 3.6GHz
- Bias adjustable for linearity optimization
- 37 dBm OIP3 at 65mA I_{DD}
- Shut-down mode pin with 1.8V Logic
- Unconditionally stable
- Integrated shutdown control pin
- Maintains OFF state with high Pin drive
- +3V to +5V supply; does not require -Vgg

Functional Block Diagram



Top View

Applications

- Repeaters / DAS
- Mobile Infrastructure
- LTE / WCDMA / CDMA / GSM
- General Purpose Wireless
- TDD or FDD systems

Ordering Information

Part No.	Description
TQL9092	Ultra-low noise, Flat Gain LNA
TQL9092-PCB	0.6-4.2 GHz Evaluation Board

Standard T/R size = 2500 pieces on a 7” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to +150°C
Operation Case Temperature	−40 to +125°C
Supply Voltage (V_{DD})	+7 V
RF Input Power, CW, 50Ω, T=25°C	+33 dBm
RF Input Power, WCDMA, 10dB PAR	+27 dBm
RF Input Power, CW, OFF State	+33 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{DD})	3.3	5.0	5.25	V
T_{CASE}	−40		+105	°C
Tj for >10^6 hours MTTF			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD} =+5V, Temp=+25°C, 50 Ω system.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		600		4200	MHz
Test Frequency			2600		MHz
Gain		21	22.6	24.5	dB
Gain Flatness	1500-3600MHz		2.0		dB
Input Return Loss			11		dB
Output Return Loss			17		dB
Noise Figure (1)			0.65	0.95	dB
Output P1dB			+19		dBm
Output IP3	Pout=+5 dBm/tone, Δf=1 MHz	+33	+37		dBm
Power Shutdown Voltage (pin 6)	On state	0		0.63	V
	Off state (Power down)	1.17		V_{DD}	V
Current, I_{DD}	On state	45	65	85	mA
	Off state (Power down)		3		mA
Power Shutdown Current (pin 6)	V_{PD} ≥ 1.17 V		140		µA
Switching Time	LNA ON to OFF		583		ns
	LNA OFF to ON		216		ns
Thermal Resistance, θ_{jc}	channel to case		48		°C/W

Note:
1. Input trace loss deducted.

S-Parameters

Test Conditions: V_{DD}=+5 V, I_{DD}=65 mA (typ.), T=+25°C, 50 Ω system, Reference planes at device pins

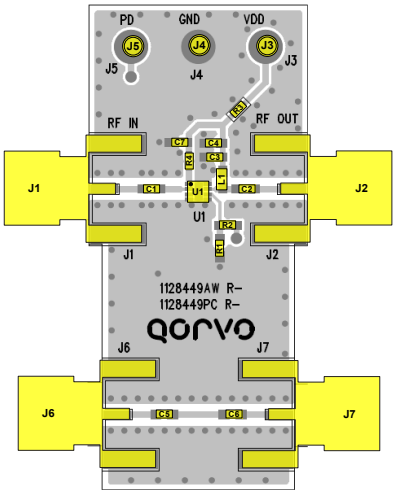
Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
0.6	-11.76	-50.69	23.21	75.64	-32.67	3.34	-17.78	-82.70
0.7	-12.71	-50.64	22.61	64.33	-32.32	-0.10	-19.37	-95.95
0.8	-13.48	-49.70	22.07	53.89	-32.07	-3.77	-21.01	-111.25
0.9	-13.97	-47.94	21.62	44.25	-31.88	-7.51	-22.57	-127.54
1.0	-14.17	-46.01	21.24	35.23	-31.74	-11.34	-24.09	-146.47
1.1	-14.12	-44.61	20.95	26.72	-31.66	-15.27	-25.21	-170.38
1.2	-13.85	-44.30	20.72	18.67	-31.60	-19.21	-25.32	163.93
1.3	-13.51	-45.93	20.57	10.97	-31.58	-23.13	-24.42	142.26
1.4	-13.22	-48.66	20.45	3.55	-31.58	-27.21	-23.14	125.62
1.5	-13.03	-52.44	20.40	-3.55	-31.60	-31.21	-22.30	112.36
1.6	-12.87	-56.00	20.40	-10.53	-31.66	-35.36	-21.21	99.97
1.7	-12.74	-60.59	20.44	-17.40	-31.73	-39.63	-20.45	90.85
1.8	-12.57	-64.83	20.53	-24.24	-31.81	-44.05	-19.74	80.82
1.9	-12.32	-70.61	20.65	-31.05	-31.91	-48.65	-19.19	74.07
2.0	-12.15	-77.39	20.82	-37.89	-32.00	-53.53	-18.89	65.49
2.1	-11.91	-85.11	21.01	-44.83	-32.11	-58.82	-18.73	57.48
2.2	-11.84	-94.45	21.26	-51.96	-32.22	-64.28	-18.88	49.58
2.3	-11.71	-103.32	21.48	-59.27	-32.33	-70.14	-19.01	40.16
2.4	-11.58	-114.41	21.77	-66.85	-32.45	-76.66	-19.75	31.25
2.5	-11.36	-125.29	22.03	-74.82	-32.56	-83.41	-20.68	19.64
2.6	-10.75	-137.87	22.35	-83.11	-32.51	-92.09	-22.11	1.63
2.7	-10.51	-152.17	22.54	-92.23	-32.96	-100.23	-25.45	-16.73
2.8	-9.95	-166.24	22.71	-101.40	-33.19	-109.01	-29.13	-56.17
2.9	-9.36	179.27	22.86	-111.02	-33.45	-118.56	-27.48	-118.31
3.0	-8.79	164.95	22.88	-121.01	-33.76	-128.78	-22.59	-154.88
3.1	-8.27	150.82	22.83	-131.17	-34.10	-139.39	-19.03	-173.88
3.2	-7.79	137.73	22.61	-141.31	-34.47	-150.14	-16.31	170.67
3.3	-7.41	124.99	22.32	-151.26	-34.84	-160.90	-14.19	158.49
3.4	-7.15	113.98	21.90	-160.90	-35.23	-171.42	-12.59	146.44
3.5	-6.96	103.20	21.40	-169.96	-35.60	178.70	-11.16	137.22
3.6	-6.82	94.04	20.87	-178.58	-35.91	169.44	-10.25	128.56
3.7	-6.79	85.65	20.27	173.50	-36.16	161.01	-9.49	120.64
3.8	-6.81	77.65	19.67	166.05	-36.31	153.47	-8.97	113.48
3.9	-6.92	70.51	19.02	159.20	-36.36	146.55	-8.48	106.15
4.0	-7.10	63.84	18.40	152.87	-36.34	140.32	-8.08	99.85

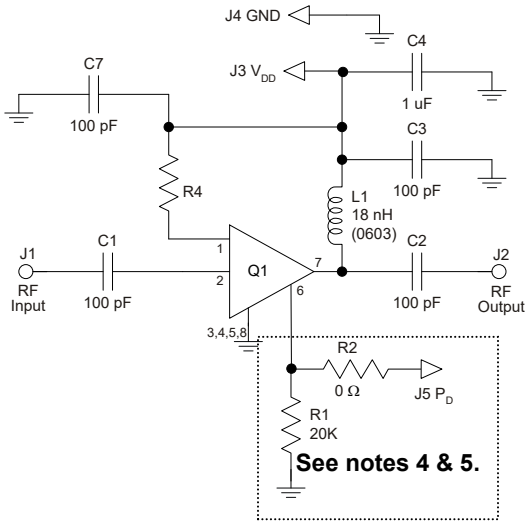
Noise Parameters

Test conditions: V_{DD}=+5 V, I_{DD}=65 mA (typ.), Temp=+25°C, 50 Ω system, Reference planes at device pins

Freq (GHz)	NF_{min} (dB)	GammaOpt (mag)	GammaOpt (deg)	Rn (Ω)
1.70	0.55	0.28	60.75	3.91
1.80	0.55	0.28	64.92	3.80
1.90	0.55	0.28	69.08	3.70
2.00	0.54	0.28	73.23	3.59
2.10	0.54	0.28	77.36	3.48
2.20	0.54	0.28	81.47	3.37
2.30	0.54	0.28	85.55	3.26
2.40	0.54	0.28	89.61	3.16
2.50	0.54	0.28	93.63	3.06
2.60	0.55	0.28	97.62	2.96
2.70	0.55	0.28	101.57	2.87
2.80	0.56	0.28	105.48	2.79
2.90	0.56	0.27	109.33	2.71
3.00	0.57	0.27	113.12	2.65
3.10	0.58	0.27	116.85	2.59
3.20	0.59	0.26	120.52	2.54
3.30	0.61	0.26	124.11	2.51
3.40	0.62	0.26	127.62	2.48
3.50	0.64	0.25	131.04	2.47
3.60	0.66	0.25	134.38	2.47
3.70	0.68	0.24	137.62	2.48
3.80	0.70	0.23	140.76	2.50
3.90	0.72	0.23	143.79	2.54
4.00	0.75	0.22	146.70	2.60
4.10	0.78	0.21	149.50	2.67
4.20	0.81	0.21	152.18	2.75

TQL9092-PCB Evaluation Board





Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. R3 (0 Ω jumper) is not shown on the schematic and may be replaced with copper trace in the target application layout.
3. All components are of 0402 size unless stated on the schematic.
4. For TDD Applications: R1 = 20K & R2 = 0Ω
5. For FDD Applications: R1 = 20K 'OR' Pin 6 tied to ground. R2 = DNP/Omitted
6. A through line is included on the evaluation board to de-embed the board losses.
7. R4 sets the current draw. Can be changed for the desired bias point. See table below.

Bill of Material – TQL9092-PCB

Reference Des.	Value	Description	Manuf.	Part Number
-	-	Printed Circuit Board	Qorvo	
U1	-	Ultra Low Noise, Flat Gain LNA	Qorvo	TQL9092
R4	5.1K	RES, 5.1K, 5%, 1/16W, 0402	various	
R1	20K	RES, 20K, 5%, 1/16W,0402	various	
R2, R3	0 Ω	RES, 0 Ω, 1/16W, 0402	various	
L1	18 nH	IND, 18 nH, 5%, Ceramic, 0603	various	
C4	1.0 µF	CAP, 1.0 µF, 10%, 10V, X5R, 0402	various	
C1, C2, C3, C5, C6	100 pF	CAP, 100 pF, 5%, 50V, NPO/C0G, 0402	various	

R4 Resistor Values for Various I_{DD} settings

I_{DD} (mA)	45	55	65	75	85	95	105	115
R4	9.2K	6.5K	5.1K	3.9K	3.1K	2.6K	2.2K	1.8K

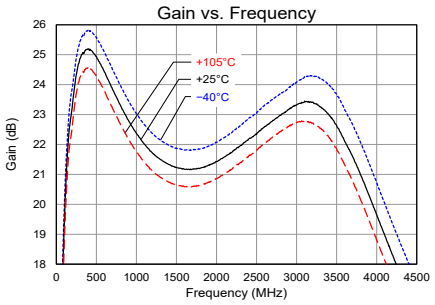
Typical Performance – TQL9092-PCB

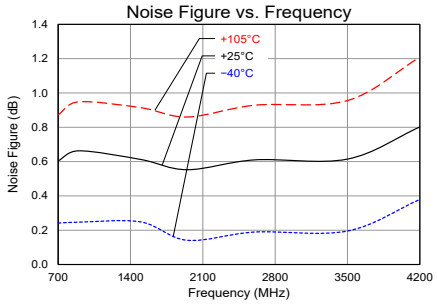
Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD}=65 mA (typ.), Temp=+25°C

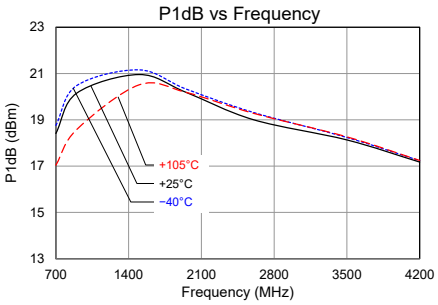
Parameter	Conditions	Typical Values					Units
Frequency		900	1950	2600	3500	4200	MHz
Gain		22.8	21.3	22.6	22.6	18.3	dB
Input Return Loss		13.5	10	10.5	11.8	9.2	dB
Output Return Loss		33	27	17	18	10.2	dB
Output P1dB		+20.1	+20.2	+19	+18.3	+17.2	dBm
OIP3	Pout=+5 dBm/tone, Δf=1 MHz	+34	+38.4	+39.2	+37.6	+35.8	dBm
OIP3	Pout=+5 dBm/tone, Δf=1 MHz I_{DD} = 80 mA	+40	+35.7	+34.7	+32.8		dBm
Noise figure	EVB input trace loss deducted	0.66	0.55	0.6	0.6	0.8	dB

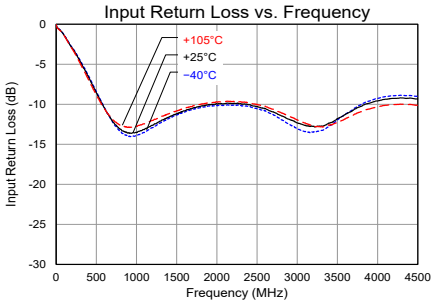
Performance Plots – TQL9092-PCB

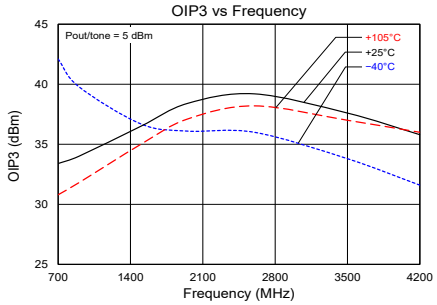
Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD} = 65mA, Temp=+25°C. Noise figure data has input trace loss deducted.

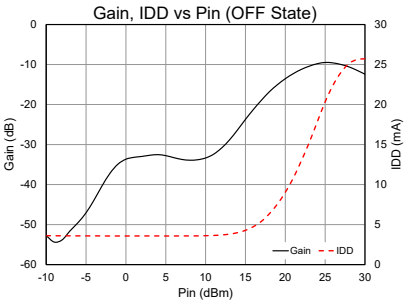


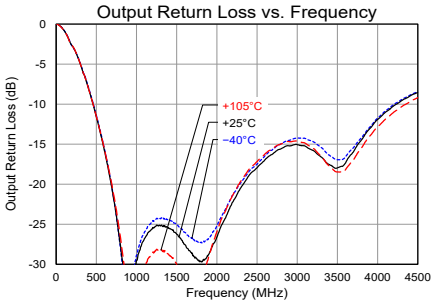


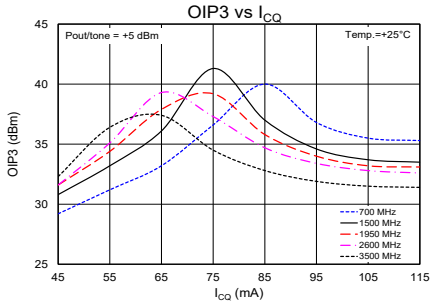


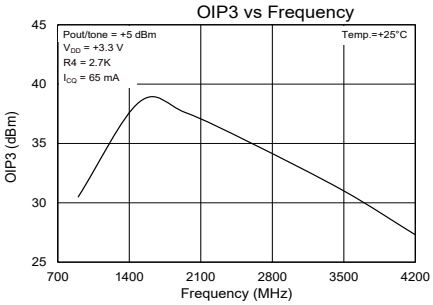












TQL9092 3.3V V_{DD} Operation

This page provides performance data when operating at 3.3V V_{DD} with 65mA and 80mA I_{DD}. The current level was adjusted with the following resistor setting on the evaluation board. Please refer to page 4 for PCB schematic and layout.

R4 = 2.4K for I_{DD} = 65mA
R4 = 1.6K for I_{DD} = 80mA

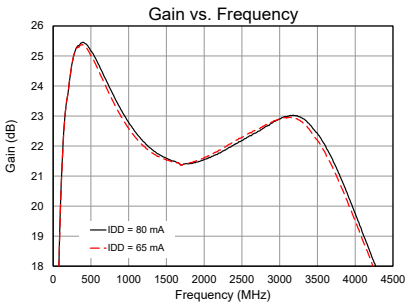
Typical Performance – VDD = 3.3V

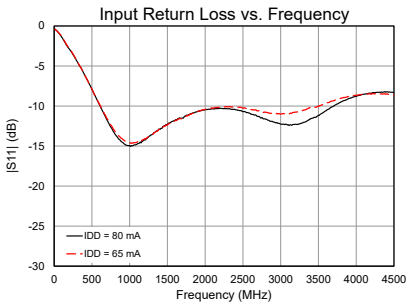
Test conditions unless otherwise noted: V_{DD}=+3.3 V, Temp=+25°C

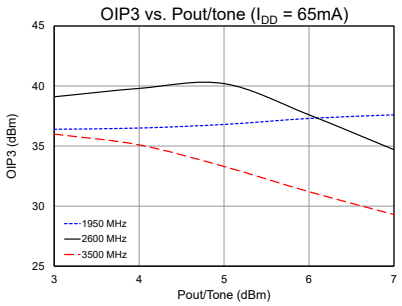
Parameter	Conditions	Typical Values						Units
Frequency		1950		2600		3500		MHz
I_{DD}		65	80	65	80	65	80	mA
Gain		21.5	21.5	22.4	22.3	22.2	22.4	dB
Input Return Loss		10.5	10.5	10.5	11	10	11	dB
Output Return Loss		26	26	18	18	18	20	dB
Output P1dB		+18.5	+18.7	+17.4	+17.6	+16	+15.8	dBm
OIP3	Pout=+5 dBm/tone, Δf=1 MHz	+36.8	+35.7	+40.2	+38.8	+33.3	+35.3	dBm
Noise figure	Input trace loss deducted	0.43	0.42	0.52	0.51	0.74	0.74	dB

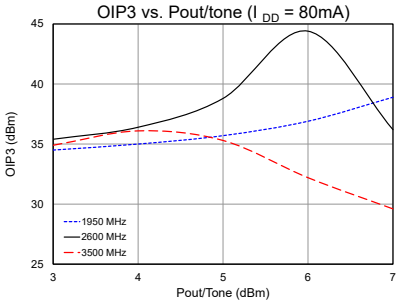
Performance Plots – TQL9092-PCB at V_{DD} = 3.3V

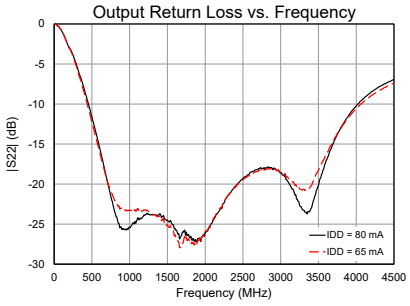
Test conditions unless otherwise noted: V_{DD}=+3.3 V, Temp=+25°C. Noise figure data has input trace loss deducted.

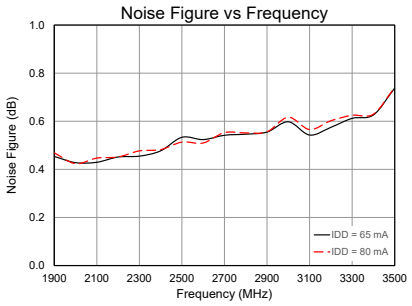




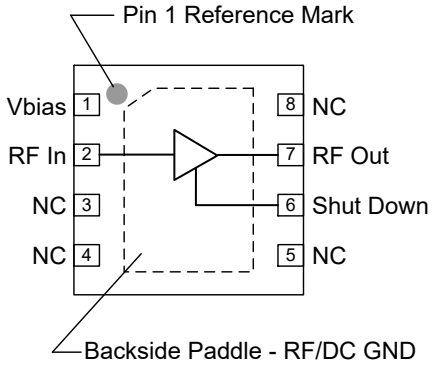








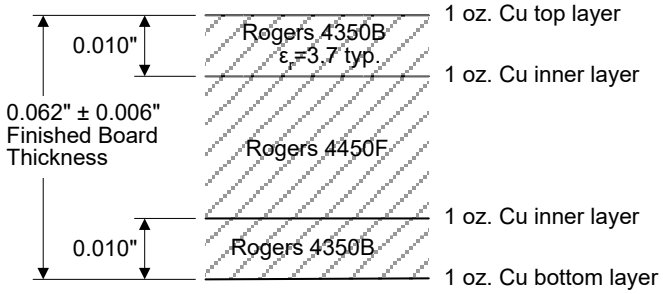
Pin Configuration and Description



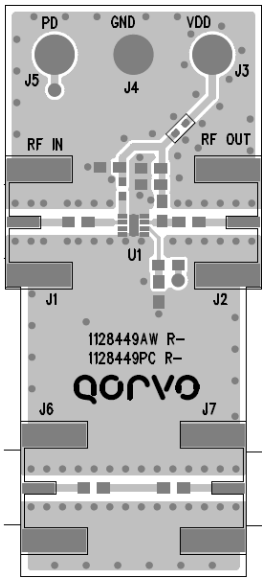
Pin No.	Label	Description
1	Vbias	Sets I_{DD} for the device.
2	RF In	RF Input pin. DC Block is required.
6	Shut Down	A high voltage ≥1.17V turns off the device. If the pin is pulled to ground or driven with a voltage ≤0.63V, then the device will operate under LNA ON state.
7	RF Out	RF Output pin, DC Block is required. It is also a DC supply Input pin. A RF choke or inductor is required for operation.
3, 4, 5, 8	NC	No electrical connection. Provide grounded land pads for PCB mounting integrity.
Backside Paddle	RF/DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance; see PCB Mounting Pattern for suggested footprint.

Evaluation Board PCB Information

Qorvo PCB 1128449 Material and Stack-up

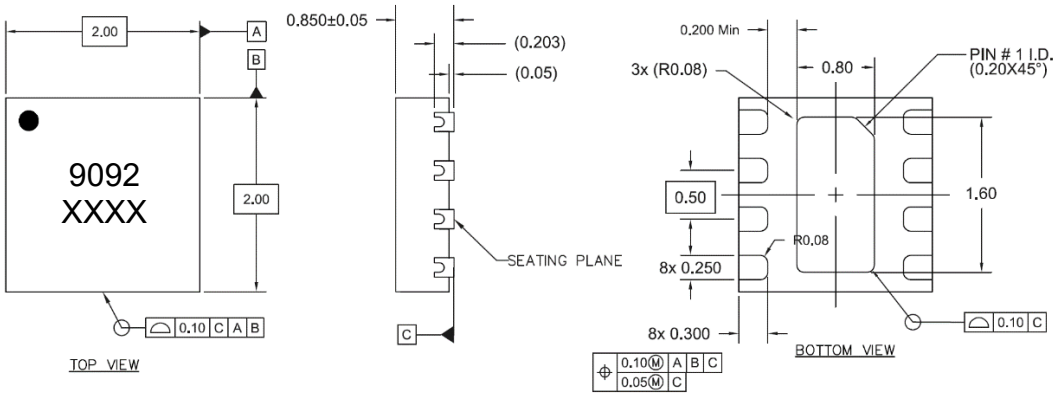


50 Ω line dimensions: width = 0.020”, spacing = 0.032”



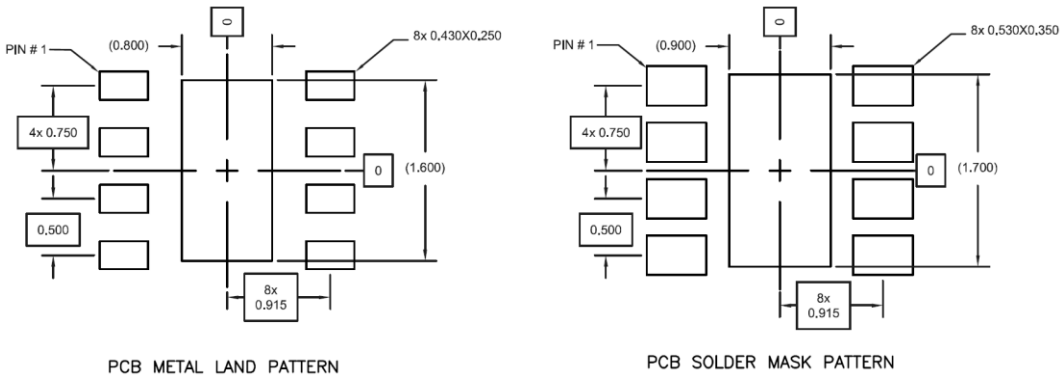
Package Marking and Dimensions

Marking: ● – Pin 1 Marker
9092 – Part Number
XXXX – Lot Code



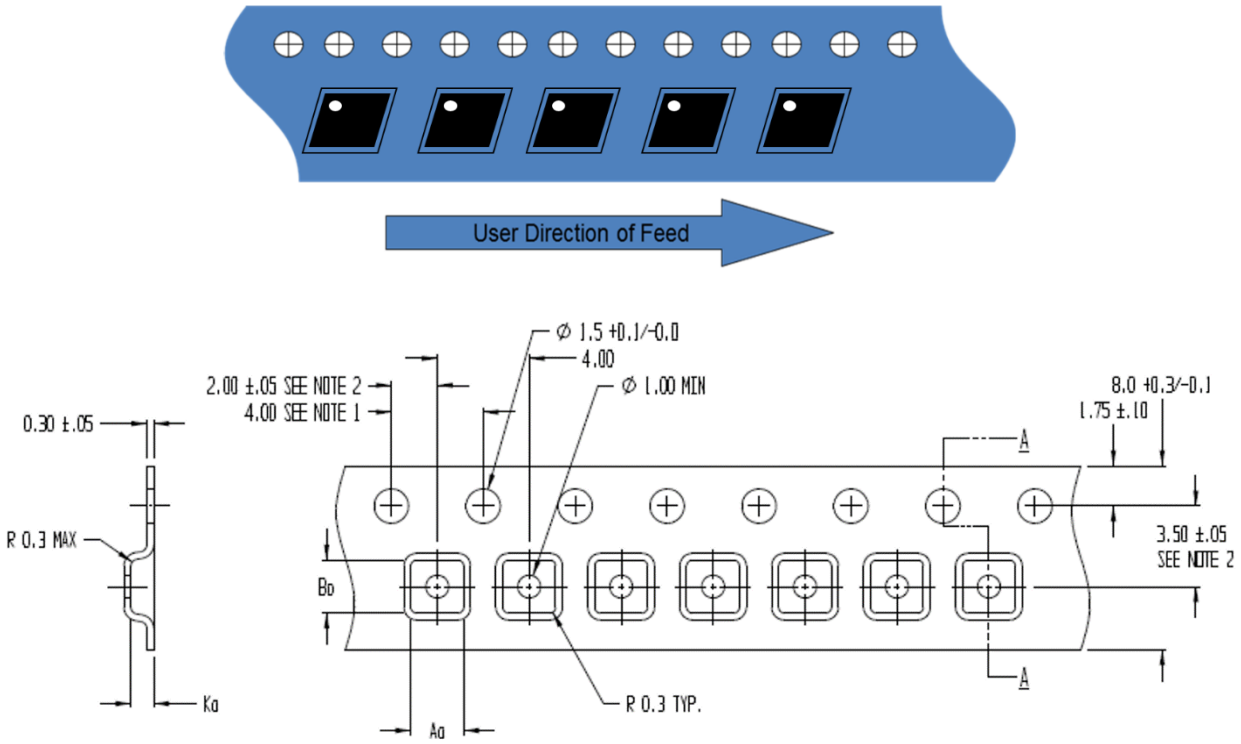
Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Minimum 3 via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated through diameter of 0.25 mm (0.010”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

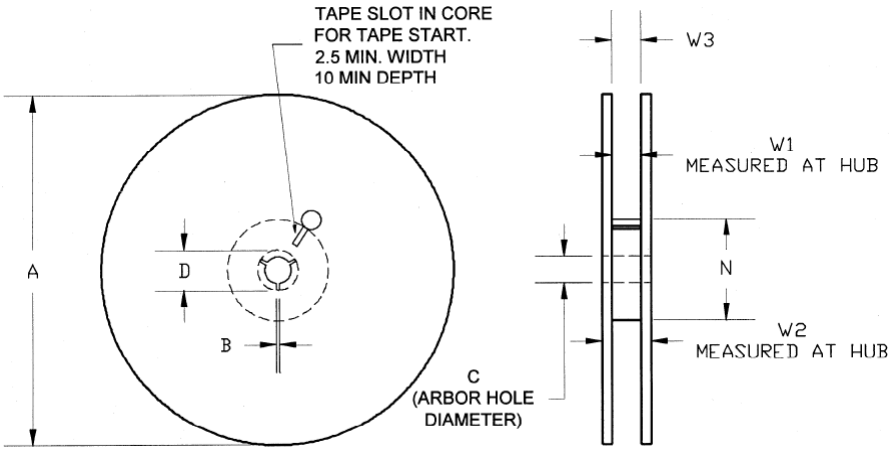
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.091	2.30
	Width	B0	0.091	2.30
	Depth	K0	0.051	1.30
	Pitch	P1	0.157	4.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.138	3.50
Cover Tape	Width (Reference Only)	C	0.213	5.40
Carrier Tape	Width	W	0.315	8.00

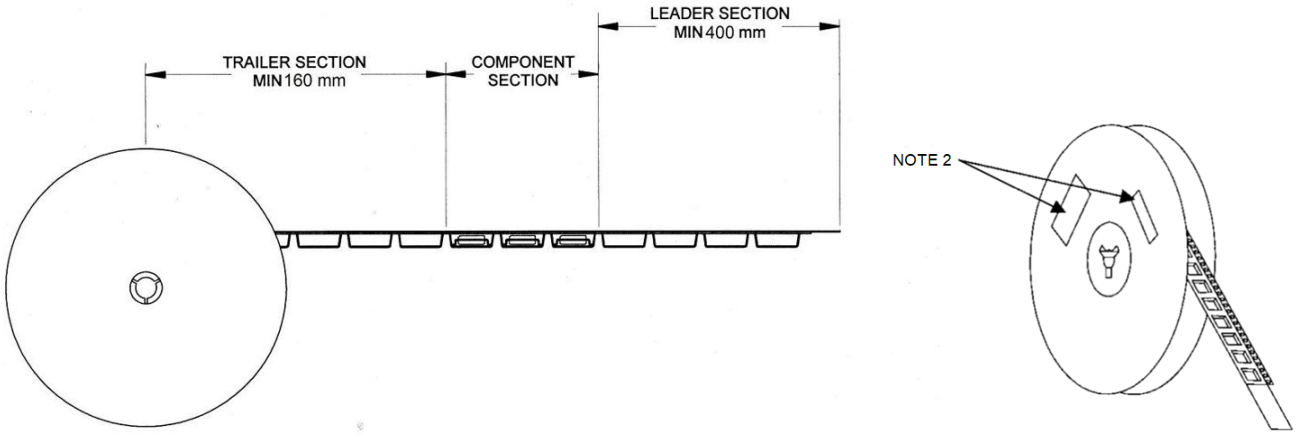
Tape and Reel Information – Reel Dimensions

Standard T/R size = 2,500 pieces on a 7” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	6.969	177.0
	Thickness	W2	0.559	14.2
	Space Between Flange	W1	0.346	8.80
Hub	Outer Diameter	N	2.293	58.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	ESDA / JEDEC JS-001-2014
ESD – Charged Device Model (CDM)	Class C3	ESDA / JEDEC JS-002-2014
MSL – Moisture Sensitivity Level	Level 1	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with lead-free (260°C max. reflow temp.) soldering process.
Solder profiles available upon request.

Contact plating: NiPdAu *(Thickness: Ni 0.508 ~1.524 µm; Pd 0.023 ~ 0.1016 µm; Au 0.00254 ~ 0.01016 µm)*

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com
Tel: 1-844-890-8163
Email: customer.support@qorvo.com

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