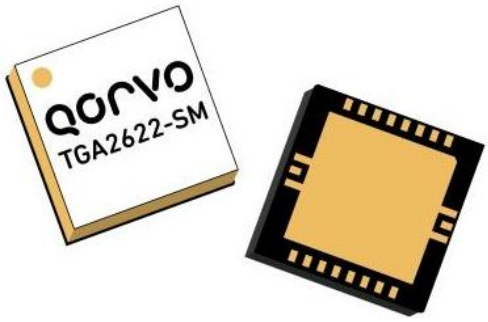
TGA2622-SM

9 – 10 GHz 35 Watt GaN Power Amplifier



QFN 7x7 mm 22L

Product Description

Qorvo's TGA2622-SM is a packaged, high power X-Band amplifier fabricated on Qorvo's production 0.25um GaN on SiC process. Operating from 9-10GHz, the TGA2622-SM typically generates 35W of saturated output power with a power-added efficiency greater than 42% and 27.5dB of large signal gain.

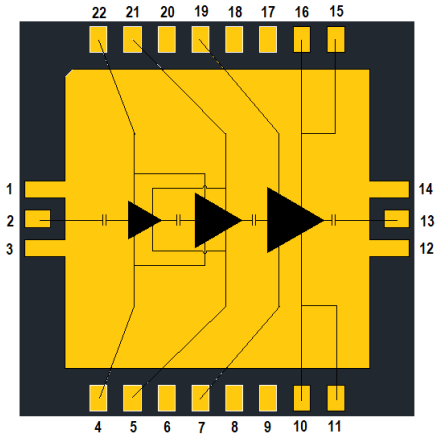
The TGA2622-SM is packaged in a 7x7mm air-cavity, laminate based QFN. Both RF ports are internally DC blocked and matched to 50 ohms enabling simple system integration. Ideally suited for pulsed applications, the TGA2622-SM offers superior power, PAE and gain performance that can save costs on existing platforms while enabling the development of future systems.

Product Features

- Frequency Range: 9 – 10 GHz
- P_{SAT}: 45.5 dBm @ P_{IN} = 18 dBm
- PAE: 42% @ P_{IN} = 18 dBm
- Power Gain: 27.5 dB @ P_{IN} = 18 dBm
- Bias: V_D = 28 V, I_{DQ} = 290 mA
  (Pulsed V_D: PW = 100 us and DC = 10 %)
- Package Dimensions: 7 x 7 x 1.64 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Weather and Marine Radar

Ordering Information

Part	Description
TGA2622-SM	9 – 10 GHz 35 W GaN Power Amplifier
TGA2622-SM EVB	Evaluation Board

Absolute Maximum Ratings

Parameter	Value
Drain Voltage (V_D)	40 V
Gate Voltage Range (V_G)	-8 to 0V
Drain Current (I_D)	4.3 A
Gate Current (I_G)	See page 11
Power Dissipation (P_{DISS}), 85°C, CW	88 W
Input Power (P_{IN}), CW, 50Ω, V_D = 28V, 85°C	24 dBm
Input Power (P_{IN}), CW, VSWR 3:1, V_D = 28V, 85°C	24 dBm
Mounting Temperature (30 seconds)	260 °C
Storage Temperature	-55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Drain Voltage (V_D)	28 V
Drain Current (quiescent, I_{DQ})	290 mA
Gate Voltage Range (V_G)	−2.8 to −2.0 V
Operating Temperature Range	−40 to 85 °C

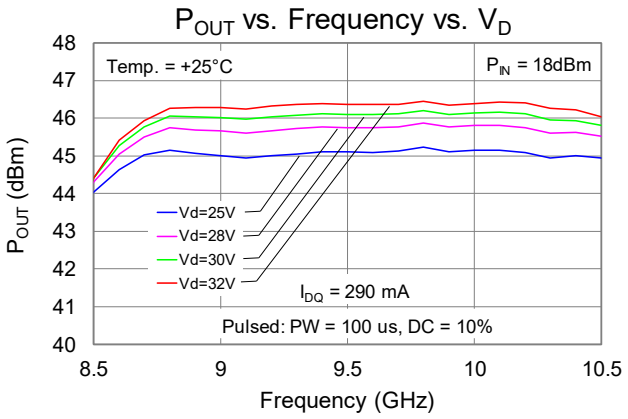
Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

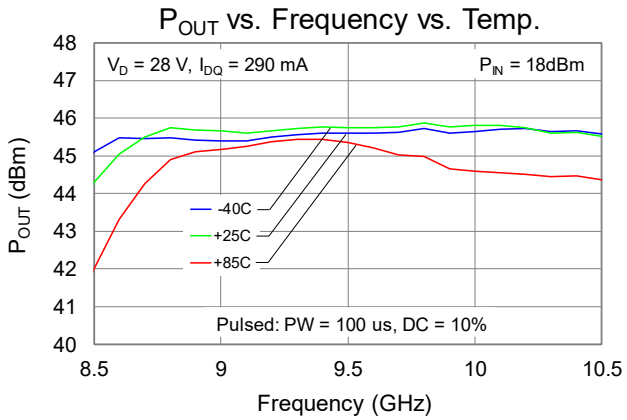
Electrical Specifications

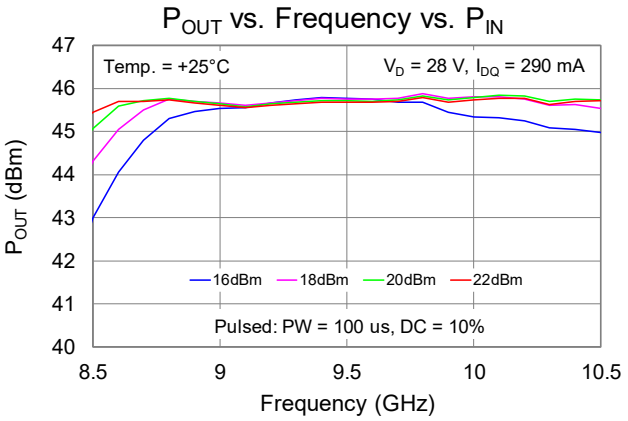
Test conditions unless otherwise noted: 25 °C, V_D = 28 V, I_{DQ} = 290 mA, Pulsed V_D: PW = 100 us, DC = 10%

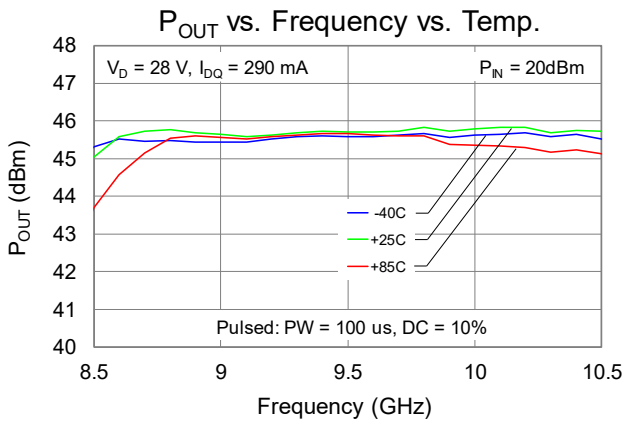
Parameter		Min	Typ	Max	Units
Operational Frequency Range		9	–	10	GHz
Output Power @ P_{IN} = 18 dBm	Frequency = 9 GHz	45	45.7	–	dBm
	Frequency = 9.5 GHz	45	45.8	–	dBm
	Frequency = 10 GHz	45	45.8	–	dBm
Power Added Efficiency @ P_{IN} = 18 dBm	Frequency = 9 GHz	40	46.4	–	%
	Frequency = 9.5 GHz	40	46.4	–	
	Frequency = 10 GHz	35	43	–	
Small Signal Gain	Frequency = 9 GHz	–	31.5	–	dB
	Frequency = 9.5 GHz	–	32.7	–	
	Frequency = 10 GHz	–	31.4	–	
Input Return Loss	Frequency = 9 GHz	–	14.7	–	dB
	Frequency = 9.5 GHz	–	15	–	
	Frequency = 10 GHz	–	11	–	
Output Return Loss	Frequency = 9 GHz	–	10.6	–	dB
	Frequency = 9.5 GHz	–	9.3	–	
	Frequency = 10 GHz	–	12	–	
Output Power Temperature Coefficient From 25°C to 85°C (Pin = 18dBm)		–	-0.02	–	dBm/°C

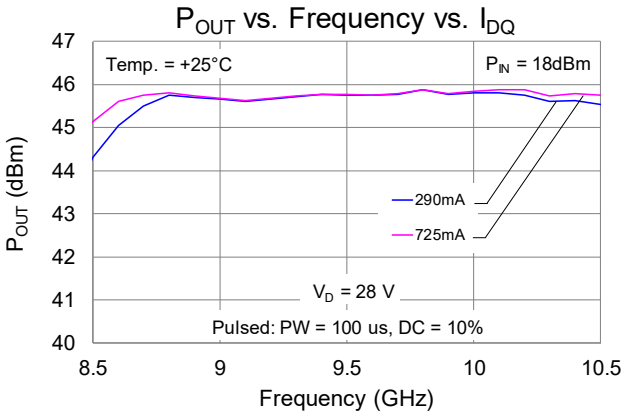
Performance Plots – Large Signal (Pulsed)

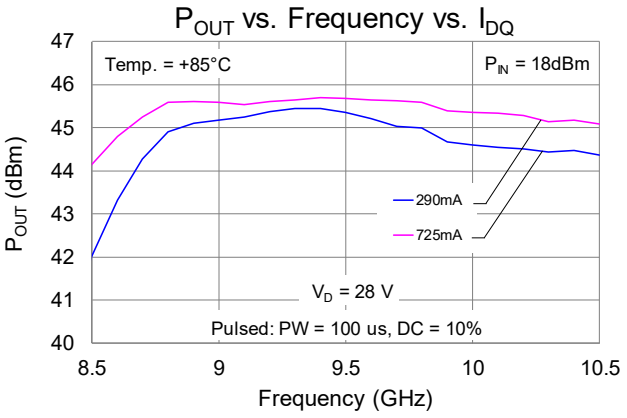




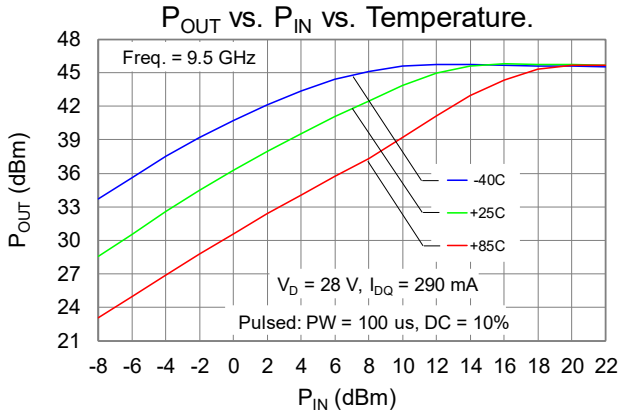


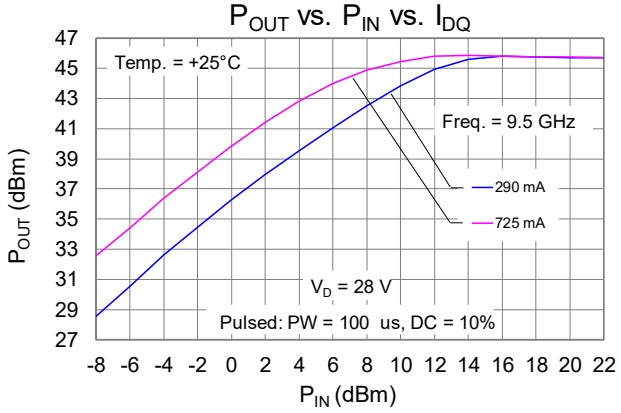


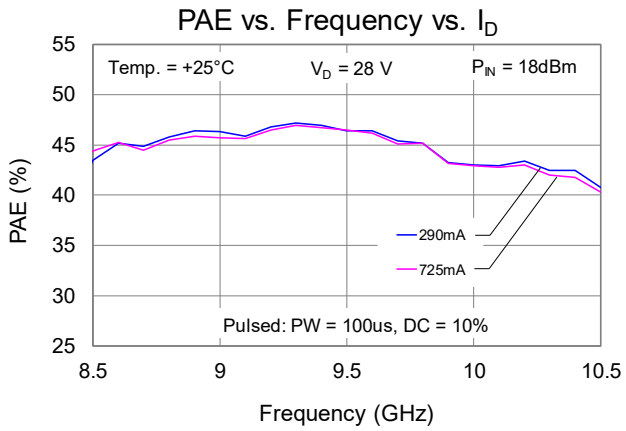


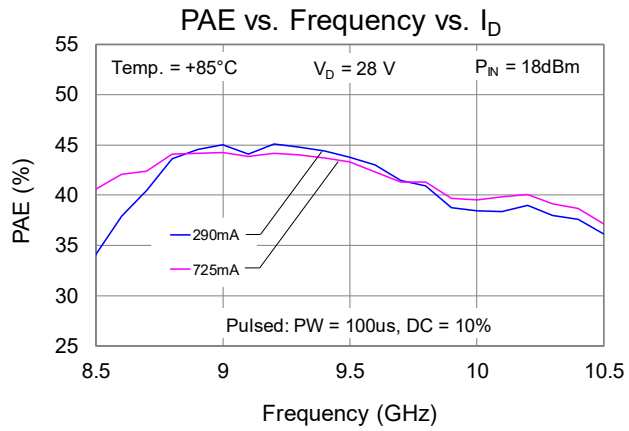


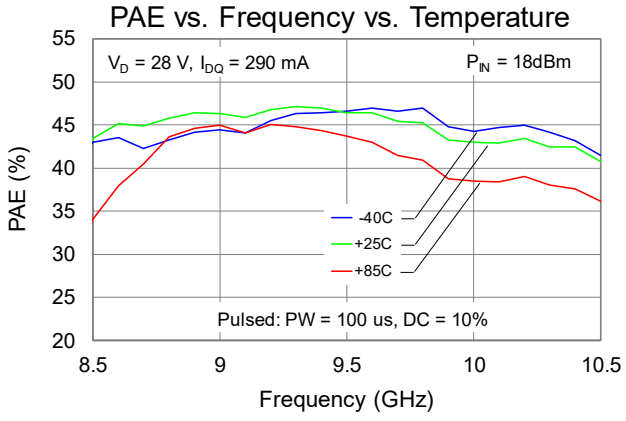
Performance Plots – Large Signal (Pulsed)

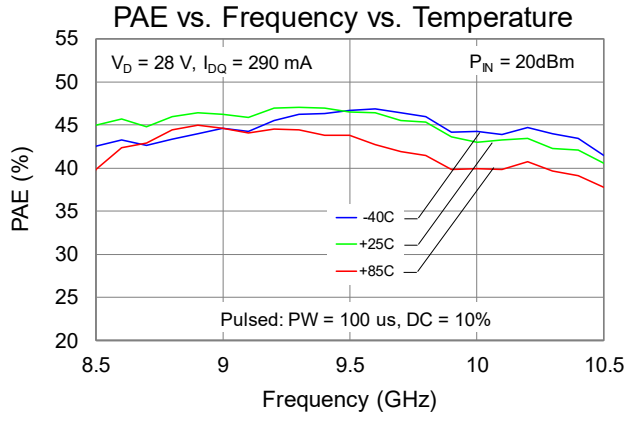






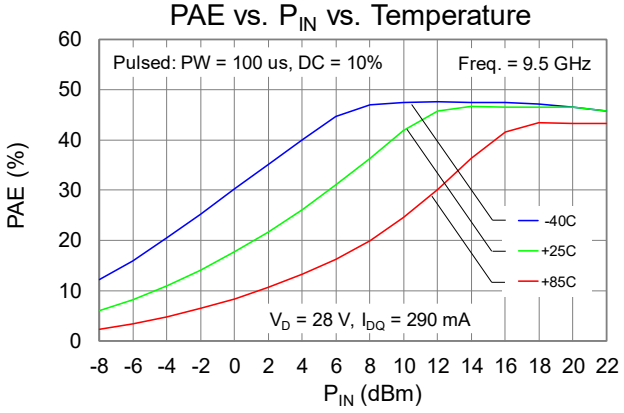




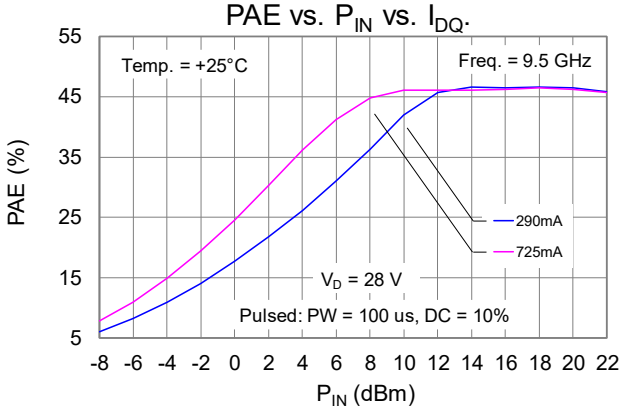


Performance Plots – Large Signal (Pulsed)

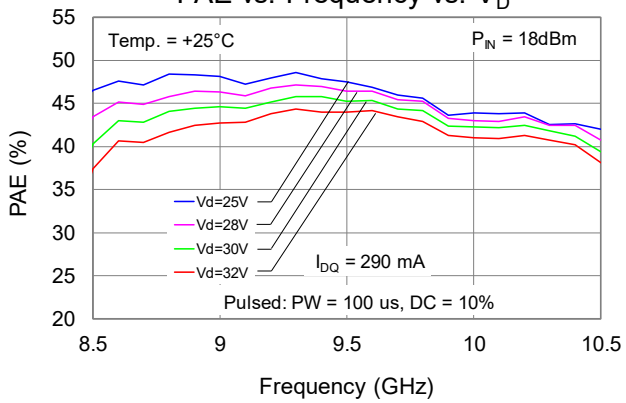
PAE vs. P_{IN} vs. Temperature



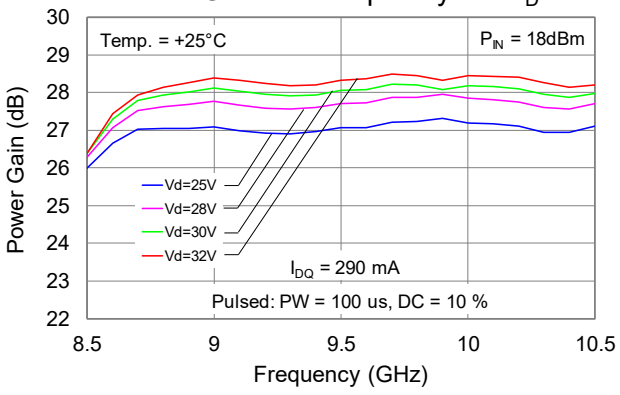
PAE vs. P_{IN} vs. I_{DQ}.



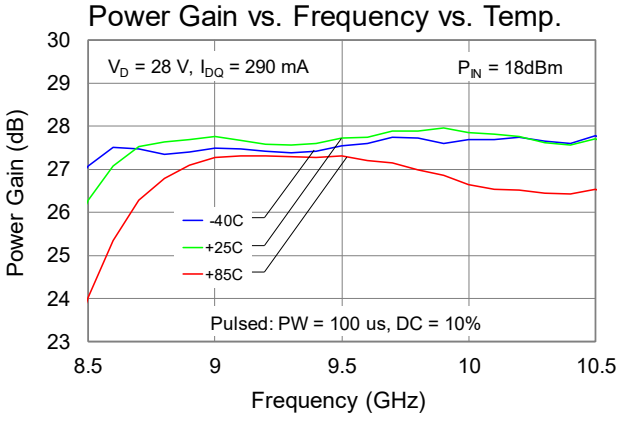
PAE vs. Frequency vs. V_D



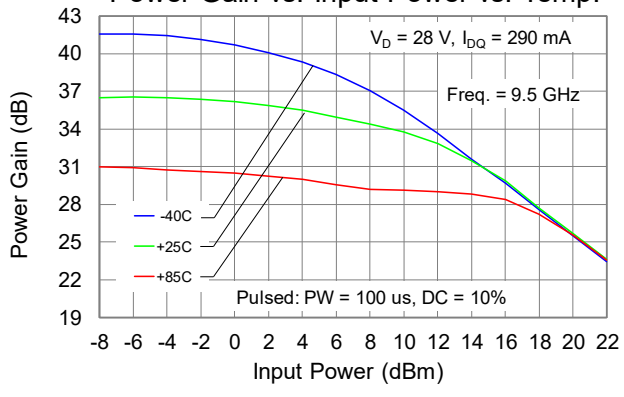
Power Gain vs. Frequency vs. V_D



Power Gain vs. Frequency vs. Temp.

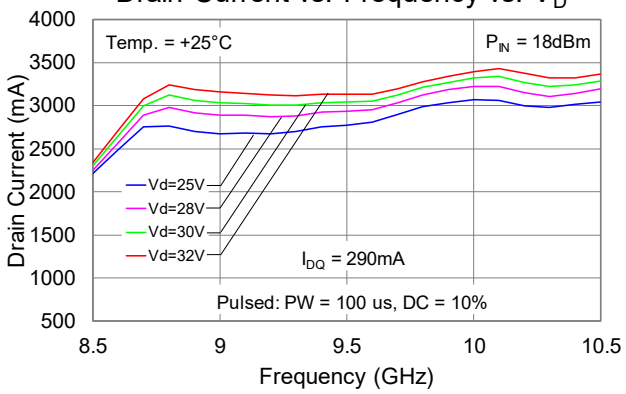


Power Gain vs. Input Power vs. Temp.

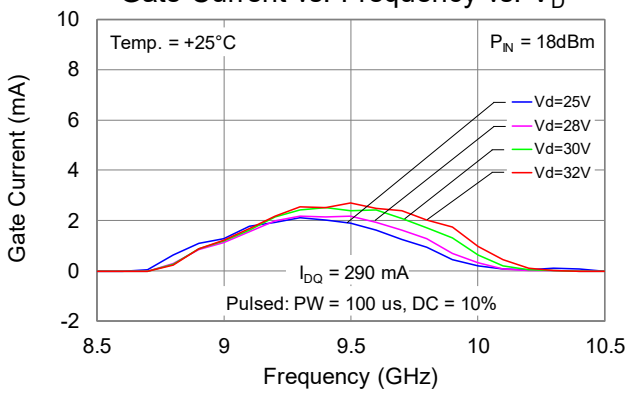


Performance Plots – Large Signal (Pulsed)

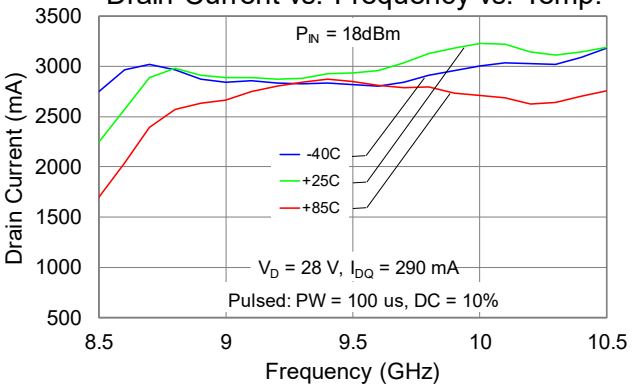
Drain Current vs. Frequency vs. V_D



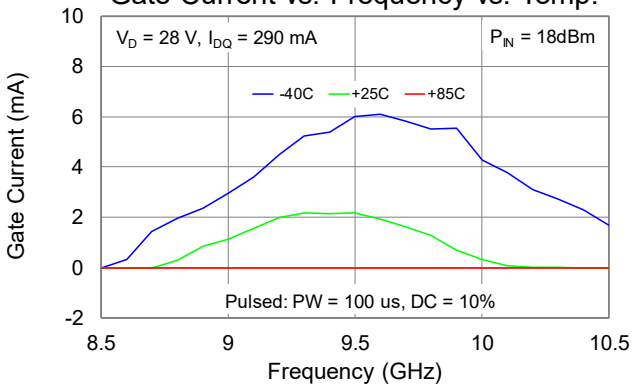
Gate Current vs. Frequency vs. V_D



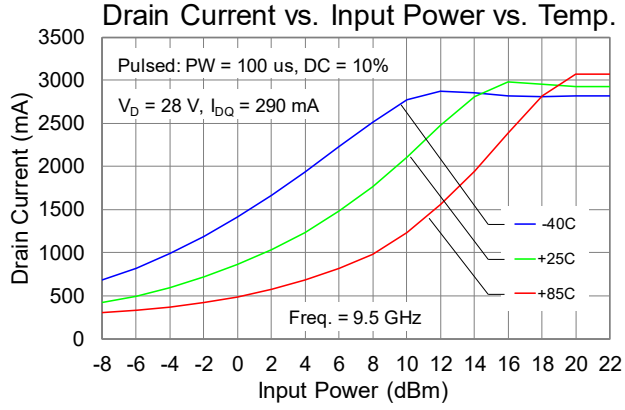
Drain Current vs. Frequency vs. Temp.



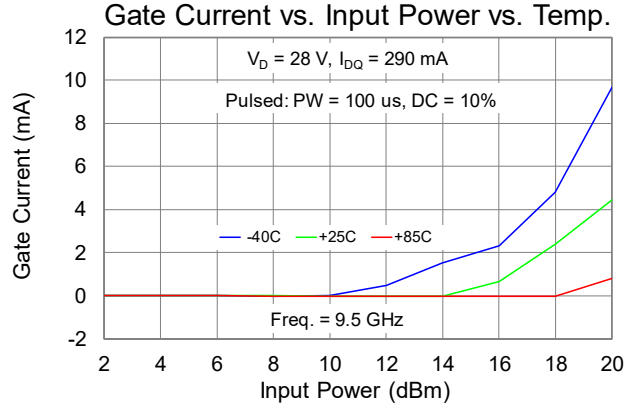
Gate Current vs. Frequency vs. Temp.



Drain Current vs. Input Power vs. Temp.

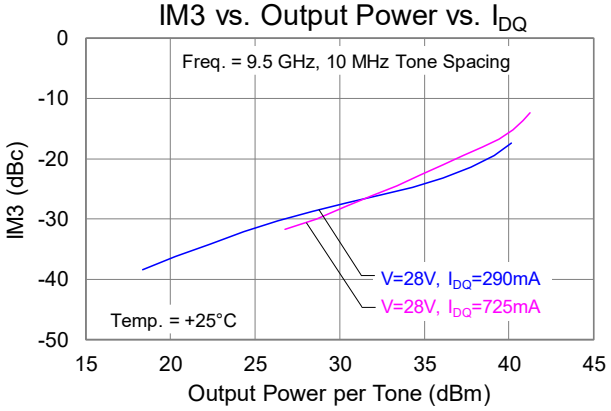


Gate Current vs. Input Power vs. Temp.

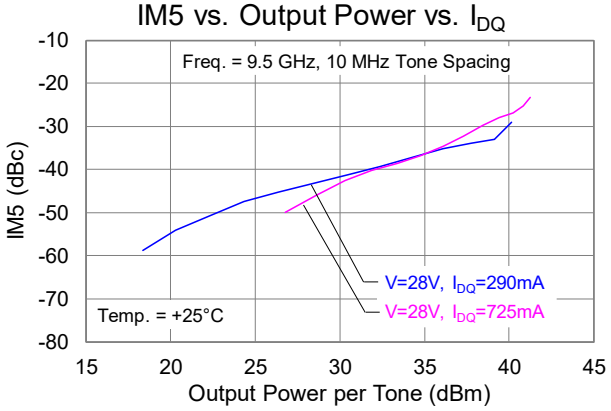


Performance Plots – Linearity (CW)

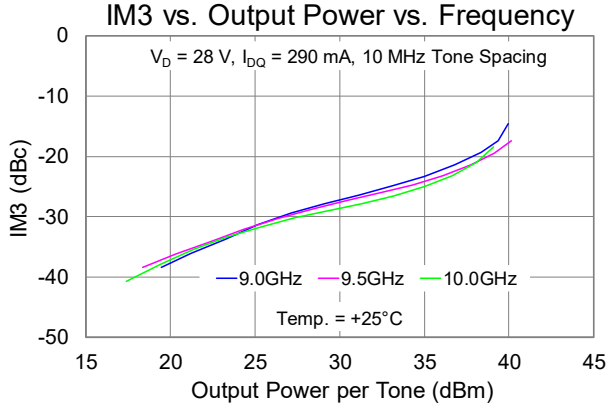
IM3 vs. Output Power vs. I_{DQ}



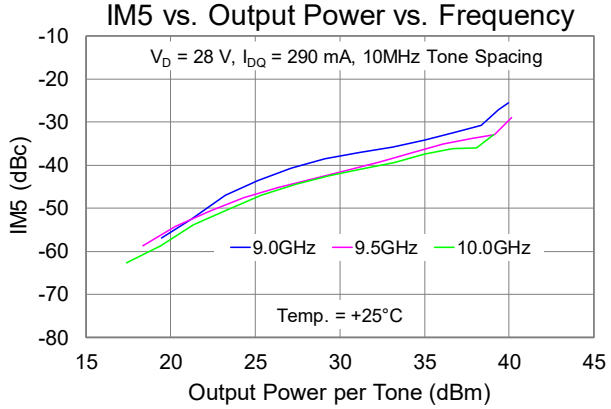
IM5 vs. Output Power vs. I_{DQ}



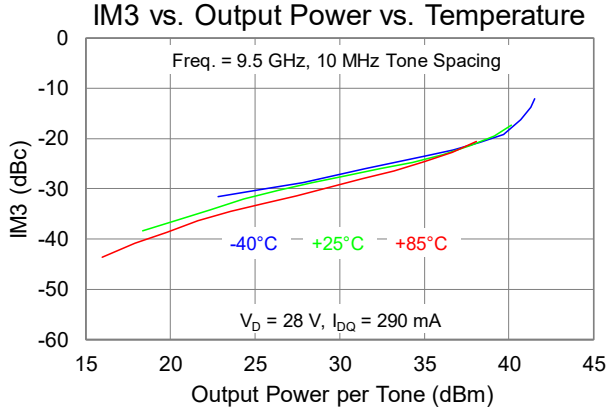
IM3 vs. Output Power vs. Frequency



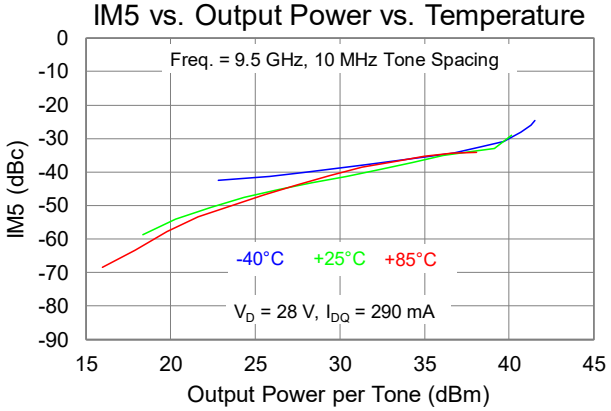
IM5 vs. Output Power vs. Frequency



IM3 vs. Output Power vs. Temperature

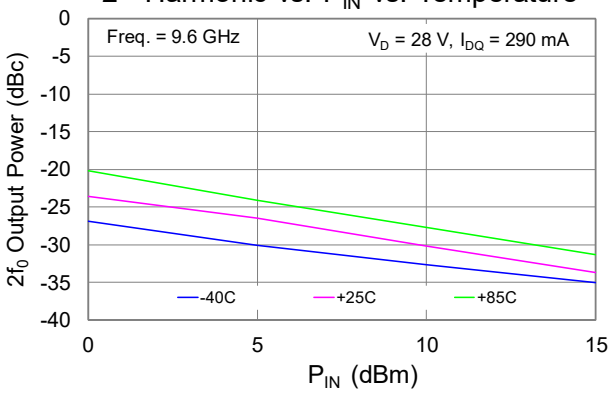


IM5 vs. Output Power vs. Temperature

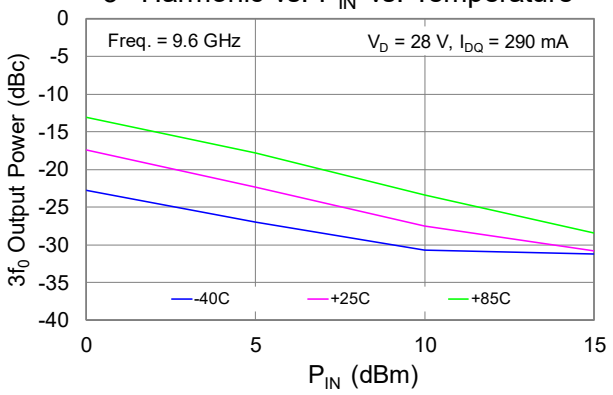


Performance Plots – Linearity (CW)

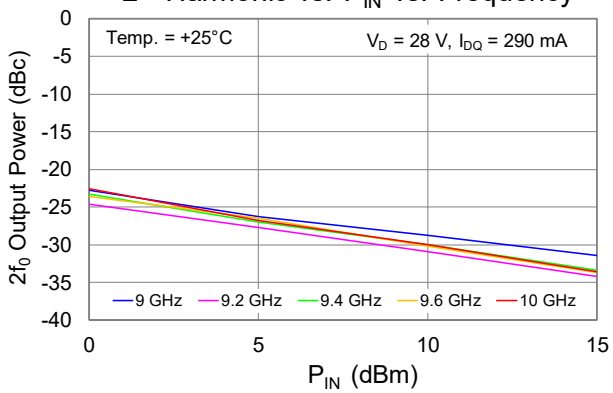
2nd Harmonic vs. P_{IN} vs. Temperature



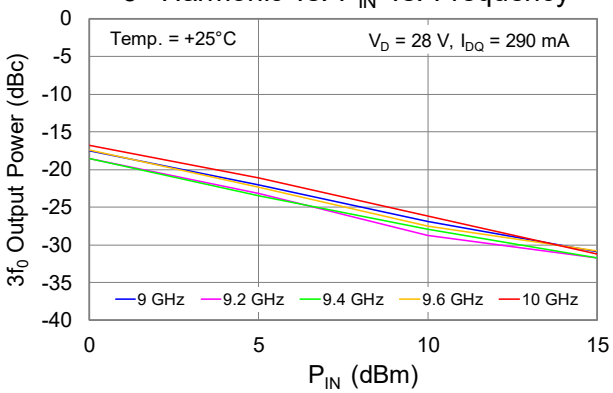
3rd Harmonic vs. P_{IN} vs. Temperature



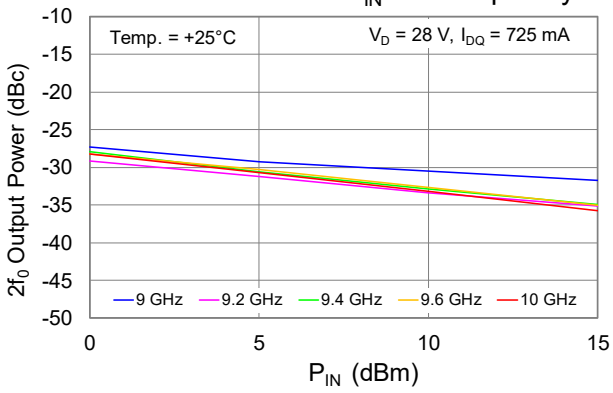
2nd Harmonic vs. P_{IN} vs. Frequency



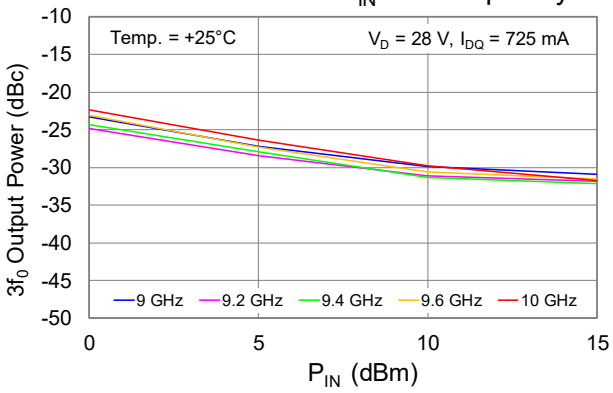
3rd Harmonic vs. P_{IN} vs. Frequency



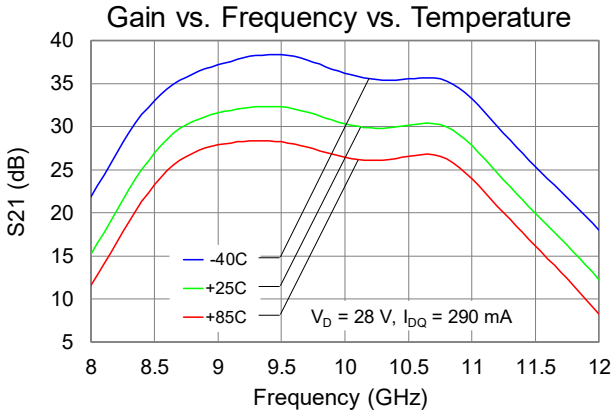
2nd Harmonic vs. P_{IN} vs. Frequency

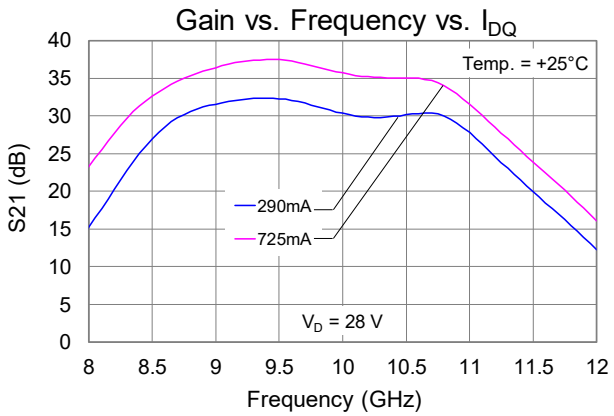


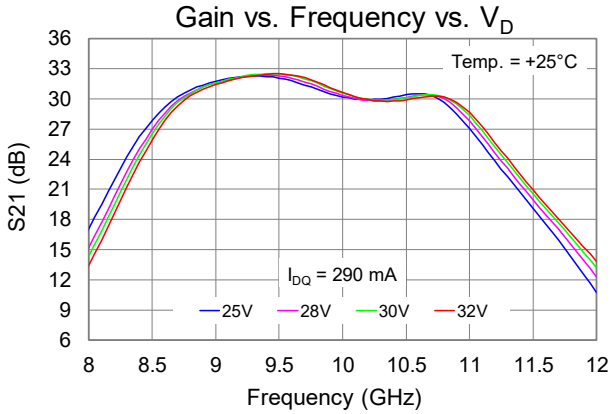
3rd Harmonic vs. P_{IN} vs. Frequency

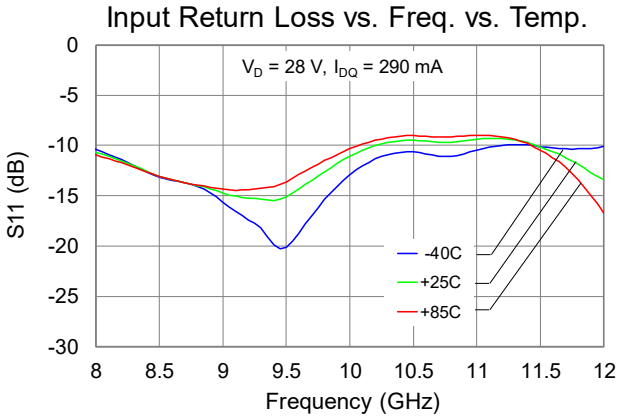


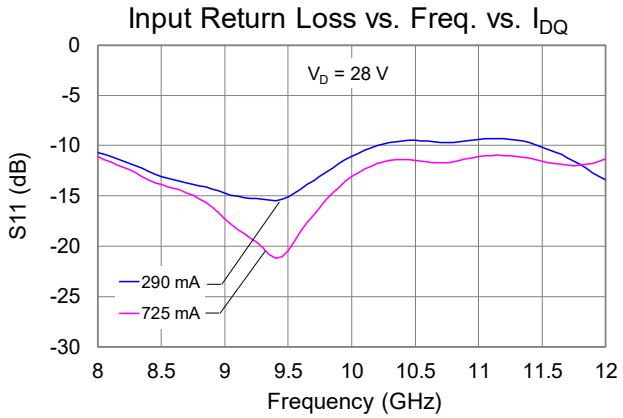
Performance Plots – Small Signal (CW)



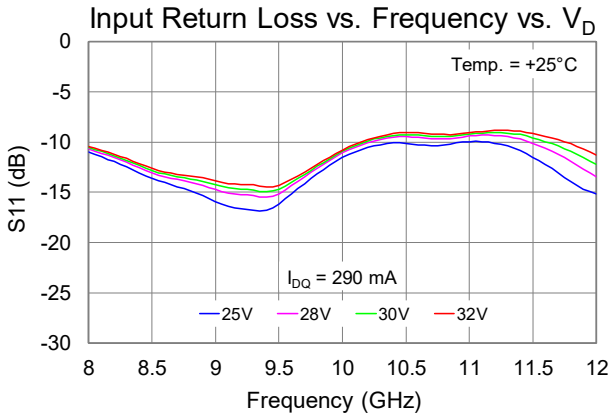


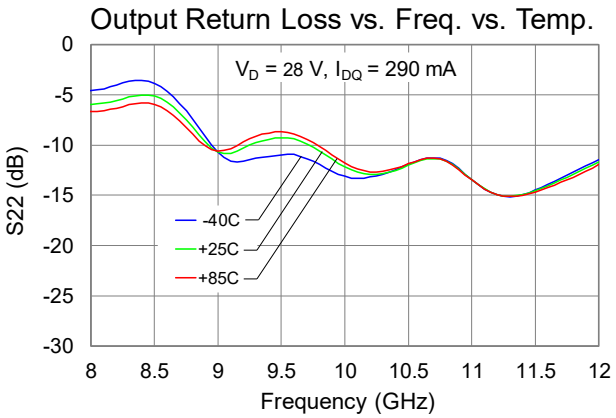


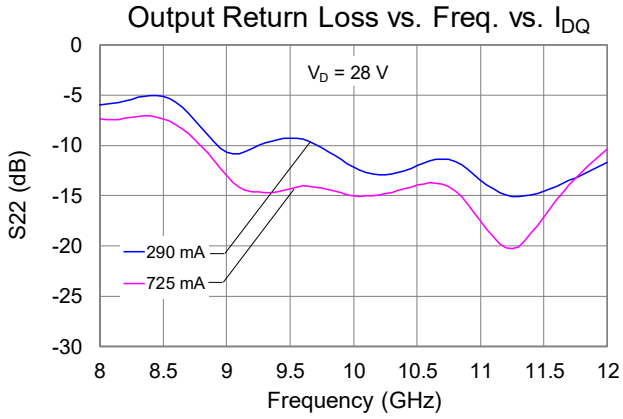


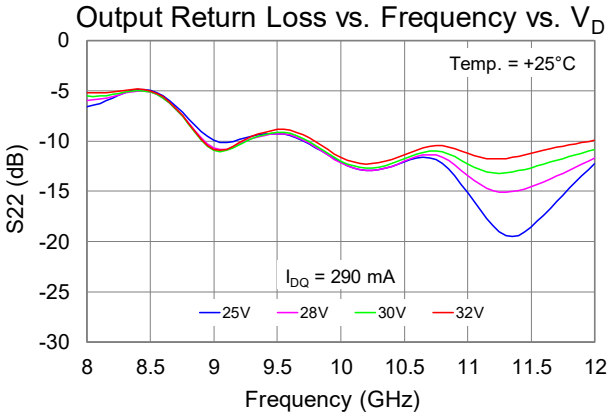


Performance Plots – Small Signal (CW)







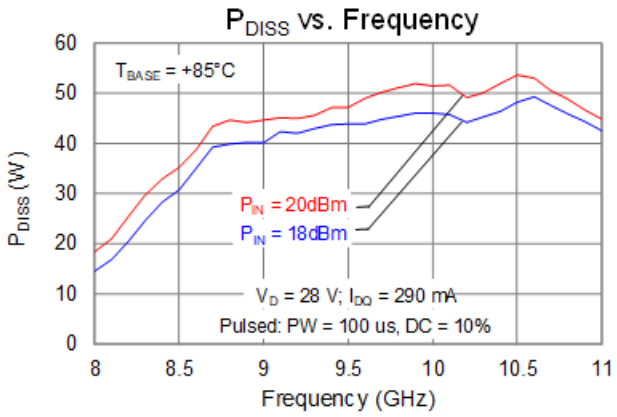


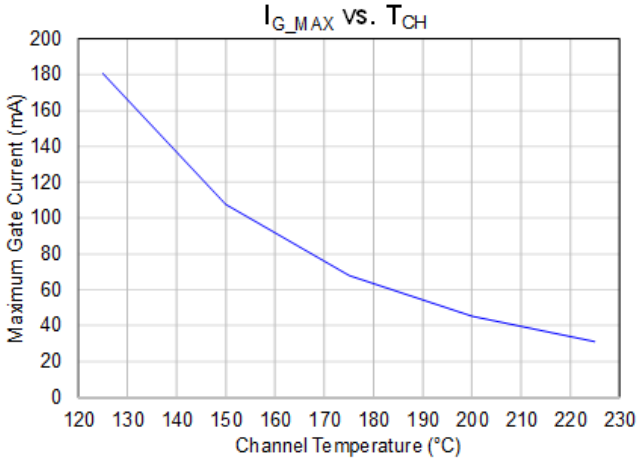
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D = 28 V, I_{DQ} = 290 mA, Smal signal or quiescnet. P_{DISS} = 8.12 W	0.51	ºC/W
Channel Temperature (T_{CH}) (Small Signal) 2		89.1	°C
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D = 28 V, I_{DQ} = 290 mA, Pulsed V_D, PW = 100 us, DC = 10 %, I_{D_Drive} = 3.1 A, P_{IN} = 20 dBm, P_{OUT} = 45.4 dBm, P_{DISS} = 52 W	0.73	ºC/W
Channel Temperature (T_{CH}) (With RF drive) 2		123.2	°C
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D = 28 V, I_{DQ} = 290 mA, CW, I_{D_Drive} = 3.1 A, P_{IN} = 20 dBm, P_{OUT} = 45.4 dBm, P_{DISS} = 52 W	1.19	ºC/W
Channel Temperature (T_{CH}) (With RF drive) 2		146.9	°C

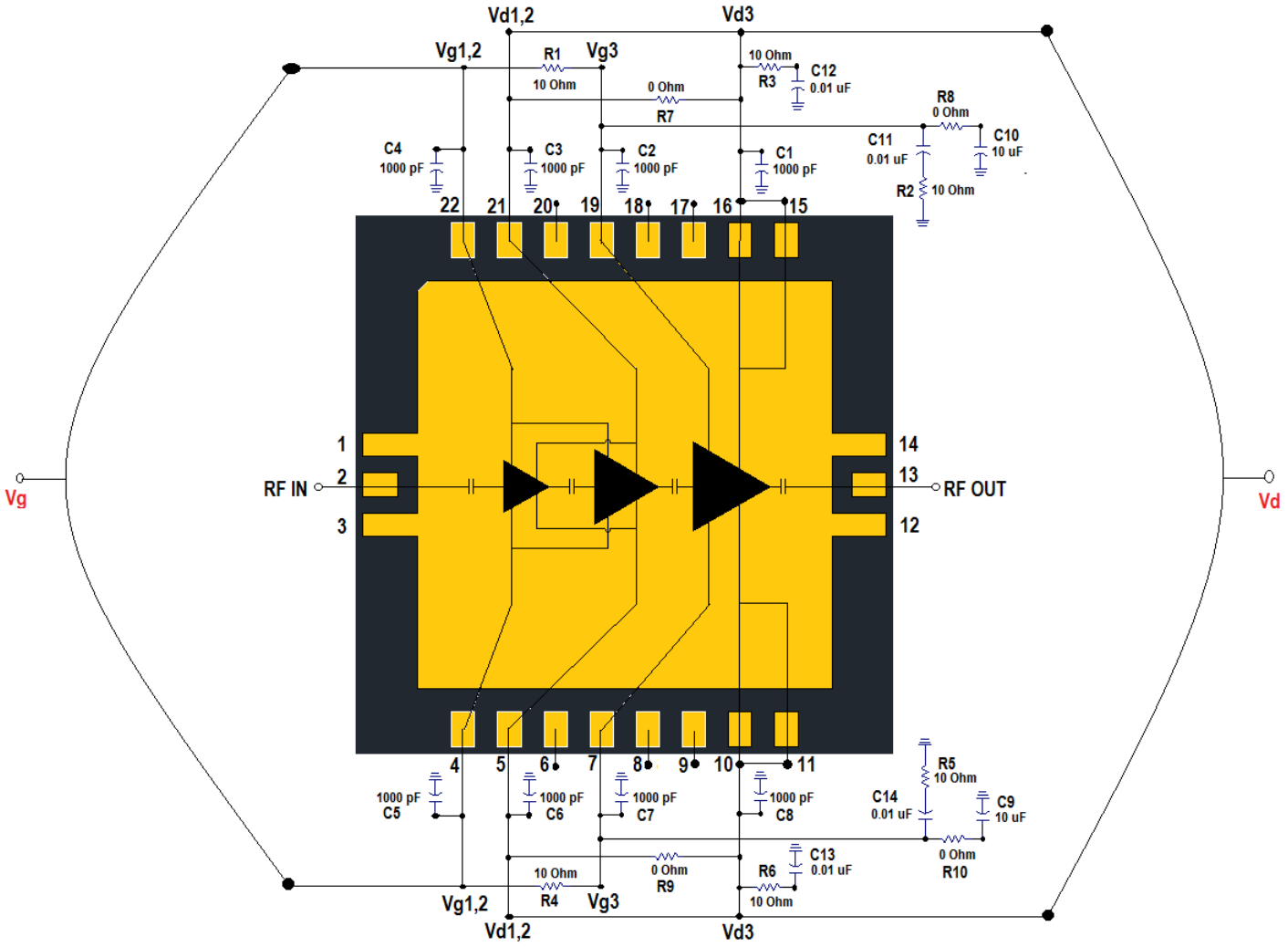
Notes:
1. Thermal Resistance referenced to the back of the package.
2. IR scan equivalent. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Power Dissipation and Maximum Gate Current





Applications Circuit



Notes:

1. V_G: must be biased from both sides - $V_{G1,2}$ & V_{G3} can be tied together.
2. V_D: must be biased from both sides - $V_{D1,2}$ & V_{D3} can be tied together.

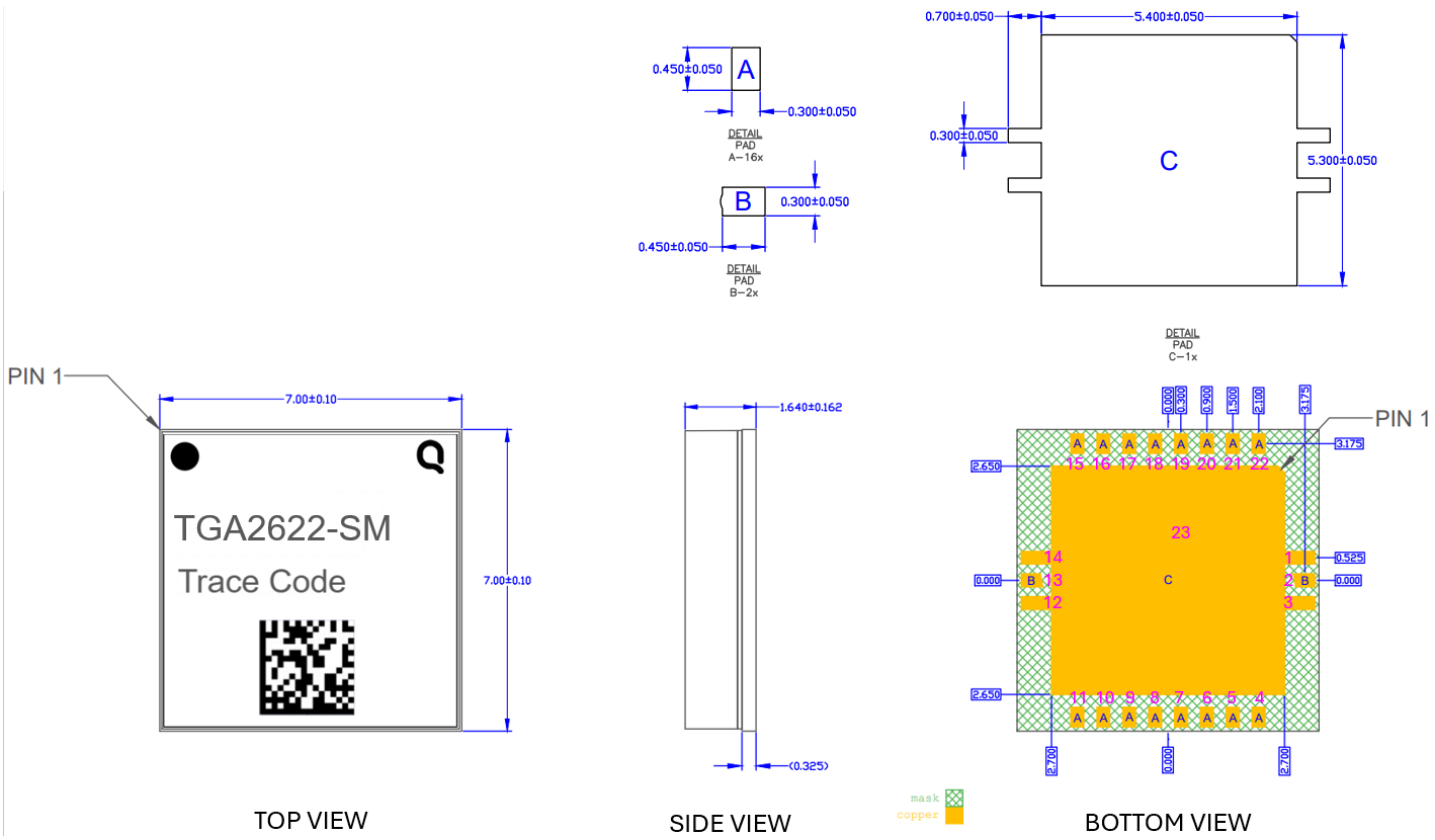
Bias Up Procedure

1. Set I_D limit to 3.5 A, I_G limit to 25 mA
2. Set V_G to −5.0 V (for pinch-off)
3. Set V_D +28 V; Ensure I_{DQ} is approx. 0 mA
4. Adjust V_G more positive until I_{DQ} = 290mA (V_G ~ −2.3 V Typical)
5. Apply RF signal

Bias Down Procedure

1. Turn off RF supply
2. Reduce V_G to −5.0V. Ensure I_{DQ} ~ 0mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Mechanical Drawing and Pin Layout

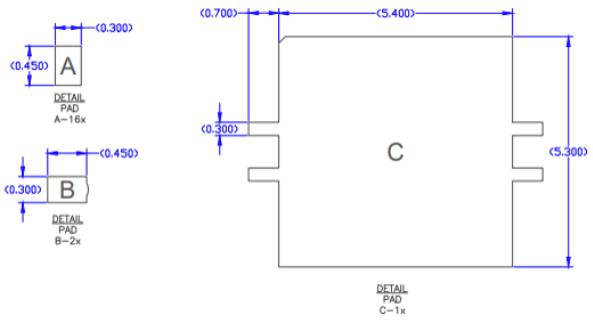


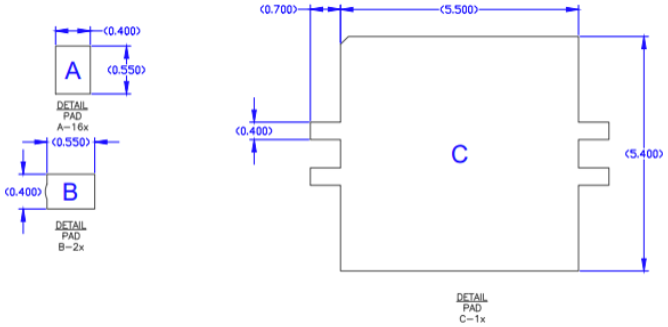
Units: Millimeters (mm)
Tolerances: unless specified: x.xx = ± 0.25; x.xxx = ± 0.100
Materials: Base: Laminate Substrate
Lid: Laminate
All metalized features are gold plated. Part is epoxy sealed
2DID Marking can be used to trace part manufacturing information

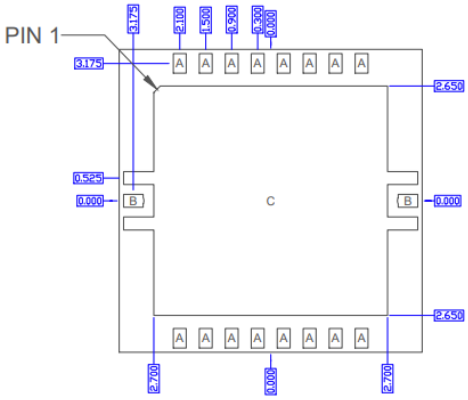
Pin Description

Pin No.	Symbol	Description
1, 3, 12, 14, 23	GND	Must be grounded on the PCB
2	RF_{IN}	Input; matched to 50 Ω; DC blocked
4, 22	$V_{G1,2}$	Gate Voltages 1,2; Bias network is required; must be biased from both sides; see recommended Application Information on page 12.
5, 21	$V_{D1,2}$	Drain voltages 1,2; Bias network is required; must be biased from both sides; see recommended Application Information on page 12.
6, 8, 9, 17, 18, 20	N/C	No internal connection
7, 19	V_{G3}	Gate Voltage 3; Bias network is required; must be biased from both sides; see recommended Application Information on page 12.
10, 11, 15, 16	V_{D3}	Drain voltage 3; Bias network is required; must be biased from both sides; see recommended Application Information on page 12.
13	RF_{OUT}	Output; matched to 50 Ω; DC blocked

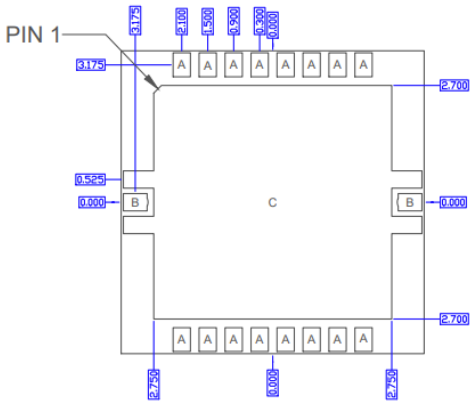
Application PCB Land Patterns and Masks







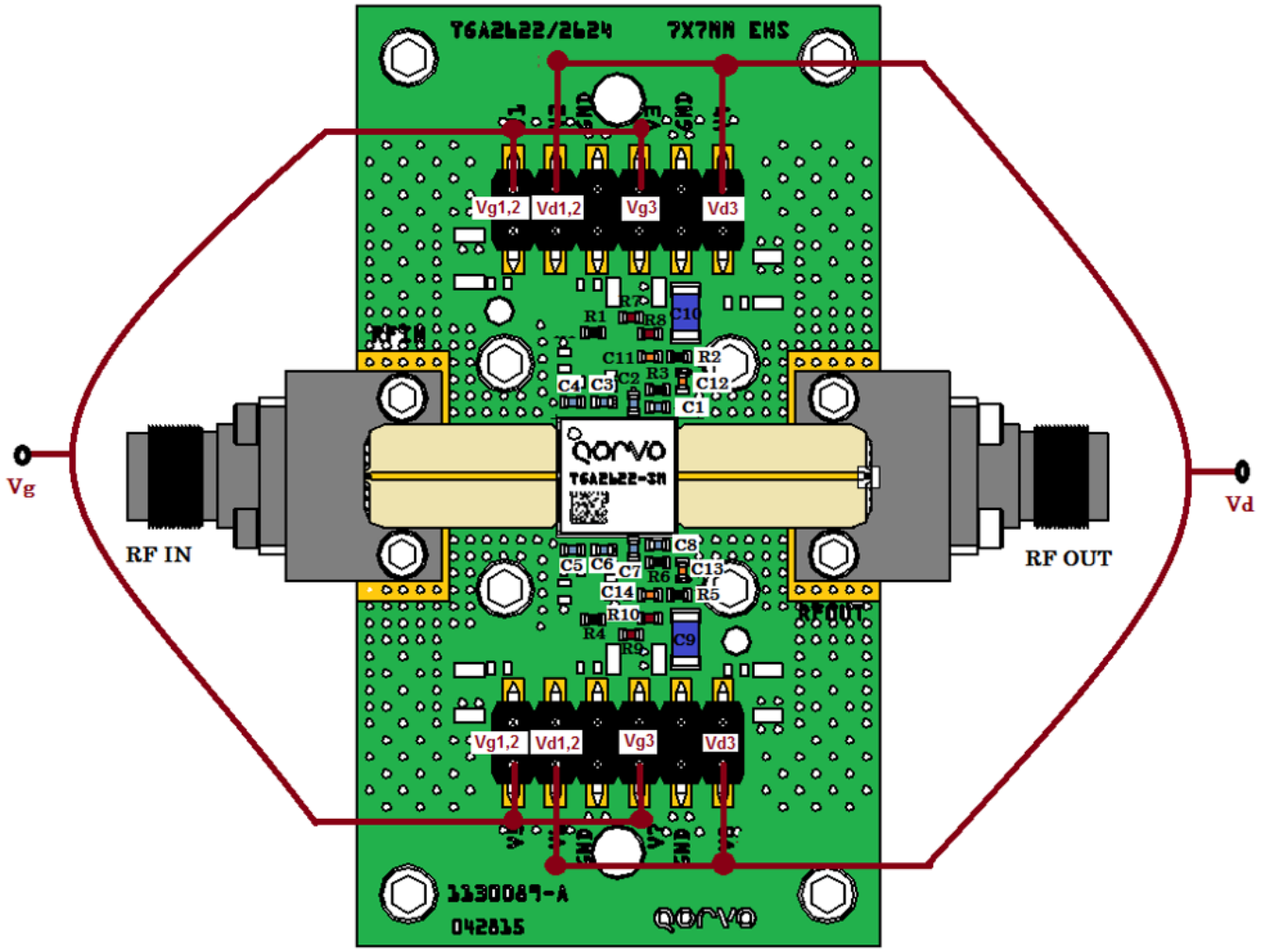
Recommended Land Pattern



Recommended Land Pattern Mask

Units: Millimeters (mm)
Tolerances: unless specified: x.xx = ± 0.25; x.xxx = ± 0.100

Evaluation Board Layout



Notes: Both Top and Bottom V_D and V_G must be biased.

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1 – C8	1000 pF	Cap, 0402, 100 V, 10%, X7R	Various	
C9 – C10	10 µF	Cap, 1206, 50 V, 20%, X5R	Various	
C11 – C14	0.01 µF	Cap, 0402, 50 V, 10%, X7R	Various	
R1 – R6	10 ohms	Res, 0402, 50 V, 5%, SMD	Various	
R7 – R10	0 ohms	Res, 0402, jumpers required for the above EVB	Various	

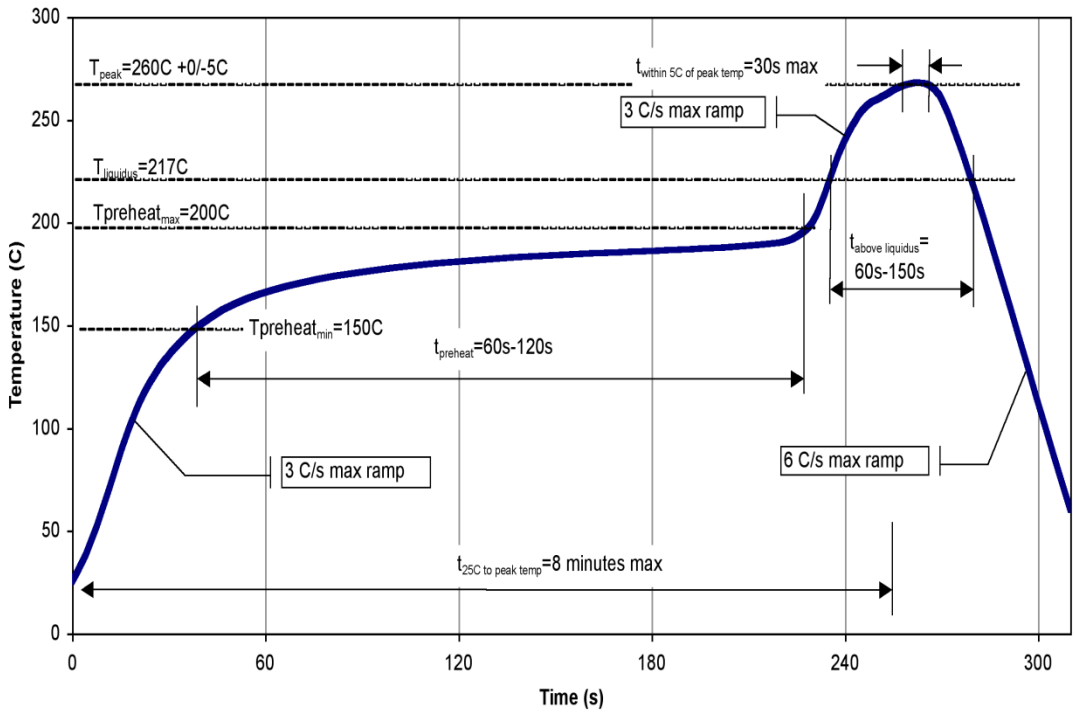
Assembly Notes

Compatible with lead-free soldering processes with 260°C peak reflow temperature.

This package is air-cavity and non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing after soldering is highly recommended.

Contact plating: Ni-Au.

Solder rework not recommended.



Recommended Soldering Temperature Profile

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	ANSI/ESD/JEDEC JS-001
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.
This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Web: www.qorvo.com

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For technical questions and application information: **Email:** info-products@qorvo.com

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