QPB9332

1.71-2.02GHz Rx Digital Variable Gain Amplifier

Product Overview

The QPB9332 is a highly integrated Receiver (Rx) Low Noise Amplifier (LNA) module. It is suitable for common Rx design to replace major active components in front of the mixer. It is targeted for Rx designs restricted in size. A 6-bit digital step attenuator (DSA) integrated in between the first LNA and the second stage high linear LNA provides 19dB gain control capability to handle wide dynamic range of Rx input signal while maintaining optimum noise figure, gain and linearity. An integrated I^2C control interface circuit enables 2-wire communication from host system with 3-bit multi module address capability. The QPB9332 is also featured with a built-in temperature sensor and a nonvolatile memory to store production and temperature data.

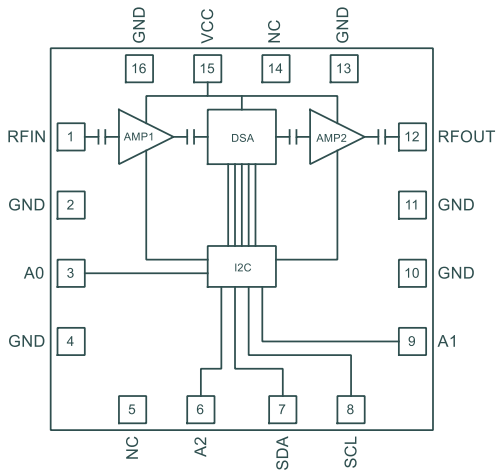
The QPB9332 amplifier stages utilize Qorvo's high performance E-pHEMT process and packaged in a RoHS-compliant, compact 8x8 mm surface-mount leadless package.

16 Pin 8 mm x 8 mm leadless SMT Package

Key Features

- 1710-2020 MHz frequency range
- Integrated LNA, digital step attenuator, linear drive amplifier, I^2C controller, temperature sensor and non-volatile memory
- 5 V DC supply with power saving mode
- 22 to 35 dB guaranteed gain range
- <1.05 dB noise figure at nominal maximum gain
- 36 dBm OIP3
- >14 dB I/O return loss
- Unconditionally stable
- Compact package size, 8x8 mm
- Same Pin assignment as QPB9330, QPB9331 and QPB9336

Functional Block Diagram



Top View

Applications

- Wireless Infrastructure
- Macro or picocell base stations
- FDD-based architectures

Ordering Information

Part No.	Description
QPB9332TR13	2500 pcs on a 13" reel
QPB9332SR	100 pcs on a 7" reel
QPB9332EVB01	Evaluation board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-50 to 150 °C
Operable Case Temperature	-40 to 110 °C
RF Input power, continuous	22 dBm
Total Power Dissipation	1.2 W
Supply Voltage	6 V

Notes:
Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{CC}	+4.75	+5	+5.25	V
T_{SENSOR} 1mm next to Pin 10 and 11	−10		+90	°C
Tj for >10^6 hours MTTF			+190	°C

Notes:
Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: T = +25°C, V_{CC} = +5V

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		1710		2020	MHz
Gain, Nominal Maximum	Programed		35		dB
Gain Adjustable Range		22		35	dB
DSA Setting Step Size			0.5		dB
DSA Setting Range			19		dB
Gain Variation over Frequency	Any single gain setting at a temperature point		2		dB
Gain Variation in Band	Single 3GPP uplink band		1		dB
Gain Setting Accuracy	DSA setting 0 to 8 dB		±0.4		dB
	DSA setting 8.5 to 19 dB		± (0.1+3%*DSA setting)		dB
LSB Gain Setting Error	Between adjacent DSA steps		±0.2		dB
Noise Figure	35 dB nominal maximum gain		1.05		dB
Input IP3	35 dB nominal maximum gain		1		dBm
Input P1dB	35 dB nominal maximum gain		-14		dBm
Input Return Loss			15		dB
Output Return Loss			14		dB
Reverse Isolation	Up to 35 dB nominal maximum gain		55		dB
Operating Current			172		mA
Gain Power ON Setting Time	DC Power On, Settle within 0.5dB		1.5		sec.
Gain Change Setting Time	Settle within 0.5dB		10		ms
Gain Wake Up Setting Time	Wake up from power saving mode and settle within 0.5dB		10		ms
Spurious Emission, RF Output	9 KHz – 1 MHz, BW 4.5 MHz		-30		dBm
	1-12750 MHz excluding 3 GPP Bands, BW 4.5MHz		-67.4		dBm
	3 GPP uplink band		-88.8		dBm
Spurious Emission, I^2C lines	9 KHz – 10 MHz		-35		dBm
	10 – 3000 MHz		-47		dBm
Temperature Sensor Accuracy			±10		°C
Thermal Resistance				29.9	°C/W

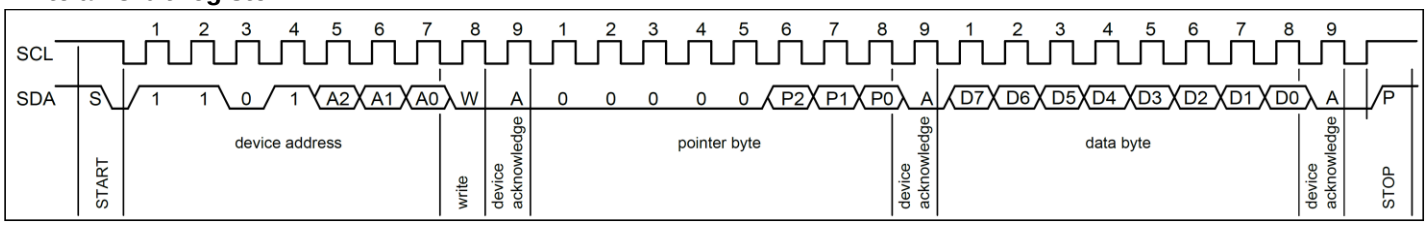
I²C Control Interface

Interface Specifications

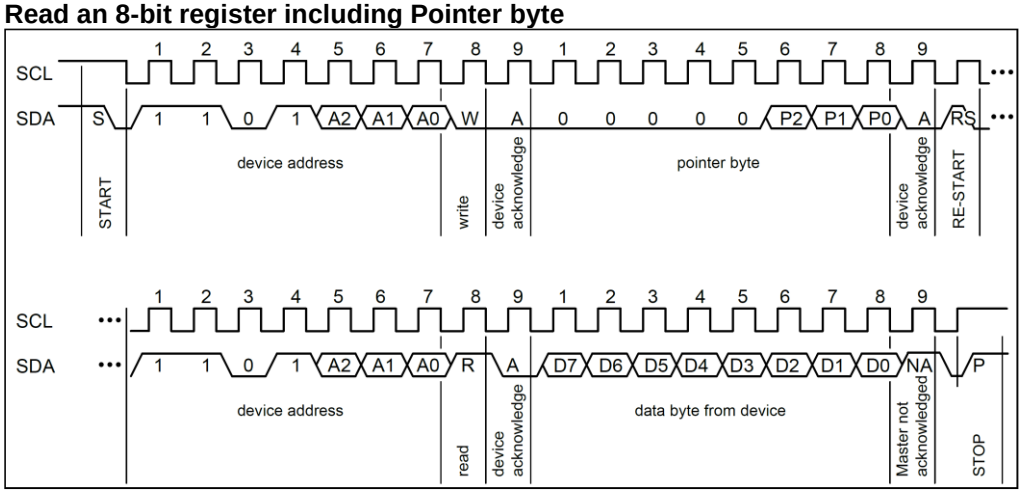
Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage for I²C, V_{DD}		1.71	1.8	1.89	V
LOW level voltage, V_{IL} V_{OL}	SCL Input; SDA Input and Output	-0.54		0.3*V_{DD}	V
HIGH level voltage, V_{IH} V_{OH}	SCL Input; SDA Input and Output	0.7* V_{DD}		V_{DD} +0.5	V
LOW level sink current, I_{OL}	SDA V_{OL} 0.4V	3			mA
Hysteresis of Schmitt trigger inputs, V_{hys}		0.05*V_{DD}			V
Pin capacitance, C_i				10	pF
Maximum Clock Frequency, f_{SCL}	SCL Input			100	KHz
Output fall time, tof	From V_{IHmin} to V_{ILmax}			250	ns
Input current of each I/O pin, Ii	0.1V_{DD}<$V_{I/O\ pin}$<0.9V_{DDmax}	-10		10	µA

Diagram of I²C Reading and Writing Transactions

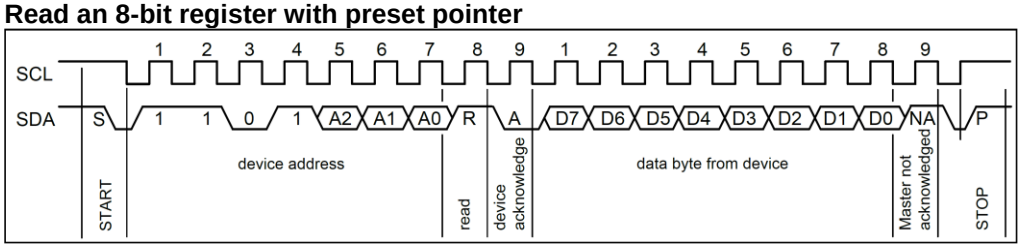
Write an 8-bit register



Read an 8-bit register including Pointer byte



Read an 8-bit register with preset pointer



Protocols for writing and reading

The QPB9332 register read and write follow the Standard-mode by the I²C-bus. The read and write transactions are defined as the following:

Signal	Description
SCL	Serial clock pulse provided by the master. Data is transferred in a sequence of 9 SCL clock pulses for every 8-bit data byte followed by 1-bit status of the acknowledgement
SDA	serial data can be changed only during the LOW duration of the SCL, except the START and STOP, the SDA signal must stable while the SCL signal is HIGH
S	START signal, initiated by the master to start a communication, the SDA goes from HIGH to LOW while the SCL is HIGH
P	STOP signal, generated by the master to stop a communication, the SDA goes from LOW to HIGH while the SCL is HIGH
W	write bit, when the write/read bit LOW in a write transaction
R	read bit, when the write/read bit HIGH in a read transaction
A	device acknowledge bit, returned by the QPB9332. It is LOW if the device works properly and HIGH if not. The master must release the SDA line during this period to give the QPB9332 the control on the SDA line
NA	Not Acknowledge bit. During this clock period, both the QPB9332 and the master release the SDA line at the end of a data transfer, the master is then enabled to generate the STOP signal

QPB9332 7-bit device address and a write/read bit

MSB						LSB		
A6	A5	A4	A3	A2	A1	A0	W/R bit	Description
1	1	0	1	X	X	X	0	Write to the device with the address
1	1	0	1	X	X	X	1	Read from the device with the address

Note: A6, A5, A4 and A3 Hard wired internally

Device Address Table

A2	A1	A0	Device Number
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

Note: A2, A1 and A0 hard wired externally with Pin 6, Pin 9, and Pin 3 respectively; Open="1"

QPB9332 Pointer Byte

B7	B6	B5	B4	B3	B2	B1	B0	Hex	Assigned Register
0	0	0	0	0	0	0	0	00h	Qorvo I²C-bus ID
0	0	0	0	0	0	0	1	01h	Attenuation
0	0	0	0	0	0	1	0	02h	Control
0	0	0	0	0	0	1	1	03h	MaxGainF1
0	0	0	0	0	1	0	0	04h	MaxGainF2
0	0	0	0	0	1	0	1	05h	Temp
0	0	0	0	0	1	1	0	06h	N/A
0	0	0	0	0	1	1	1	07h	N/A

Register List

Register Name	Pointer Hex Value	R/W	Default Value	Description
Qorvo I2C-bus ID	00h	Read only	00011100	Qorvo device I2C-bus ID
Attenuation	01h	R/W	00000000	8-bit DSA control word
Control	02h	R/W	00000000	8-bit QPB9332 functionalities
MaxGainF1	03h	Read only	Component specific	1950MHz, Production measured maximum Gain
MaxGainF2	04h	Read only	Component specific	1747.5MHz, Production measured maximum Gain
Temp	05h	Read only	N/A	Temperature data measured with on module internal sensor

Note: Registers will be reset to default after power-up (POR) and all register values will remain during power saving mode

Qorvo I²C-bus ID Register (00h)

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	1	1	1	0	0

Attenuation Register (01h)

B7	B6	B5	B4	B3	B2	B1	B0	Attenuation (dB)
0	0	0	0	0	0	0	0	0.0
0	0	0	0	0	0	0	1	0.5
0	0	0	0	0	0	1	0	1.0
0	0	0	0	0	0	1	1	1.5
0	0	0	0	0	1	0	0	2.0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
0	0	1	1	1	1	1	0	31.0
0	0	1	1	1	1	1	1	31.5

Control Register (02h)

B7	B6	B5	B4	B3	B2	B1	B0	Description
0	0	0	0	0	0	0	0	Normal operation mode; No temperature measurement;
0	0	0	0	0	0	0	1	RF amplifiers in Power saving mode; No temperature measurement;
0	0	0	0	0	0	1	0	Normal operation mode; Execute temperature measurement temp-to-digital conversion, result will be in Temp register after 100ms (max.) B1 bit will automatically back to “0” when conversion is ready
0	0	0	0	0	0	1	1	RF amplifiers in Power saving mode; Execute temperature measurement temp-to- digital conversion, result will be in Temp register after 100ms (max.) B1 bit will automatically back to “0” when conversion is ready

Note: I^2C interface will fully operation at any control state

Maximum Gain Registers (03h and 04h)

B7	B6	B5	B4	B3	B2	B1	B0
0	0	X	X	X	X	X	X

F1 1950MHz Max. Gain Table for Register (03h)

Register Value	Gain (dB)
00000000	35.0
00000001	35.1
00000010	35.2
00000011	35.3
00000100	35.4
00000101	35.5
00000110	35.6
00000111	35.7
.	.
.	.
.	.
00111110	41.2
00111111	41.3

F2 1747.5MHz Max. Gain Table for Register (04h)

Register Value	Gain (dB)
00000000	35.0
00000001	35.1
00000010	35.2
00000011	35.3
00000100	35.4
00000101	35.5
00000110	35.6
00000111	35.7
.	.
.	.
.	.
00111110	41.2
00111111	41.3

Temperature Register (05h)

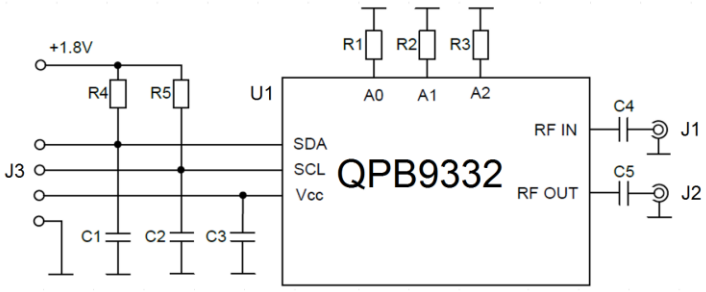
B7	B6	B5	B4	B3	B2	B1	B0	Temperature (°C)
0	0	0	0	0	0	0	0	-60.000
0	0	0	0	0	0	0	1	-59.216
0	0	0	0	0	0	1	0	-58.431
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
0	1	0	0	1	1	0	0	-0.392
0	1	0	0	1	1	0	1	+0.392
0	1	0	10	1	1	1	0	+1.170
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	0	1	+138.431
1	1	1	1	1	1	1	0	+139.216
1	1	1	1	1	1	1	1	+140.000

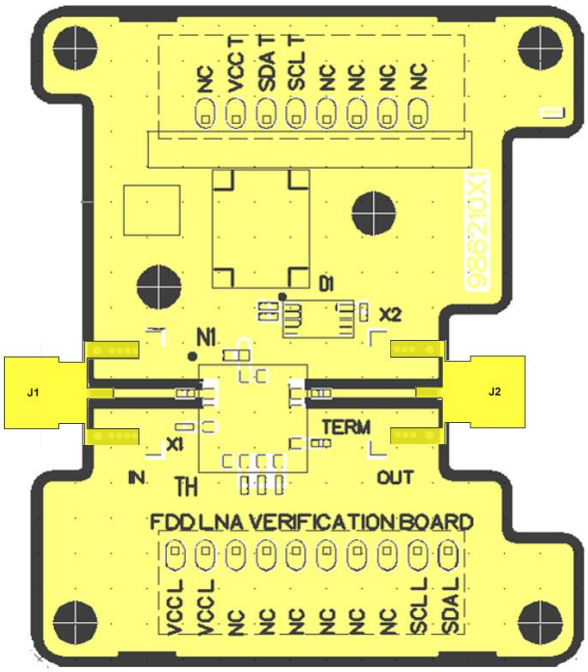
Performance Summary

Test conditions unless otherwise noted: T = +25 °C, V_{CC} = +5 V, Gain at 35 dB the nominal programmed maximum

Frequency	1710	1865	2020	MHz
Gain	35.8	35.0	34.4	dB
Gain Flatness, all states		1.49		dB
Gain Flatness, all states on single 3GPP uplink		0.44		dB
Input Return Loss	22.7	21.8	20.9	dB
Output Return Loss	26.1	21.1	19.2	dB
Input IP3, Gain=35dB (Pout/tone=+3dBm, Δf=1MHz)	1.51	1.03	1.29	dBm
Input IP3, Gain=29dB (Pout/tone=+3dBm, Δf=1MHz)	6.6	6.8	6.9	dBm
Input IP3, Gain=22dB (Pout/tone=+3dBm, Δf=1MHz)	11.0	11.9	12.3	dBm
Noise Figure, Gain=35dB	0.81	0.79	0.78	dB
Noise Figure, Gain=29dB	1.11	1.12	1.12	dB
Noise Figure, Gain=22dB	2.58	2.51	2.59	dB
Amplifier Current, I_{AMP}		173		mA

Application Circuit Schematic and Layout





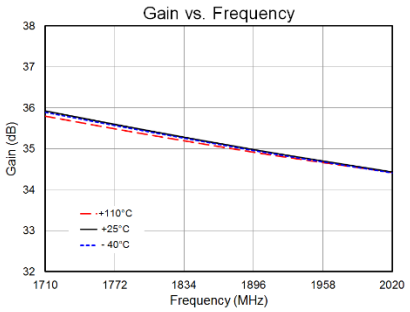
Bill of Material

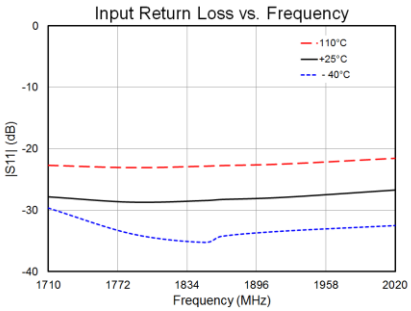
Ref Des	Value	Description	Manuf.	Part Number
PCB	n/a	Printed Circuit Board	Qorvo	
U1	n/a	Rx LNA DVGA Module	Qorvo	QPB9332
R1, R2, R3	0 Ω	Resistor, 0 Ω, 0402	Various	
C1, C2	10 pF	Capacitor, 0402, 10 pF, 50V, COG	Various	
C3	1.0 µF	Capacitor, 0603, 1.0 µF, 10%, 16V, X7R	Various	
C4, C5	100 pF	Capacitor, 0402, 100 pF, 5%, 50V, COG	Various	
J1, J2	SMA	SMA Edge Mount RF connector	Various	
J3	20 POS	Connector, Header 20POS .100” SMD	Samtec	TSM-100-01-L-DV-P

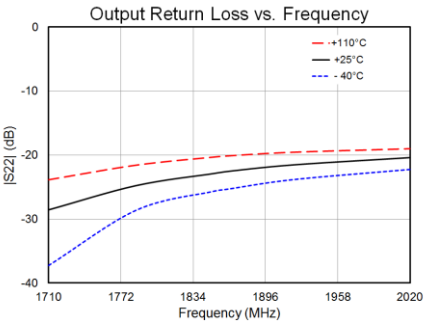
Note: R4 and R5 are I^2C bus pull up resistors should be located on the I^2C controller or host system side

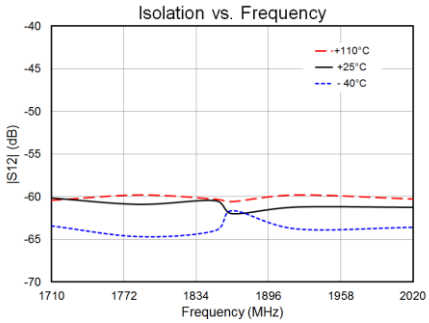
Performance Plots

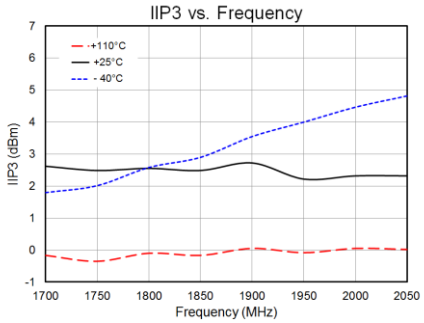
Test conditions unless otherwise noted: V_{CC} = +5 V, Gain at 35 dB the nominal programmed maximum

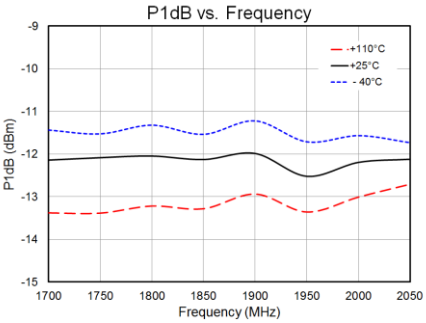


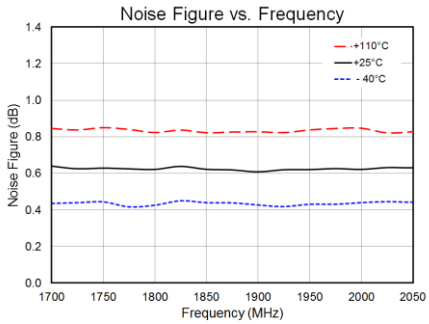


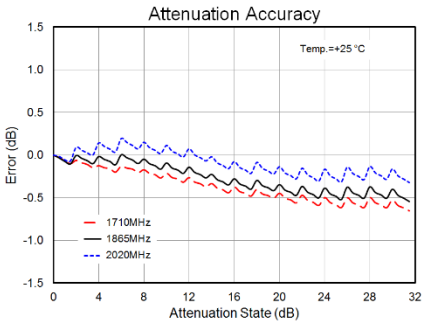


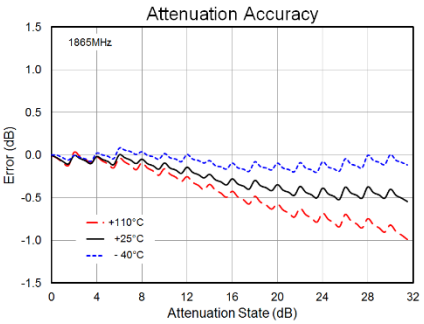


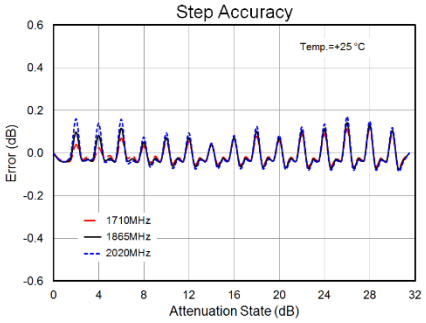


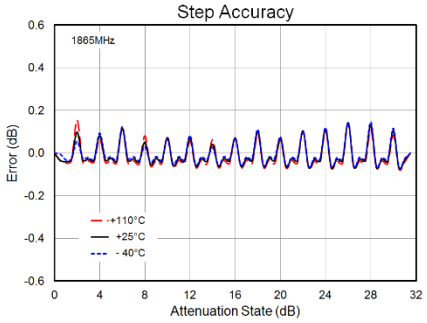




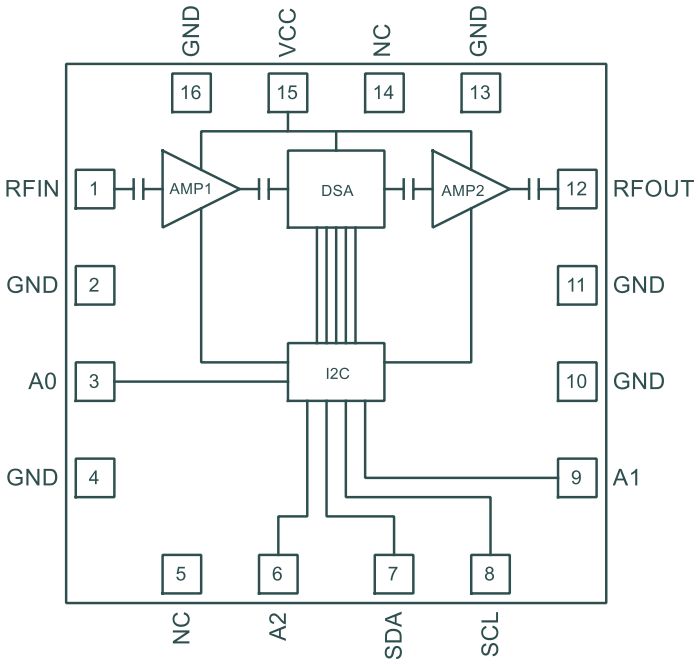








Pin Configuration and Description

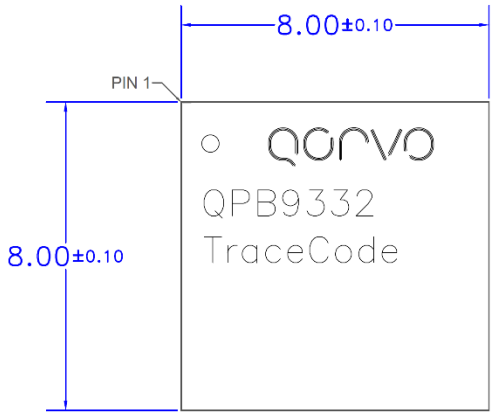


Top View

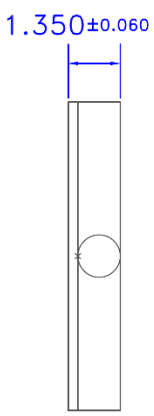
Pin No.	Label	Description
1	RFIN	RF Input, internally matched to 50 Ω
2,4,10,11,13,16	GND	Ground connection, internally connected
3	A0	I^2C slave address input Pin, bit #0
5, 14	NC	No internal connection, can be left floating or connect to ground
6	A2	I^2C slave address input Pin, bit #2
7	SDA	I^2C Data bidirectional, Open-Drain or Collector
8	SCL	I^2C Clock input, Open-Drain or Collector
9	A1	I^2C slave address input Pin, bit #1
12	RF OUT	RF Output, internally matched to 50 Ω
15	VCC	DC Voltage supply input
Package Base Backside Pad	GND	Ground connection. The back side of the package should be connected to the ground plane though as short of a connection as possible. PCB via holes under the device are required.

Package Marking and Dimensions

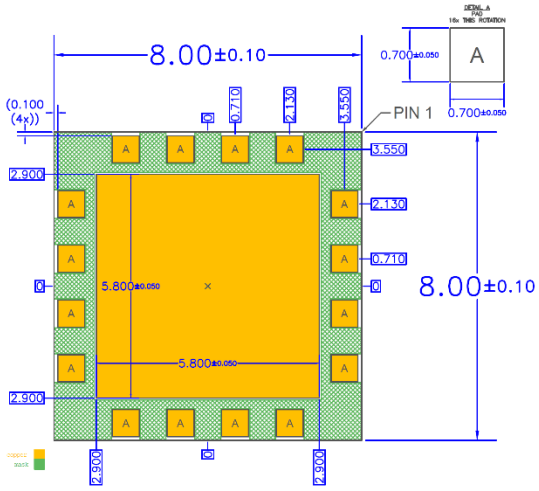
Marking: Pin 1 indicator and Qorvo Logo
Part number – QPB9332
Trace Code – XXXXXXXX (up to 8 characters assigned by sub-contractor)



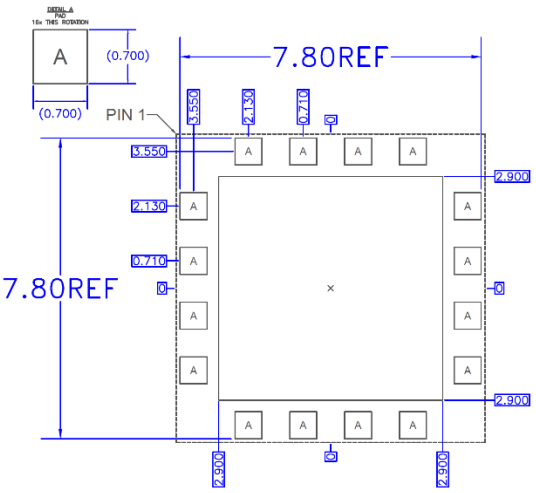
TOP VIEW



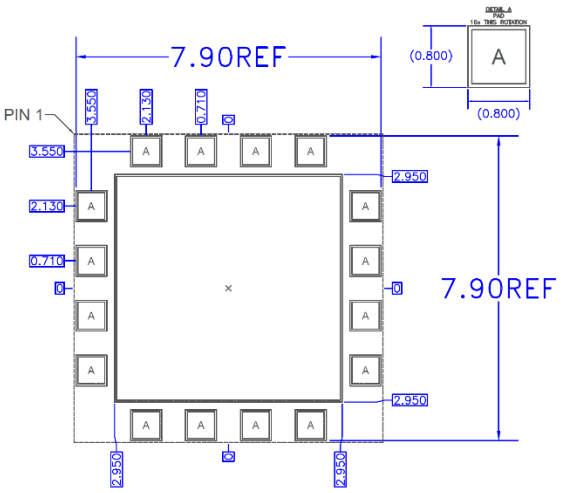
SIDE VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN



RECOMMENDED LAND PATTERN MASK

Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 2	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: Electrolytic plated Au over Ni

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements.
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

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