QPA0001

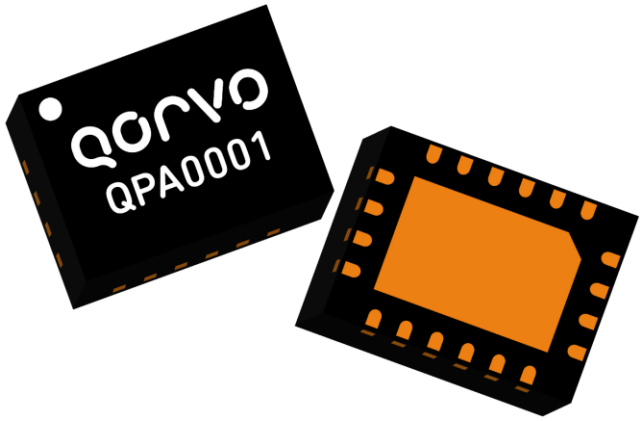
8.5 – 10.5 GHz 2W GaN Driver Amplifier

Product Description

Qorvo's QPA0001 is a packaged driver amplifier fabricated on Qorvo's 0.15 um QGaN15 on SiC process. Operating from 8.5 to 10.5 GHz, the QPA0001 can deliver 2 W saturated output power, 50 % power-added efficiency and 27 dB of large signal gain.

QPA0001 incorporates active bias control to provide customers with bias point stability while reducing system complexity.

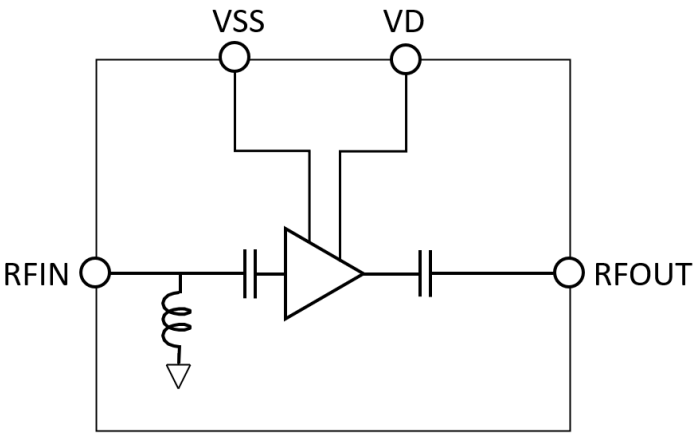
The QPA0001 is available in a 4x3 mm mold encapsulated QFN. With a compact size, it can support tight lattice spacing requirements for phased array radar applications.



Product Features

- Frequency Range: 8.5 – 10.5 GHz
- Small Signal Gain: 33 dB (mid-band)
- Pout: 33 dBm (P_{IN} = 6 dBm)
- Large Signal Gain: 27 dB (@Pin = 6 dBm)
- PAE: 50 % Pulse Mode
- Input Return Loss: 12 dB
- Output Return Loss: 10 dB
- Harmonic: -20 dBc (@ Pin = 6 dBm)
- Active Bias Control: V_D = 16 V, I_{DQ} = 55 mA typical
- Package Dimensions: 4.0 x 3.0 x 0.65 mm

Functional Block Diagram



Applications

- Commercial and military radar
- Communications

Ordering Information

Part No.	Description
QPA0001	Shipping Tray, Qty 50
QPA0001TR7	Tape and Reel 7 ", Qty 250
QPA0001EVB01	QPA0001 Evaluation Board, Qty 1

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Drain Voltage (VD)		16		V
Drain Current (I_{DQ}, self-bias, values are typical)		55		mA
Drain Current Under RF Drive		See plots		mA
Active Gate Control Voltage (Vss)	-3.3	-3	-2.7	V
Active Gate Control Current Under RF Drive		See plots		mA
Temperature (T_{BASE})	−40		+85	°C

Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter [1, 3]	Min	Typ	Max	Units
Operational Frequency Range	8.5		10.5	GHz
Small Signal Gain		33		dB
Input Return Loss		12		dB
Output Return Loss		10		dB
Output Power (@ Pin = 6 dBm) [2]		33		dBm
Power Added Efficiency (@ Pin = 6 dBm) [2]		50		%
Large Signal Gain (@ Pin = 6 dBm) [2]		27		dB
2nd Harmonic Suppression (@ Pin = 6 dBm)		-20		dBc
3rd harmonic Suppression (@ Pin = 6 dBm)		-35		dBc
Small Signal Gain Temperature Coefficient		-0.15		dB/°C

1 Test conditions unless otherwise noted: T_{BASE} = +25 °C, V_D = +16 V, IDQ= 55 mA typical, Vss = -3.0 V.
2. Power tested under pulse mode, PW = 100uS, DC = 10%.
3. Data de-embedded of fixture losses.

Absolute Maximum Ratings

Parameter	Min Value	Max Value	Units
Drain Voltage (VD)	-	29.5	V
Gate Voltage Range (Vss)	-4	-2.5	V
Drain Current (I_{DS})	-	700	mA
Active Gate Control Current (IVss)	-	10	mA
Input Power (P_{IN}), CW, 50 Ω, 85 °C,	-	30	dBm
Input Power (P_{IN}), CW, Output VSWR 3:1, 85 °C	-	30	dBm
Mounting Temperature (30 Seconds)	-	260	°C
Storage Temperature	-55	150	°C

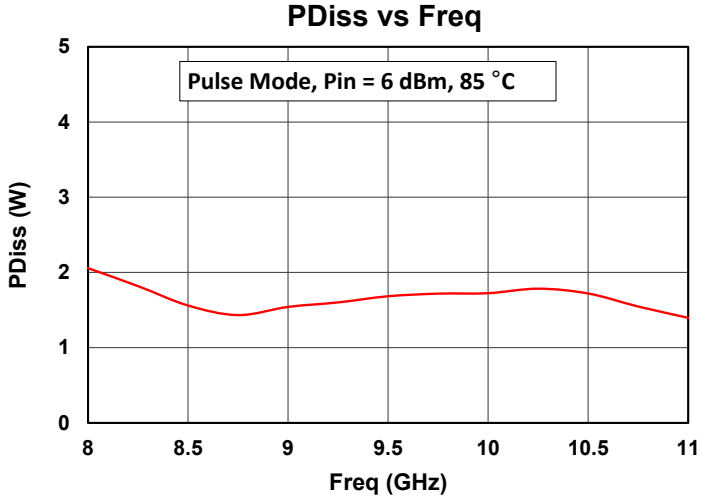
Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

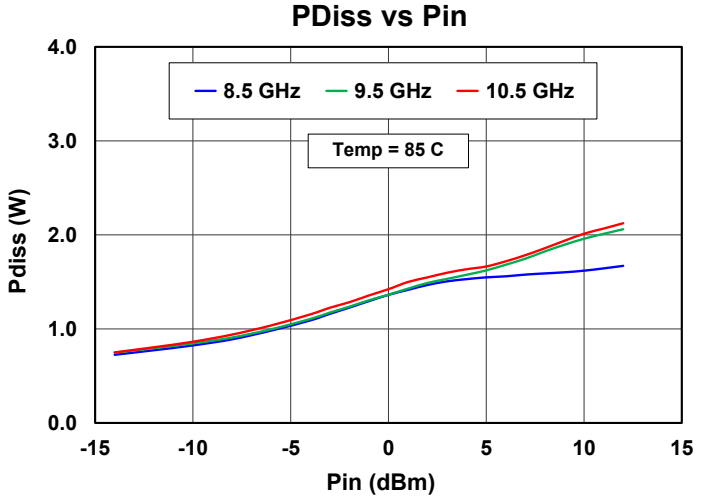
Thermal and Reliability Information

Parameter	Values	Units	Conditions
Under Drive, Thermal Resistance (θ_{JC}) (1,2,3)	11.4	°C/W	T_{BASE} = 85 °C, V_D = +16 V, Pulse Mode, 100uS, 10% Freq = 10.25 GHz, $IDS_{\_DRIVE}$ = 221 mA P_{IN} = +6 dBm, P_{OUT} = +32.4 dBm, P_{DISS} = 1.80 W
Channel Temperature (T_{CH}) 2	105.5	°C	

Notes:

1. Thermal resistance is referenced to the package backside.
2. Base or ambient temperature is 85 °C, channel temperature is IR scan equivalent.
3. Refer to the following document for more information:
   GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

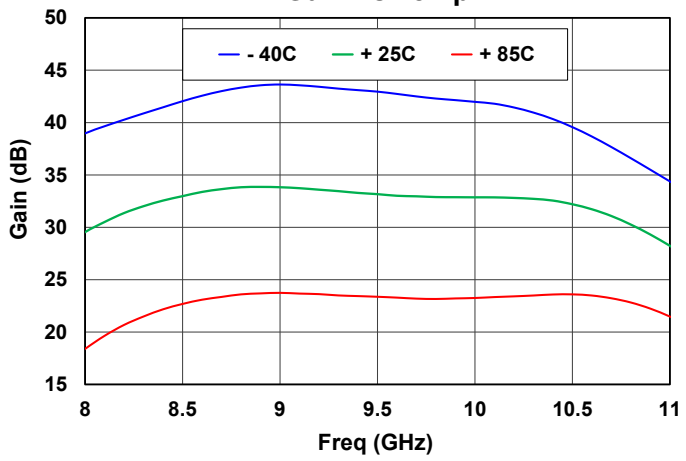




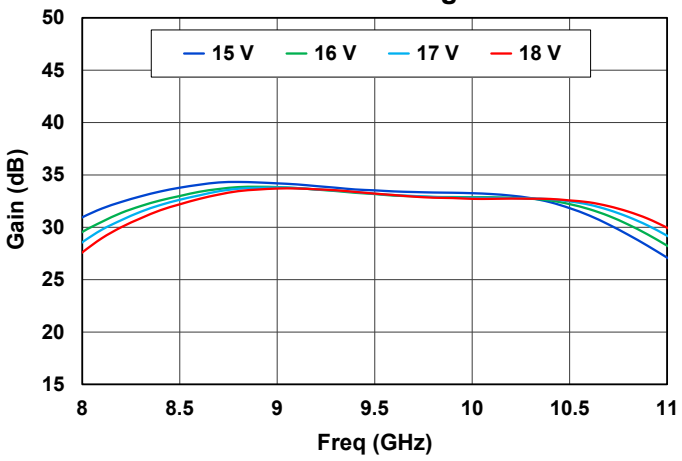
Performance Plots – Small Signal

Test conditions unless otherwise specified: V_D = 16 V, Vss = -3 V, 25 °C

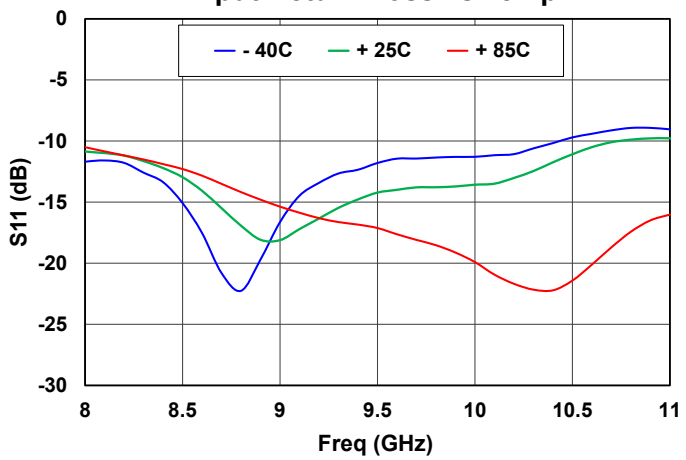
Gain vs Temp



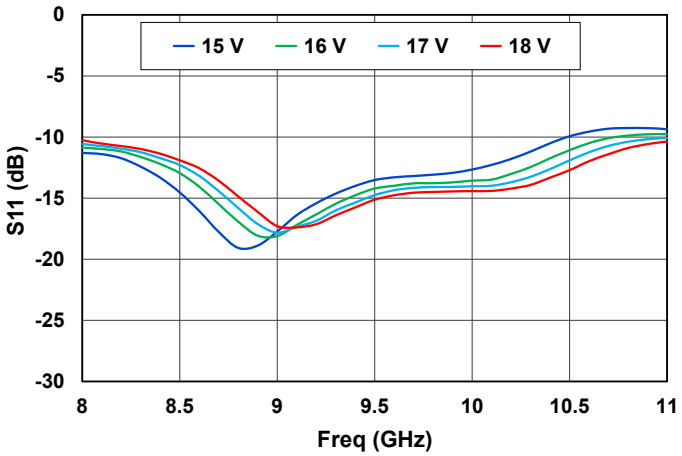
Gain vs Voltage



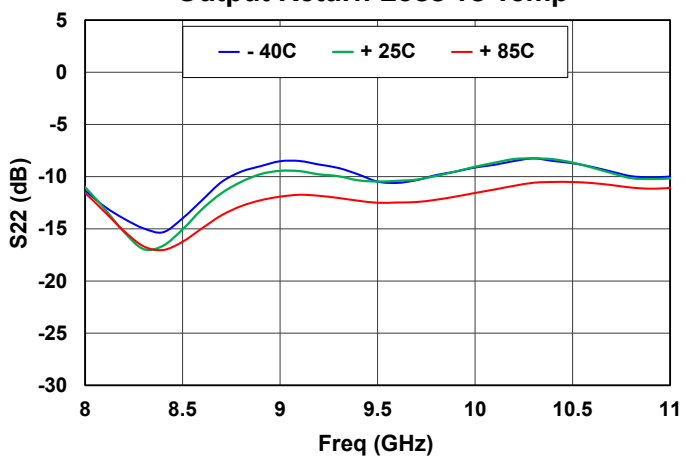
Input Return Loss vs Temp



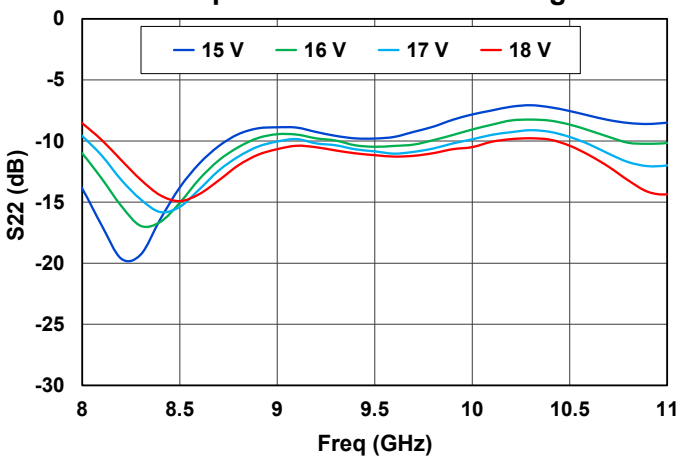
Input Return Loss vs Voltage



Output Return Loss vs Temp



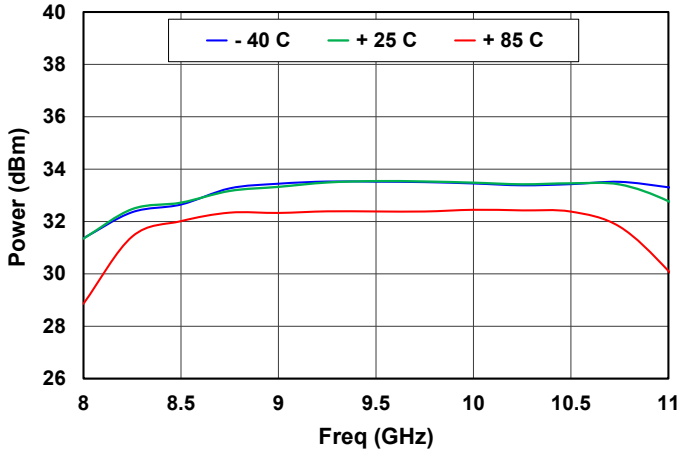
Output Return Loss vs Voltage



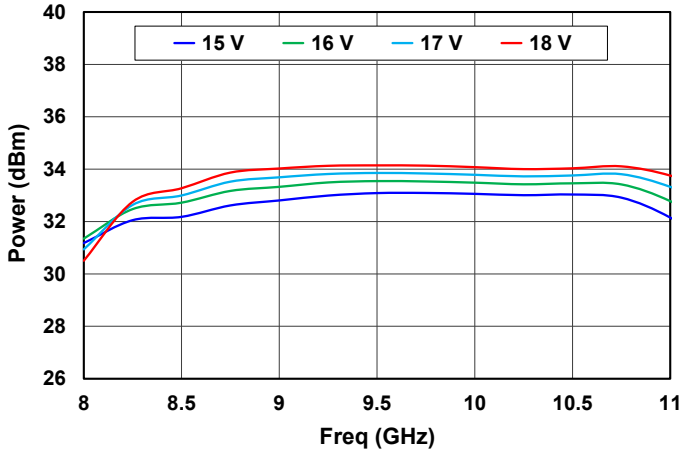
Performance Plots, Large Signal

Test Conditions unless otherwise stated: VD = 16 V, Vss = -3 V, Pulse Pin = 6 dBm, PW = 100 uS, DC = 10%, 25 °C

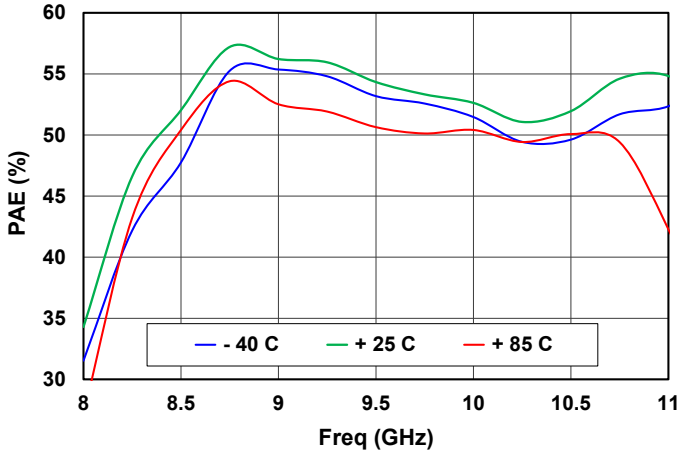
Power vs Temperature



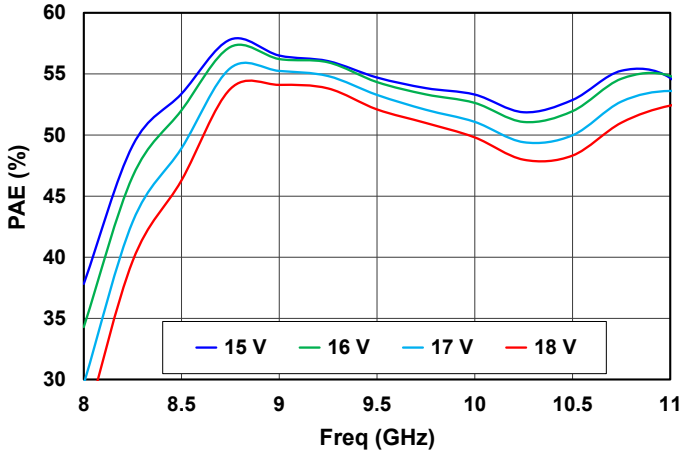
Power vs Voltage



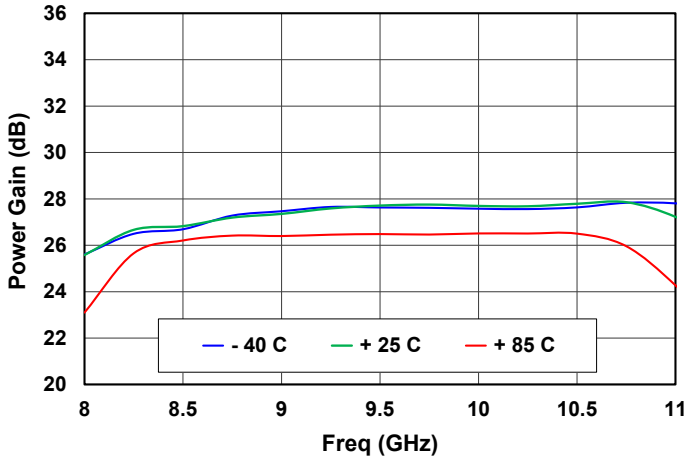
PAE vs Temperature



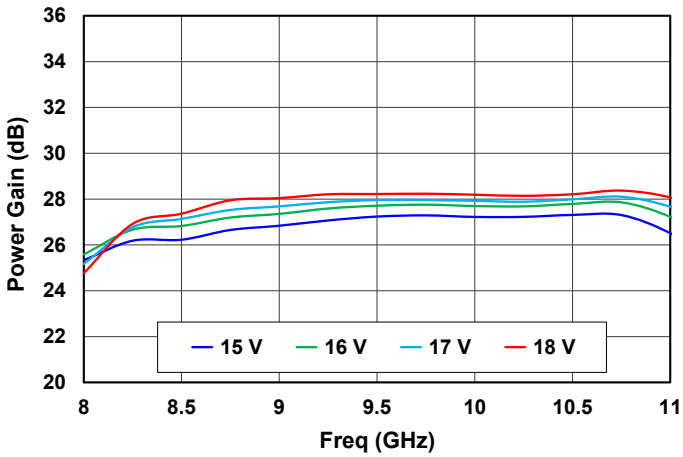
PAE vs Voltage



Power Gain vs Temperature

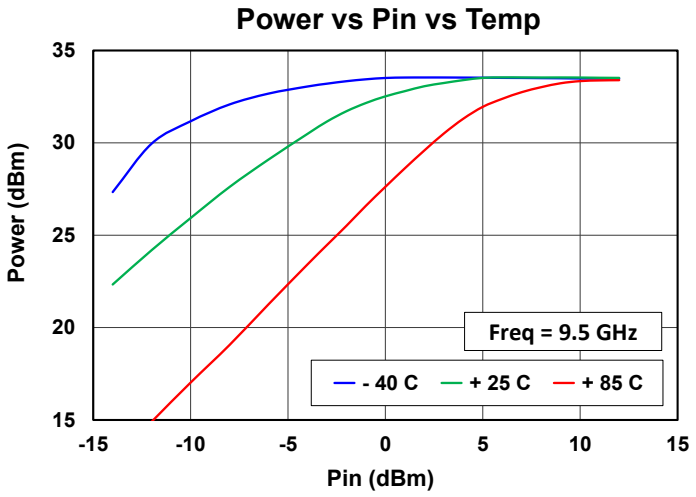


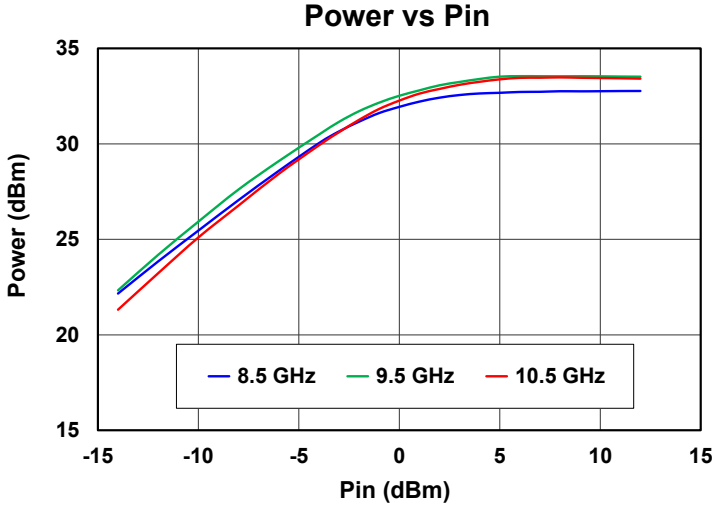
Power Gain vs Voltage

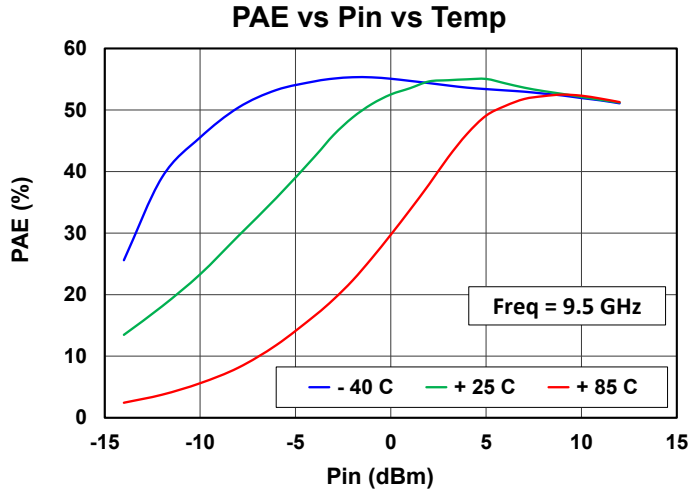


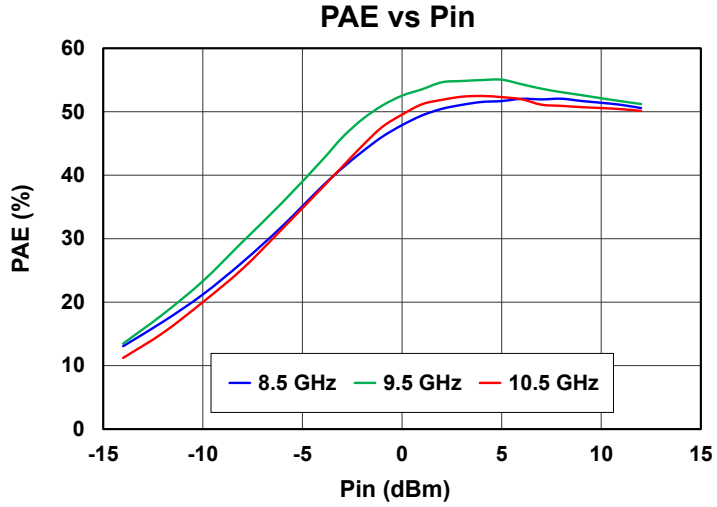
Power Sweep

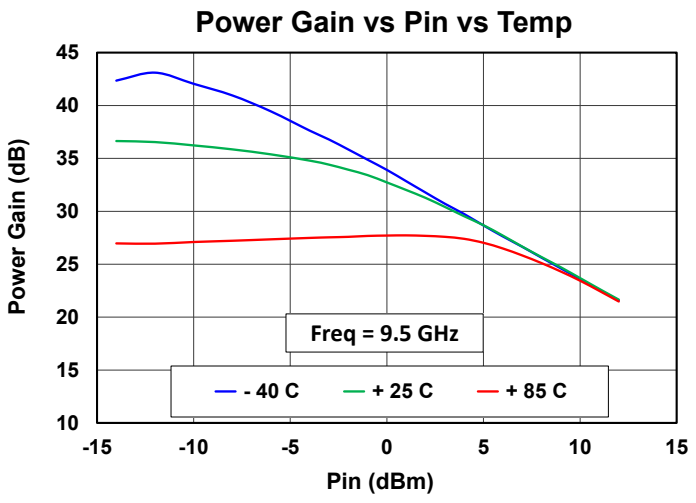
Test Conditions unless otherwise stated: VD = 16 V, Vss = -3 V, Pulse Mode, PW = 100 uS, DC = 10%, 25 °C

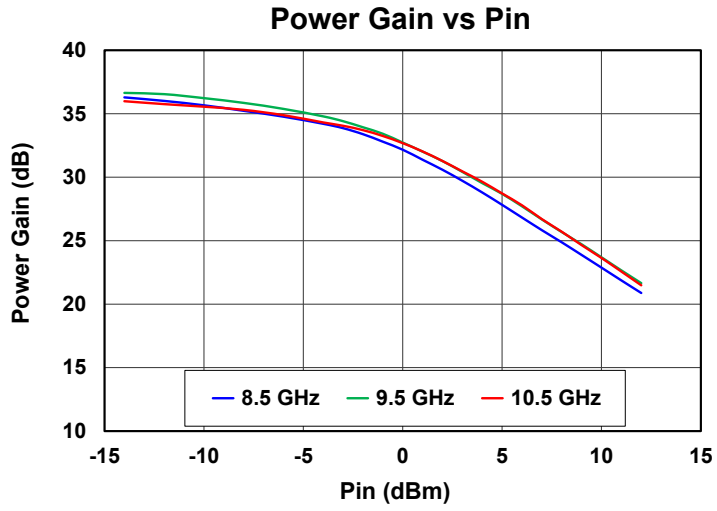








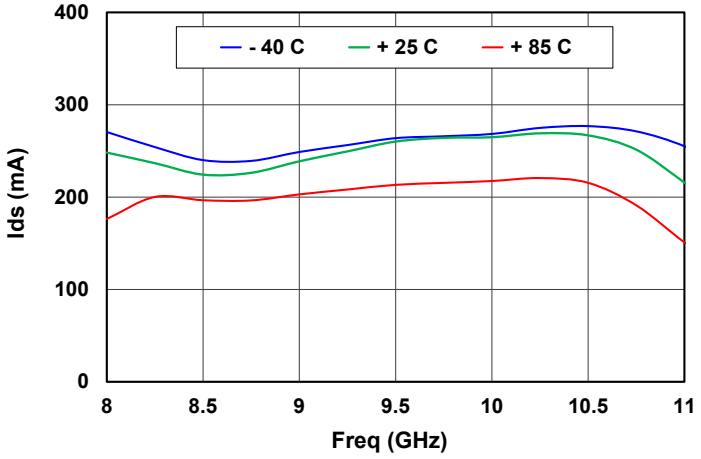




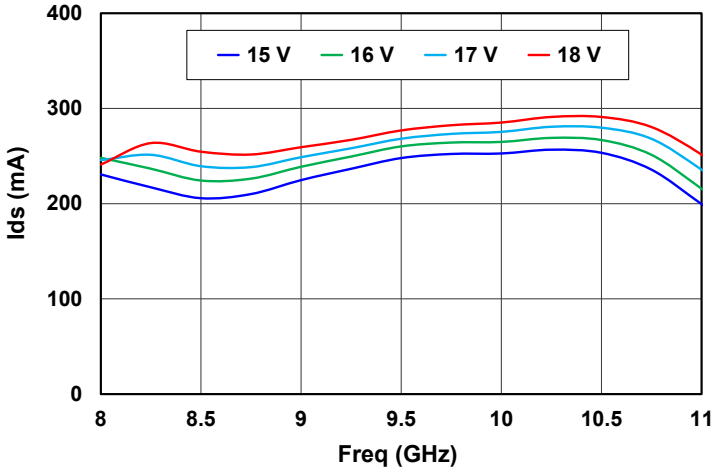
Power Sweep

Test Conditions unless otherwise stated: VD = 16 V, Vss = -3 V, Pulse Pin = 6 dBm, PW = 100 uS, DC = 10%, 25 °C

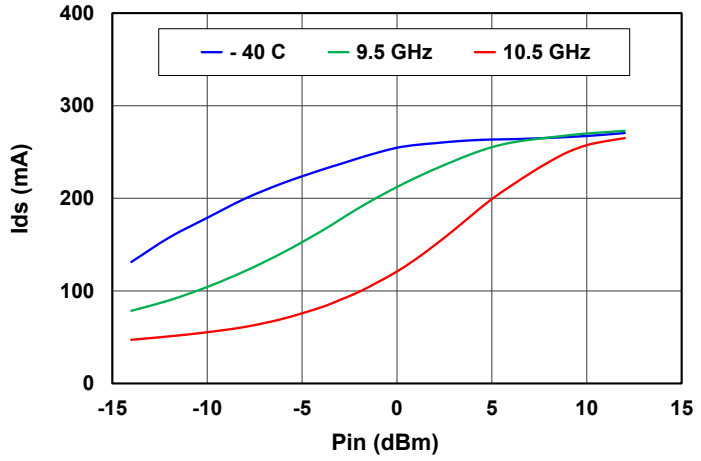
Drain Current vs Temperature



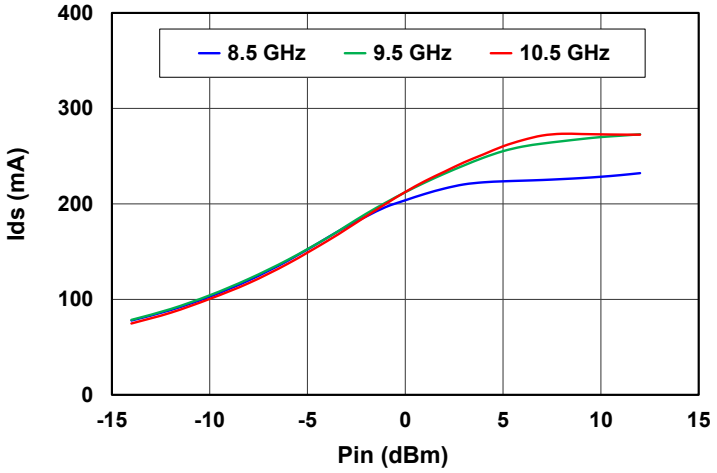
Drain Current vs Voltage



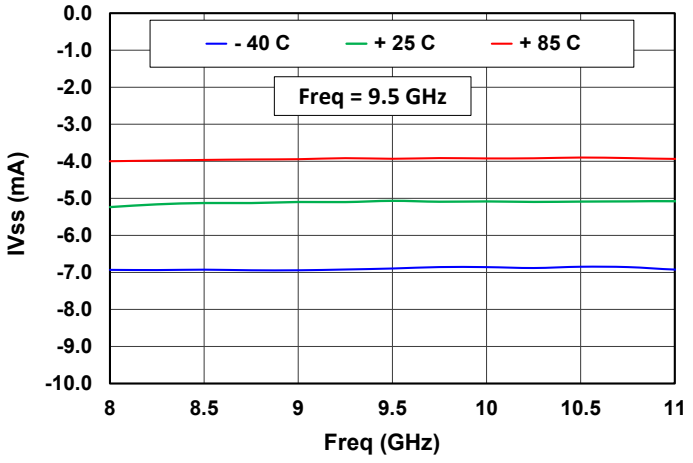
Drain Current vs Temp



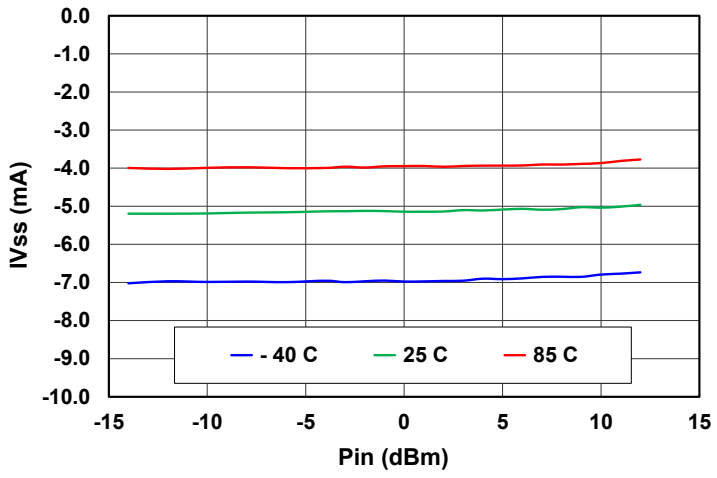
Drain Current vs Pin



Bias Control Currnet vs Temperature

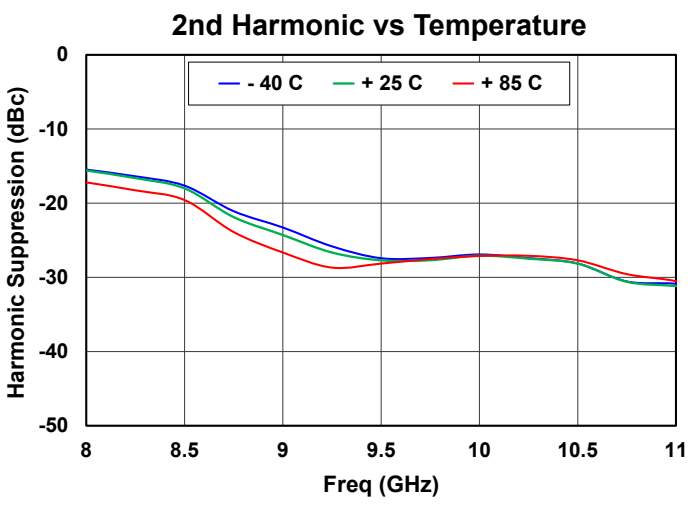


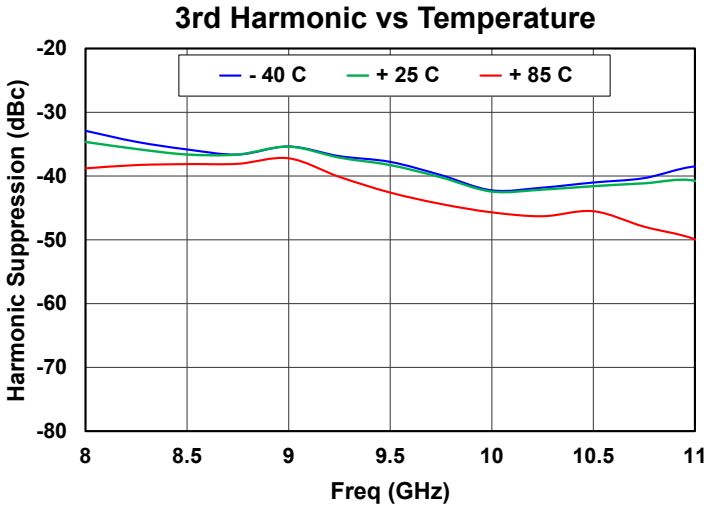
Bias Control Current vs Pin

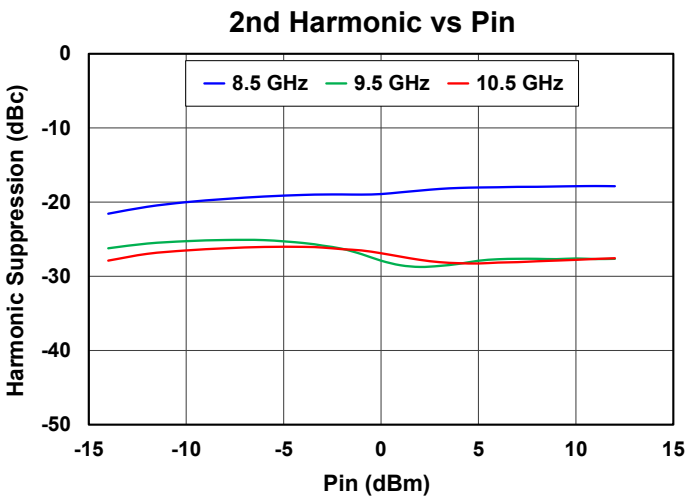


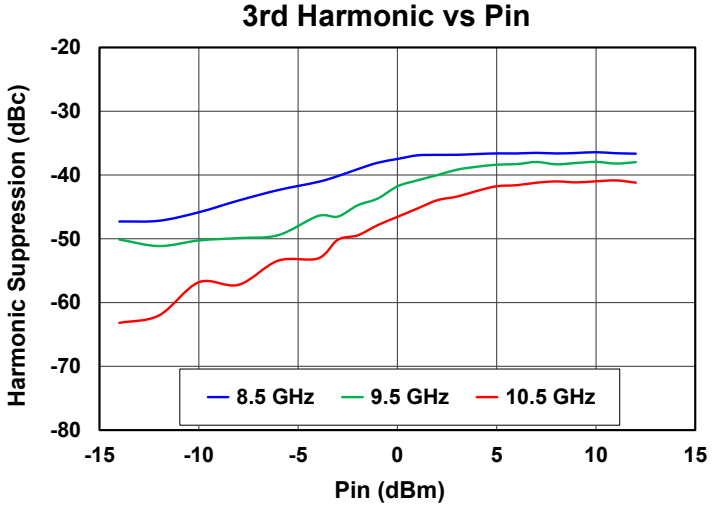
Harmonic Suppressions

Test Conditions unless otherwise stated: VD = 16 V, Vss = -3 V, Pulse Pin = 6 dBm, PW =100 uS, DC = 10%, 25 °C

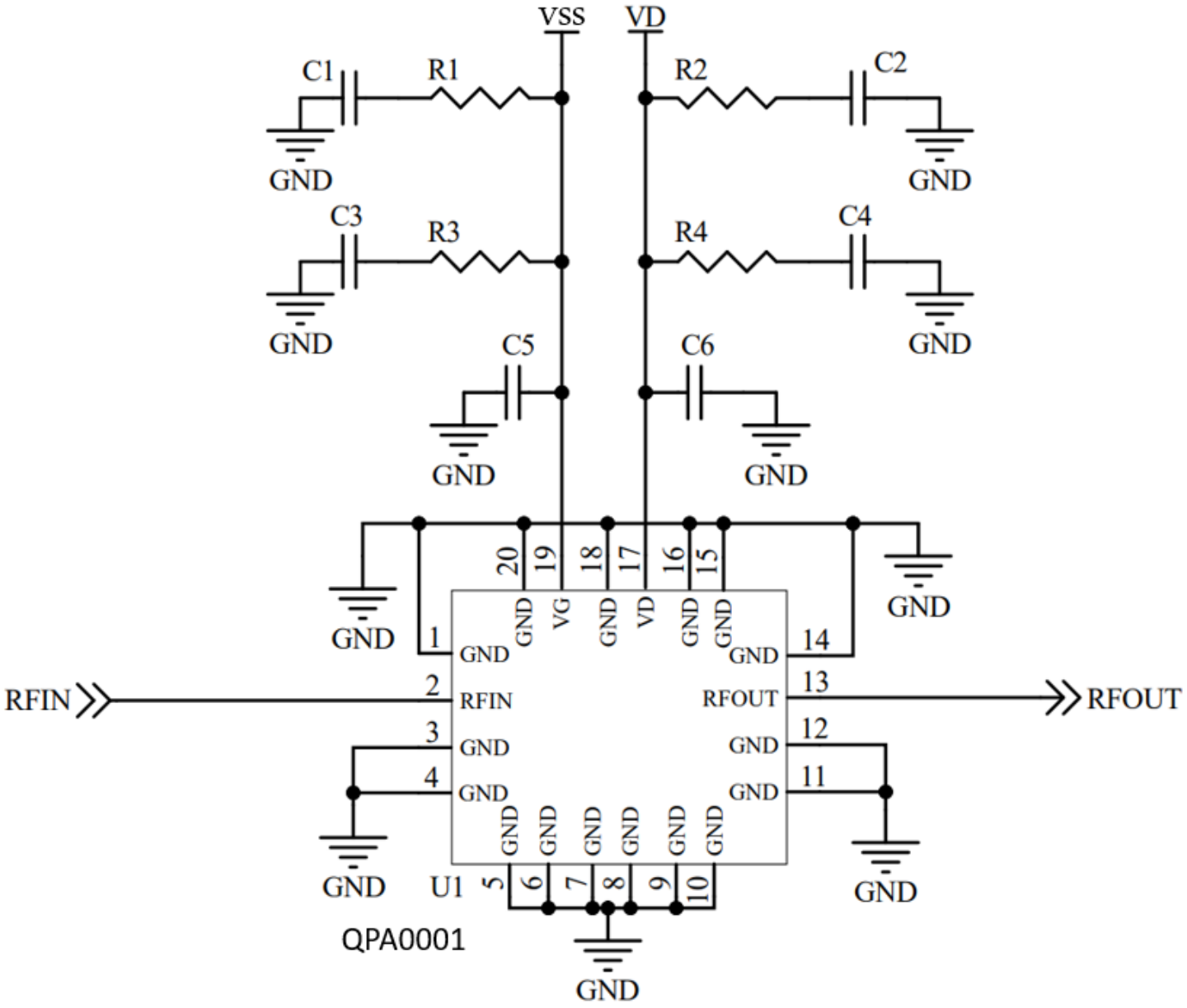








Application Circuit



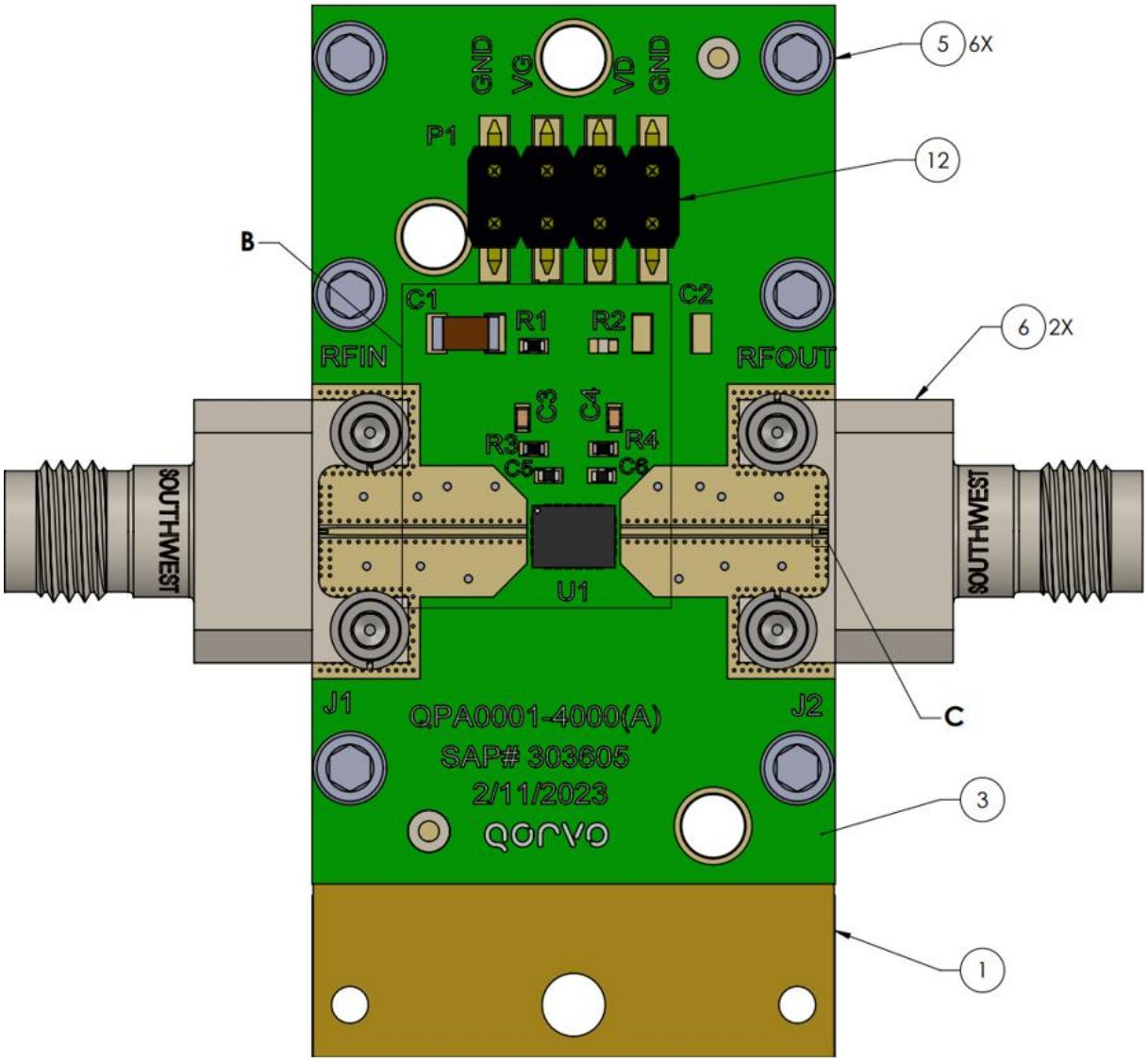
Bias Up Procedure

1. Set VD limit to 700 mA, Vss limit to 10 mA
2. Apply −3 V to Vss
3. Apply +16 V to VD, current should be around 55 mA
4. Turn on RF supply

Bias Down Procedure

1. Turn off RF supply
2. Turn off VD supply
3. Turn off Vss supply

EVB and BOM

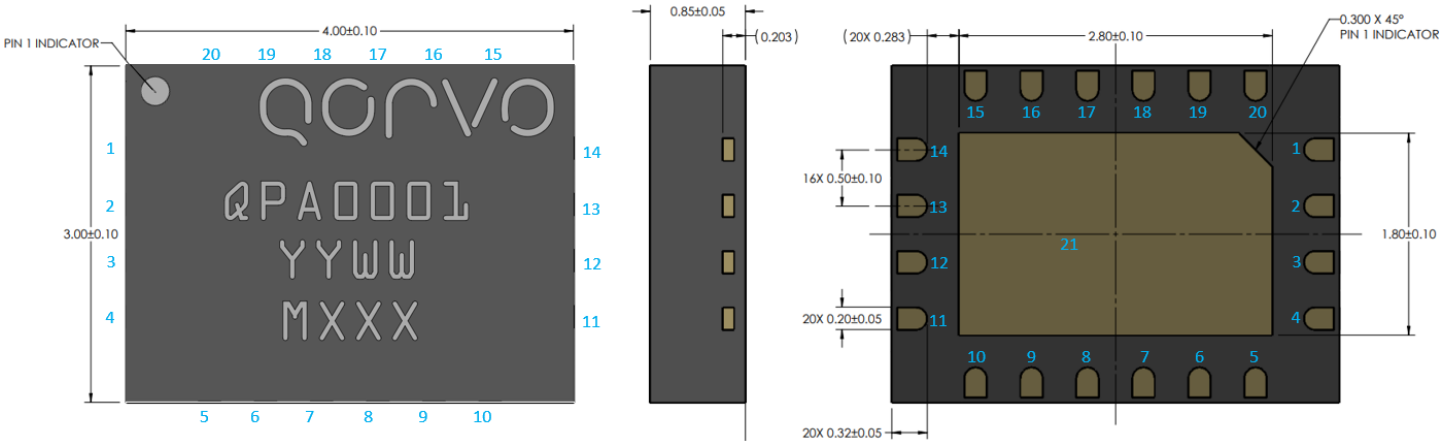


RF Layer is 0.008” thick Rogers Corp. RO4003C, ε_r = 3.38. Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector.
Off-chip components not listed below are not populated, VG is connected to Vss.

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1	10 µF	Cap, 10 uF, 1206, 50V, X5R, 20%	Various	
C5, C6	1000 pF	Cap, 1000pF, 0402, 50V, X7R, 10%	Various	
C3, C4	0.1 uF	Cap, 0.1 uF, 0402, 50V, X7R, 10%	Various	
R1	2 Ohms	Res, 2 Ohm, 0402, 1/16W, 5%	Various	
R3, R4	10 Ohms	Res, 10 Ohm, 0402, 1/10W, 5%	Various	
J1, J2	-	CONN, 2.92mm, end launch, F.	Southwest Microwave	1092-01A-12

Pin Configuration and Description



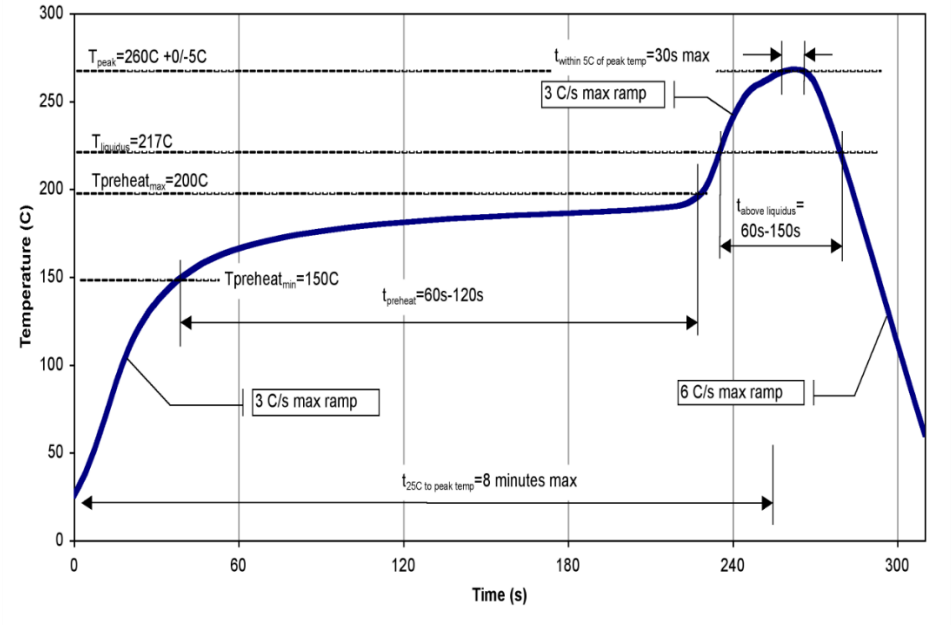
Dimensions in mm.
Package is mold encapsulated. Package lead finish is gold plated with typical gold thickness of 0.1 um
Part Marking: QPA0001: Part Number, YY = Part Assembly Year, WW = Part Assembly Week, MXXX = Batch ID

Pin No.	Label	Description
1, 3-12, 14-16, 18, 20	NC	No internal connections, can be grounded
2	RFIN	Input; matched to 50 Ω; DC grounded
19	Vss	Active gate control
13	RFOUT	Output; matched to 50 Ω; DC blocked
17	VD	Drain power supply
21	GND	Package base ground

Solderability

1. Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C peak reflow temperature.

Recommended Soldering Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1C	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	C2b	ESDA / JEDEC JS-002-2014
MSL – Convection Reflow 260 °C	3	JEDEC standard IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

Important Notices

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