QS91

QFN Style
Solder-Down
Computer On Module

- 27mm square
- 2.6mm total height
- QS family pin-compatible
- Solder-down version
- QFN type lead style
  - 1mm pitch
  - 100 pads
  - Thermal pad
- Visual solder joint inspection possible after soldering
- Single-sided assembly
- 3.3V power supply

Key Features

- NXP i.MX 91 — ARM® Cortex®-A55, 1.4 GHz; NXP's EdgeLock® secure enclave
- RAM — 512 MB LPDDR4
- ROM — 4 GB eMMC
- Grade — Industrial
- Temperature — -25°C to 85°C
- Display support
  - RGB Display Interface
- Connectivity
  - 2x USB 2.0
  - Ethernet, RGMII
  - 1x eMMC/SD
  - 2x CAN-FD
  - 8x UART, 7x I²C, 8x SPI, PWM, SAI, 2x FLEXIO
  - ADC (4-channel, 12-bit), Tamper Detection
  - Up to 60x 3.3V General Purpose I/O

OS Support

- Linux

i.MX 91

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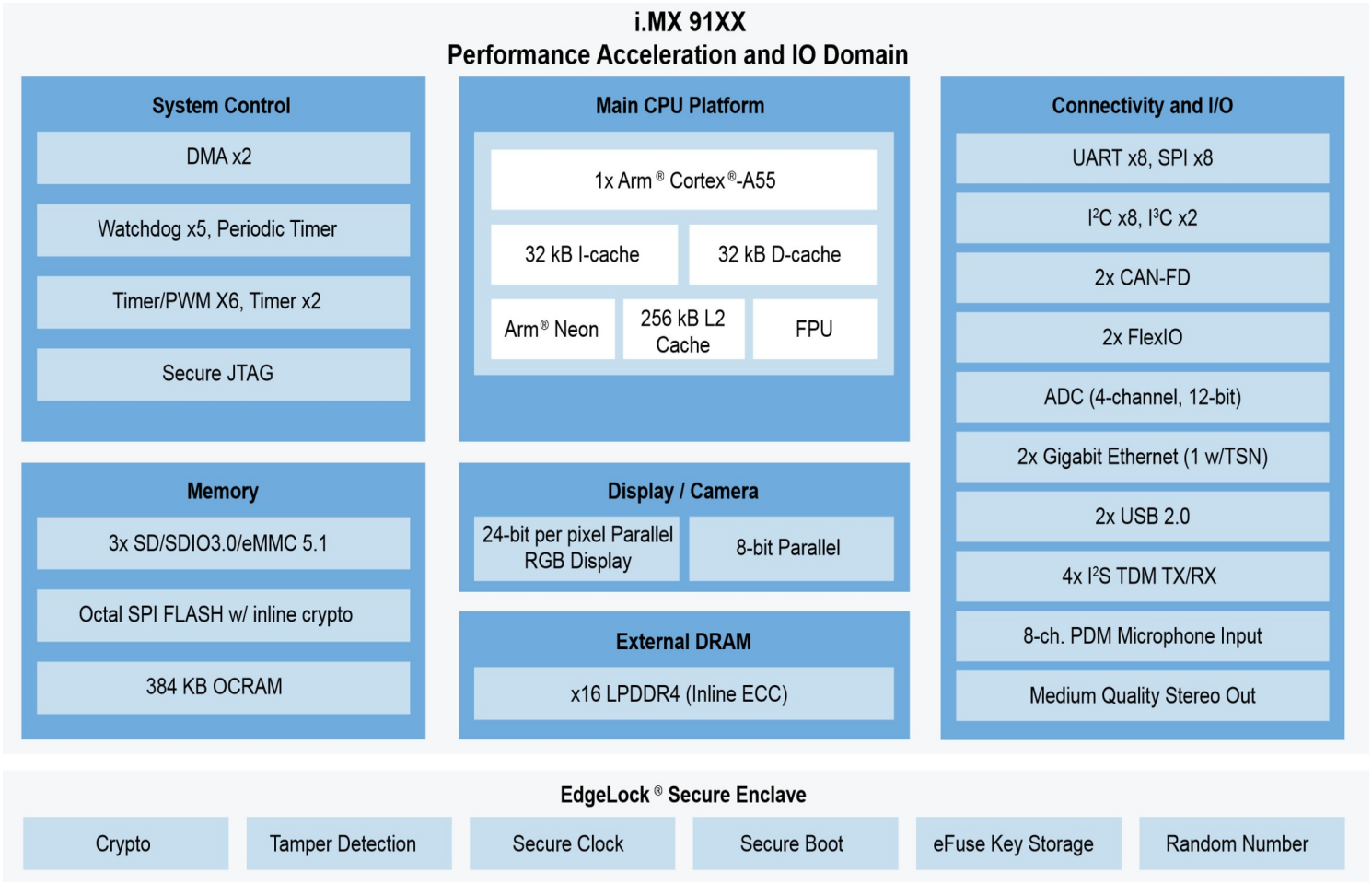

QS91 – QSRZ – QSMP – Differentiating Features

	QS91 NXP i.MX 9131	**QSRZ** Renesas RZ/G2L	**QSMP-1570** STM32MP157C	**QSMP-1350** STM32MP135C
Primary Arm® Core	Cortex®-A55 1.4 GHz	2x Cortex®-A55 1.2 GHz	2x Cortex®-A7 650 MHz	Cortex®-A7 650 MHz
Secondary Arm® Core	-	Cortex®-M33 200 MHz	Cortex®-M4 200 MHz	-
RAM	512MB LPDDR4	512MB/1GB DDR3L	256MB/512MB DDR3L	256MB DDR3L
ROM	4 GB eMMC	4 GB eMMC	4 GB eMMC	4 GB eMMC
Display Interface	RGB	RGB + MIPI DSI	RGB + MIPI DSI	RGB
GPU	-	Yes	Yes	-
Video De-/Encode	-	Yes	-	-
Compatibiliy	27mm QS Standard Pinout			
Temperature	-25°C to 85°C	-40°C to 85°C	-25°C to 85°C	-25°C to 85°C

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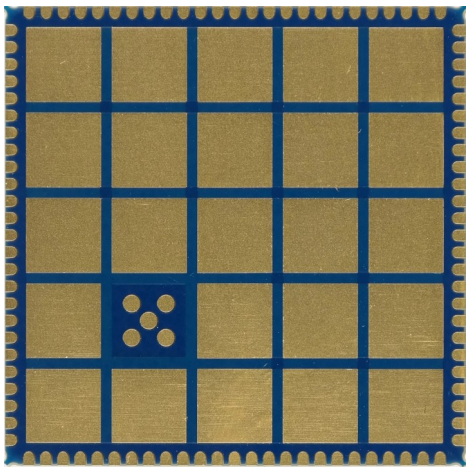
QFN Style Computer On Module Advantages

Defined Return Path

The reason PCB layout becomes more and more important is because of the trend to faster, higher integrated, smaller formfactors, and lower power electronic circuits. The higher the switching frequencies are, the more radiation may occur on a PCB. With good layout, many EMI problems can be minimized to meet the required specifications.

When a module or component is used in a design, the supplier specifies the basis for such a layout. It's not only the pinout which should lead to an easy wiring without the need for crossings. He also has to provide a proper solution for the signal path back to the module. If this return path, mostly the ground plane, cannot be connected near the signal pin, the return current has to take another way and this may result in a loop area. The larger the area, the more radiation and EMI problems may occur.

Ka-Ro QSCOM modules uses a large ground pad on the bottom side. With this a defined ground plane connection is available for all signals. In addition to have a good return path for all signals this large ground pad can be used for cooling.



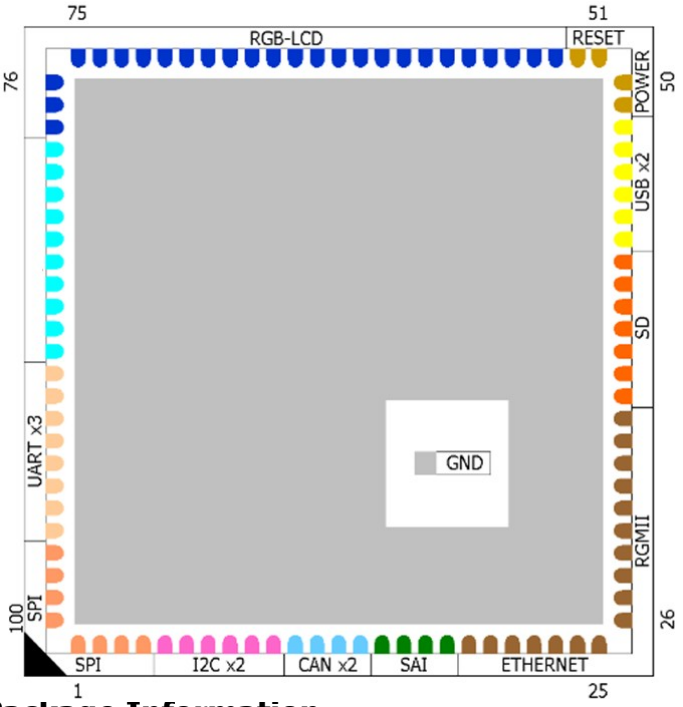
Easy Wiring - Even 2-layer printed circuit boards can be used.

With a solid ground plane on the bottom layer, high speed signals can be routed on the top layer at a defined impedance. However, this is only possible if a peripheral or plug can be connected directly without crossing other routes.

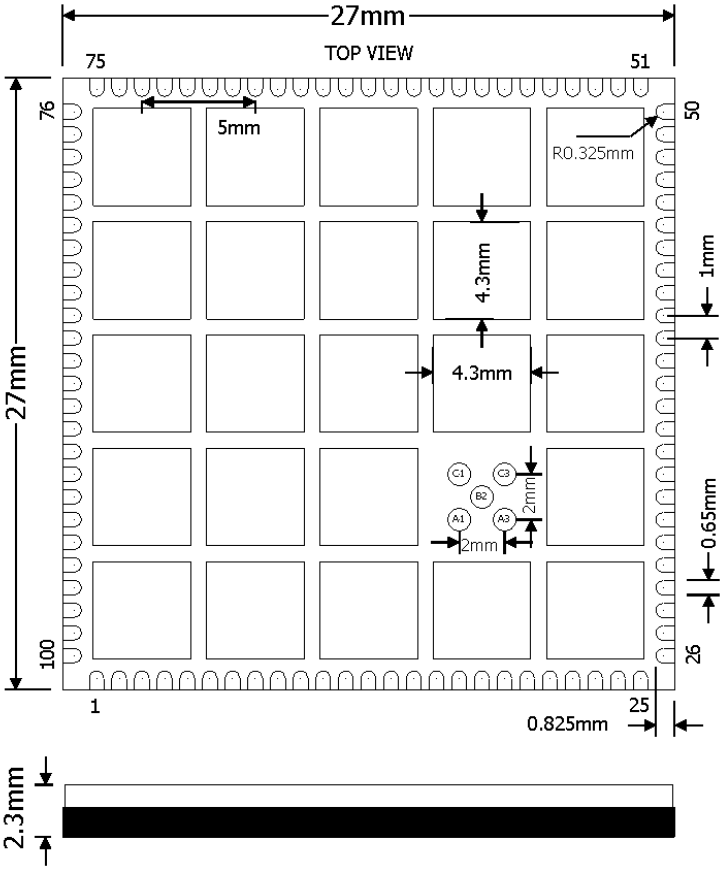
Advanced Soldering

Using a large solder pad underneath the component has not only electrical and thermal advantages. It is also used to hold the component at a defined height during soldering, without the solder being compressed by the weight of the components, which could result in short circuits.

Standard Contact Assignments

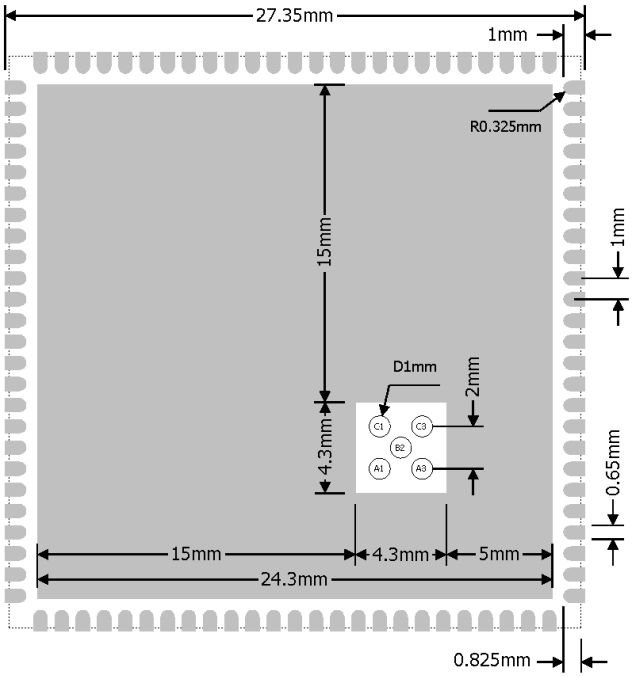


Package Information

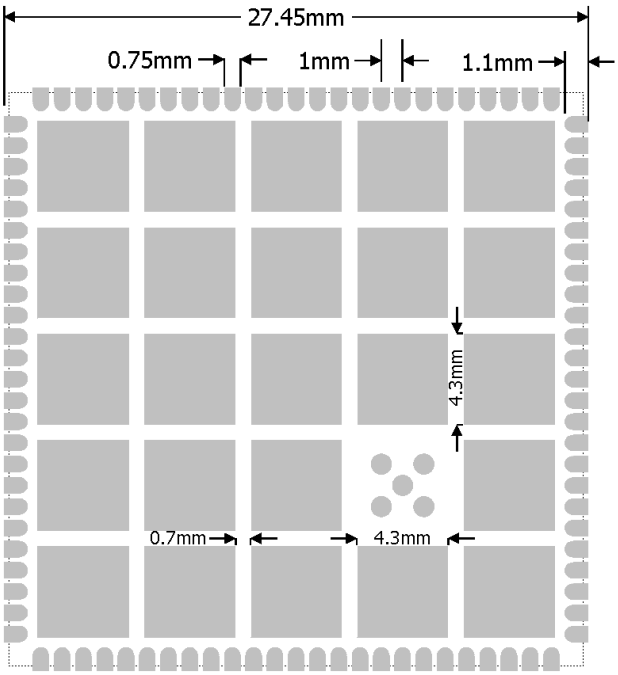


Layout Guidelines

Land pattern

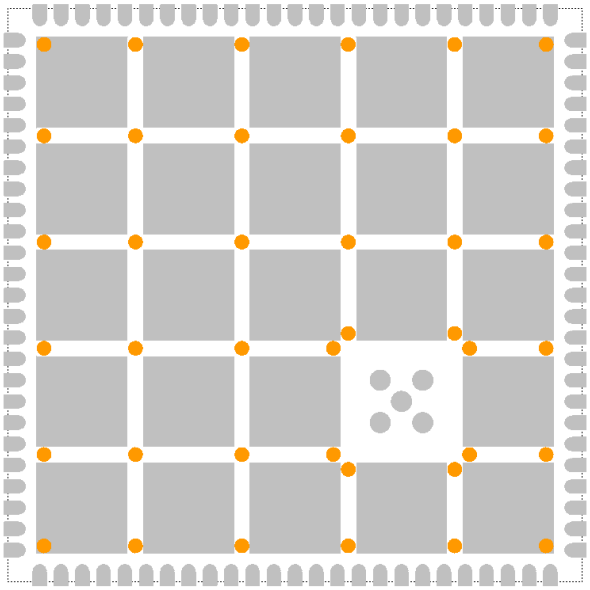


See figure above for the suggested module layout. The five 1mm pads in the square GND pad cutout can be omitted if no JTAG Boundary Scan test is used. The solder mask openings are shown below.



The ground pad solder mask on the bottom side of the QSCOM module is divided into sections for a better reliability of the solder joint and self-alignment of the component.

If the via holes used on the application board have a diameter larger than 0.3 mm, it is recommended to mask the via holes to prevent solder wicking through the via holes. Solders have a habit of filling holes and leaving voids in the thermal pad solder junction, as well as forming solder balls on the other side of the application board which can in some cases be problematic. The 0.7mm wide solder mask stripes can be used to arrange the vias as shown here:

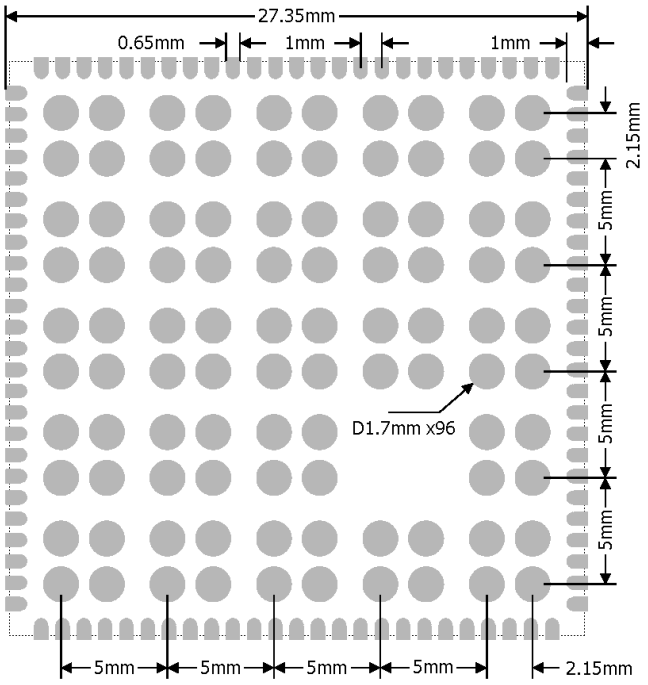


Soldering Recommendations

Ka-Ro QSCOM modules are compatible with industrial standard reflow profile for Pb-free solders. Ka-Ro will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendations should be taken as a starting point guide.

- Refer to technical documentations of particular solder paste for reflow profile configurations
- Avoid using more than one flow.
- A 150µm stencil thickness is recommended.
- Aperture size of the stencil should be 1:1 with the pad size.
- A low residue, "no clean" solder paste should be used due to low mounted height of the component.

Recommended stencil design

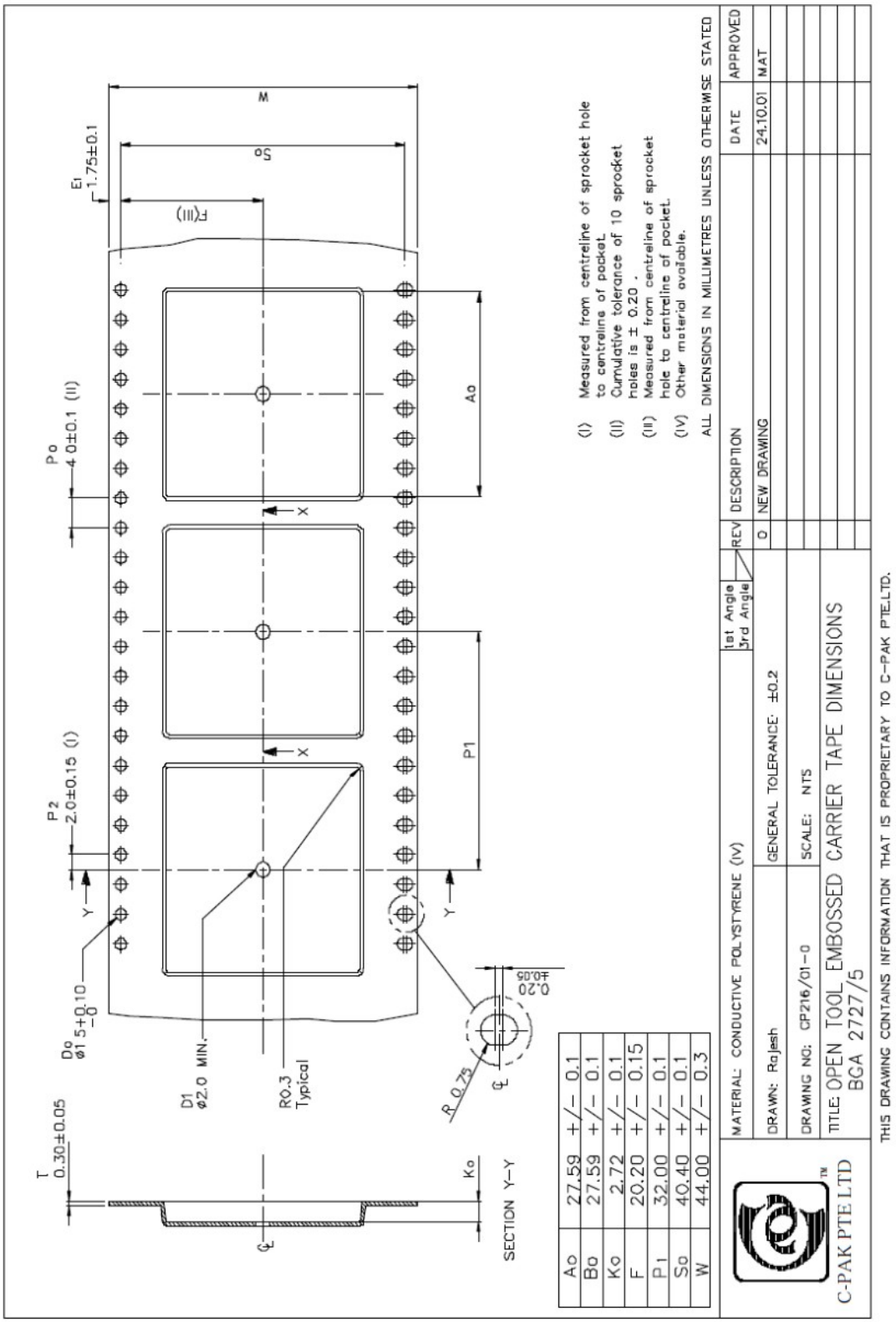


Aperture size of the stencil is 1:1 with the pad size. Four 1.7mm diameter bumps are used for each of the 4.3mm square GND pads sections giving a 50% solder paste padding. The lower component settling with this ensures that the pads at the edge are always soldered even at vertical misalignment by distortion or warping.

Thermal Considerations

A low residue, "no clean" solder paste should be used due to low mounted height of the component.The QSCOM module consume more than 1 W of DC power. In any application where high ambient temperatures for more than a few seconds can occur, it is important that a sufficient cooling surface is provided to dissipate the heat. The thermal pad at the bottom of the module must be connected to the application board ground planes by soldering. The application board should provide a number of vias under and around the pad to conduct the produced heat to the board ground planes, and preferably to a copper surface on the other side of the board in order to conduct and spread the heat. The module internal thermal resistance should in most cases be negligible compared to the thermal resistance from the module into air, and common equations for surface area required for cooling can be used to estimate the temperature rise of the module. Only copper planes on the circuit board surfaces with a solid thermal connection to the module ground pad will dissipate heat. For an application with high load the maximum allowed ambient temperature should be reduced due to inherent heating of the module, especially with small fully plastic enclosed applications where heat transfer to ambient air is low due to low thermal conductivity of plastic. The module measured on the evaluation board exhibits a temperature rise of about 20°C above ambient temperature. An insufficiently cooled module will rapidly heat beyond operating range in ambient room temperature.

Packaging


M
So
E1 1.75±0.1
F(III)
Po 4.0±0.1 (II)
Ao
P2 2.0±0.15 (I)
P1
Do ø1.5+0.10 -0
D1 ø2.0 MIN.
R0.3 Typical
R 0.75
0.20 +0.05
T 0.30±0.05
Ko
SECTION Y-Y
(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED
REV DESCRIPTION DATE APPROVED
0 NEW DRAWING 24.10.01 MAT
1st Angle 3rd Angle
MATERIAL: CONDUCTIVE POLYSTYRENE (IV)
DRAWN: Rajesh
GENERAL TOLERANCE: ±0.2
DRAWING NO: CP216/01-0
SCALE: NTS
TITLE: OPEN TOOL EMBOSSED CARRIER TAPE DIMENSIONS BGA 2727/5
C-PAK PTE LTD
THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO C-PAK PTE.LTD.
Ao 27.59 +/- 0.1
Bo 27.59 +/- 0.1
Ko 2.72 +/- 0.1
F 20.20 +/- 0.15
P1 32.00 +/- 0.1
So 40.40 +/- 0.1
W 44.00 +/- 0.3

PINOUT

PIN	Type	QS Standard	i.MX91 Pad Name	Alternate functions	GPIO	Description (refer to i.MX 91 manuals for details)
POWER SUPPLY & RESET						
1st SPI						
1	3V3	SPIA_NSS	SAI1_TXFS	SAI1_TX_SYNC SAI1_TX_DATA01 **LPSPI1_PCS0** LPUART2_DTR_B MQS1_LEFT	GPIO1[11]	BOOT_MODE2 (i.MX93 internal pull-down)
2	3V3	SPIA_MISO	SAI1_TXC	SAI1_TX_BCLK LPUART2_CTS_B **LPSPI1_SIN** LPUART1_DSR_B CAN1_RX	GPIO1[12]	
3	3V3	SPIA_MOSI	SAI1_RXD0	SAI1_RX_DATA00 SAI1_MCLK **LPSPI1_SOUT** LPUART2_DSR_B MQS1_RIGHT	GPIO1[14]	
4	3V3	SPIA_SCK	SAI1_TXD0	SAI1_TX_DATA00 LPUART2_RTS_B **LPSPI1_SCK** LPUART1_DTR_B CAN1_TX	GPIO1[13]	BOOT_MODE3 (i.MX93 internal pull-down)
I2C						
5	3V3	I2CA_SCL	I2C2_SCL	**LPI2C2_SCL** I3C1_PUR LPUART2_DCB_B I3C1_PUR_B TPM2_CH2 SAI1_RX_SYNC	GPIO1[2]	
6	3V3	I2CA_SDA	I2C2_SDA	**LPI2C2_SDA** LPUART2_RIN_B TPM2_CH3 SAI1_RX_BCLK	GPIO1[3]	
7	3V3	INTA	ENET2_MDC	ENET2_MDC LPUART4_DCB_B SAI2_RX_SYNC FLEXIO2_FLEXIO14	GPIO4[14]	
8	3V3	I2CB_SCL	GPIO_IO29	**LPI2C3_SCL** FLEXIO1_FLEXIO29	GPIO2[29]	
9	3V3	I2CB_SDA	GPIO_IO28	**LPI2C3_SDA** FLEXIO1_FLEXIO28	GPIO2[28]	
10	3V3	INTB	ENET2_MDIO	ENET2_MDIO LPUART4_RIN_B SAI2_RX_BCLK FLEXIO2_FLEXIO15	GPIO4[15]	
CAN						
11	3V3	CANA_RX	PDM_BIT_STREAM0	PDM_BIT_STREAM00, MQS1_RIGHT LPSPI1_PCS1 TPM1_EXTCLK LPTMR1_ALT2 **CAN1_RX**	GPIO1[9]	
12	3V3	CANA_TX	PDM_CLK	PDM_CLK MQS1_LEFT LPTMR1_ALT1 **CAN1_TX**	GPIO1[8]	
13	3V3	CANB_RX	SD2_DATA1	USDHC2_DATA1 ENET2_1588_EVENT1_IN **CAN2_RX**, FLEXIO1_FLEXIO04 CCMSRCGPCMIX_WAIT	GPIO3[4]	
14	3V3	CANB_TX	SD2_DATA0	USDHC2_DATA0 ENET2_1588_EVENT0_OUT **CAN2_TX**, FLEXIO1_FLEXIO03 CCMSRCGPCMIX_OBSERVE2	GPIO3[3]	

PIN	Type	QS Standard	i.MX91 Pad Name	Alternate functions	GPIO	Description (refer to i.MX 91 manuals for details)
SAI						
15	3V3	SAI_TX	ENET2_RX_CTL	ENET2_RGMII_RX_CTL LPUART4_DSR_B **SAI2_TX_DATA00** FLEXIO2_FLEXIO22	GPIO4[22]	
16	3V3	SAI_RX	ENET2_TD3	ENET2_RGMII_TD3 **SAI2_RX_DATA00** FLEXIO2_FLEXIO16	GPIO4[16]	
17	3V3	SAI_SCK	ENET2_TXC	ENET2_RGMII_TXC ENET2_TX_ER **SAI2_TX_BCLK** FLEXIO2_FLEXIO21	GPIO4[21]	
18	3V3	SAI_FS	ENET2_TX_CTL	ENET2_RGMII_TX_CTL LPUART4_DTR_B **SAI2_TX_SYNC** FLEXIO2_FLEXIO20	GPIO4[20]	
ETHERNET						
19	3V3	ENET_RST	SD2_CLK	USDHC2_CLK ENET1_1588_EVENT0_ OUT, I3C2_SDA, FLEXIO1_FLEXIO01 CCMSRCGPCMIX_OBSERVE0	GPIO3[1]	
20	3V3	ENET_CK125	CCM_CLKO1	CCMSRCGPCMIX_CLKO1 FLEXIO1_FLEXIO26	GPIO3[26]	
21	3V3	ENET_INT	SD2_DATA2	USDHC2_DATA2 ENET2_1588_EVENT1_OUT MQS2_RIGHT, FLEXIO1_FLEXIO05 CCMSRCGPCMIX_STOP	GPIO3[5]	
22	3V3	ENET_MDIO	ENET1_MDIO	ENET1_MDIO LPUART3_RIN_B I3C2_SDA HSIOMIX_OTG_PWR1 FLEXIO2_FLEXIO01	GPIO4[1]	
23	3V3	ENET_MDC	ENET1_MDC	ENET1_MDC LPUART3_DCB_B I3C2_SCL HSIOMIX_OTG_ID1 FLEXIO2_FLEXIO00	GPIO4[0]	
24	3V3	ENET_RXC	ENET1_RXC	CCM_ENET1_CLOCK_ GENERATE_RX_CLK ENET1_RX_ER FLEXIO2_FLEXIO09	GPIO4[9]	
25	3V3	ENET_RX_CTL	ENET1_RX_CTL	ENET1_RGMII_RX_CTL LPUART3_DSR_B HSIOMIX_OTG_PWR2 FLEXIO2_FLEXIO08	GPIO4[8]	
26	3V3	ENET_RXD0	ENET1_RD0	ENET1_RGMII_RD0 LPUART3_RX FLEXIO2_FLEXIO10	GPIO4[10]	
27	3V3	ENET_RXD1	ENET1_RD1	ENET1_RGMII_RD1 LPUART3_CTS_B LPTMR2_ALT1 FLEXIO2_FLEXIO11	GPIO4[11]	
28	3V3	ENET_RXD2	ENET1_RD2	ENET1_RGMII_RD2 LPTMR2_ALT2 FLEXIO2_FLEXIO12	GPIO4[12]	
29	3V3	ENET_RXD3	ENET1_RD3	ENET1_RGMII_RD3 LPTMR2_ALT3 FLEXIO2_FLEXIO13	GPIO4[13]	
30	3V3	ENET_TX_CTL	ENET1_TX_CTL	ENET1_RGMII_TX_CTL LPUART3_DTR_B FLEXIO2_FLEXIO06	GPIO4[6]	
31	3V3	ENET_TXC	ENET1_TXC	CCM_ENET1_CLOCK_ GENERATE_TX_CLK ENET1_TX_ER FLEXIO2_FLEXIO07	GPIO4[7]	
32	3V3	ENET_TXD3	ENET1_TD3	ENET1_RGMII_TD3 CAN2_TX, HSIOMIX_OTG_ID2 FLEXIO2_FLEXIO02	GPIO4[2]	
33	3V3	ENET_TXD2	ENET1_TD2	ENET1_RGMII_TD2 CCM_ENET1_CLOCK_ GENERATE_REF_CLK CAN2_RX HSIOMIX_OTG_OC2 FLEXIO2_FLEXIO03	GPIO4[3]	

PIN	Type	QS Standard	i.MX91 Pad Name	Alternate functions	GPIO	Description (refer to i.MX 91 manuals for details)
34	3V3	ENET_TXD1	ENET1_TD1	ENET1_RGMII_TD1 LPUART3_RTS_B I3C2_PUR HSIOMIX_OTG_OC1 FLEXIO2_FLEXIO04	GPIO4[4]	
35	3V3	ENET_TXD0	ENET1_TD0	ENET1_RGMII_TD0 LPUART3_TX FLEXIO2_FLEXIO05	GPIO4[5]	
SD						
36	3V3	SD_CD	SD2_DATA3	USDHC2_DATA3 LPTMR2_ALT1, MQS2_LEFT FLEXIO1_FLEXIO06 CCMSRCGPCMIX_EARLY_ RESET	GPIO3[6]	
37	3V3	SD_D1	SD3_DATA1	USDHC3_DATA1 FLEXSPI1_A_DATA01 FLEXIO1_FLEXIO23	GPIO3[23]	
38	3V3	SD_D0	SD3_DATA0	USDHC3_DATA0 FLEXSPI1_A_DATA00 FLEXIO1_FLEXIO22	GPIO3[22]	
39	3V3	SD_CLK	SD3_CLK	USDHC3_CLK FLEXSPI1_A_SCLK FLEXIO1_FLEXIO20	GPIO3[20]	
40	3V3	SD_CMD	SD3_CMD	USDHC3_CMD FLEXSPI1_A_SS0_B FLEXIO1_FLEXIO21	GPIO3[21]	
41	3V3	SD_D3	SD3_DATA3	USDHC3_DATA3 FLEXSPI1_A_DATA03 FLEXIO1_FLEXIO25	GPIO3[25]	
42	3V3	SD_D2	SD3_DATA2	USDHC3_DATA2 FLEXSPI1_A_DATA02 FLEXIO1_FLEXIO24	GPIO3[24]	
USB						
43	analog	USBA_VBUS	USB2_VBUS			USB supply voltage input. 4K7 / 10K voltage divider is used to drive USB2_VBUS@3.3V
44	analog	USBA_DN	USB2_D_N			
45	analog	USBA_DP	USB2_D_P			
46	analog	USBB_VBUS	USB1_VBUS			USB supply voltage input. 4K7 / 10K voltage divider is used to drive USB1_VBUS@3.3V
47	analog	USBB_DN	USB1_D_N			
48	analog	USBB_DP	USB1_D_P			
POWER SUPPLY & RESET						
49 50	VIN	3.3V power supply input				
51	POR	PMIC reset input pin. Pulled to LDO1 (1.8V) power rail by an onboard 10K resistor. Asserted low, PMIC performs reset. Leave unconnected, if not used.				
52	BOOT_MODE					L: Boot from FLASH H: Boot from UART
DISPLAY						
53	3V3	**LCD_DE**	GPIO_IO01	LPI2C3_SCL MEDIAMIX_CAM_DATA00 **MEDIAMIX_DISP_DE** LPSPI6_SIN, LPUART5_RX LPI2C5_SCL, FLEXIO1_FLEXIO01	GPIO2[1]	
54	3V3	**LCD_VSYNC**	GPIO_IO02	LPI2C4_SDA MEDIAMIX_CAM_VSYNC **MEDIAMIX_DISP_VSYNC** LPSPI6_SOUT, LPUART5_CTS_B LPI2C6_SDA, FLEXIO1_FLEXIO02	GPIO2[2]	

PIN	Type	QS Standard	i.MX91 Pad Name	Alternate functions	GPIO	Description (refer to i.MX 91 manuals for details)
55	3V3	**LCD_HSYNC**	GPIO_IO03	LPI2C4_SCL MEDIAMIX_CAM_HSYNC **MEDIAMIX_DISP_HSYNC** LPSPI6_SCK LPUART5_RTS_B LPI2C6_SCL FLEXIO1_FLEXIO03	GPIO2[3]	
56	3V3	**LCD_CLK**	GPIO_IO00	LPI2C3_SDA MEDIAMIX_CAM_CLK **MEDIAMIX_DISP_CLK** LPSPI6_PCS0 LPUART5_TX LPI2C5_SDA FLEXIO1_FLEXIO00	GPIO2[0]	
57	3V3	**LCD_R1**	GPIO_IO21	SAI3_TX_DATA00, PDM_CLK **MEDIAMIX_DISP_DATA17** LPSPI5_SCK LPSPI4_SCK TPM4_CH1 SAI3_RX_BCLK	GPIO2[21]	
58	3V3	**LCD_R2**	GPIO_IO22	USDHC3_CLK, SPDIF_IN **MEDIAMIX_DISP_DATA18** TPM5_CH1 TPM6_EXTCLK LPI2C5_SDA FLEXIO1_FLEXIO22	GPIO2[22] 10K-PU	
59	3V3	**LCD_R3**	GPIO_IO23	USDHC3_CMD, SPDIF_OUT **MEDIAMIX_DISP_DATA19** TPM6_CH1 LPI2C5_SCL FLEXIO1_FLEXIO23	GPIO2[23]	
60	3V3	**LCD_R4**	GPIO_IO24	FLEXIO1_FLEXIO24 LPSPI6_PCS1 USDHC3_DATA0 TPM3_CH3 **MEDIAMIX_DISP_DATA20** JTAG_MUX_TDO	GPIO2[24]	
61	3V3	**LCD_R5**	GPIO_IO25	USDHC3_DATA1 CAN2_TX **MEDIAMIX_DISP_DATA21** TPM4_CH3 JTAG_MUX_TCK LPSPI7_PCS1 FLEXIO1_FLEXIO25	GPIO2[25]	
62	3V3	**LCD_R6**	GPIO_IO26	LPSPI8_PCS1 USDHC3_DATA2 TPM5_CH3 **MEDIAMIX_DISP_DATA22** SAI3_TX_SYNC PDM_BIT_STREAM01 JTAG_MUX_TDI	GPIO2[26]	
63	3V3	**LCD_R7**	GPIO_IO27	USDHC3_DATA3, CAN2_RX **MEDIAMIX_DISP_DATA23** TPM6_CH3 JTAG_MUX_TMS LPSPI5_PCS1 FLEXIO1_FLEXIO27	GPIO2[27]	
64	3V3	**LCD_G2**	GPIO_IO14	LPUART3_TX MEDIAMIX_CAM_DATA06 **MEDIAMIX_DISP_DATA10** LPSPI8_SOUT LPUART8_CTS_B LPUART4_TX FLEXIO1_FLEXIO14	GPIO2[14]	
65	3V3	**LCD_G3**	GPIO_IO15	LPUART3_RX MEDIAMIX_CAM_DATA07 **MEDIAMIX_DISP_DATA11** LPSPI8_SCK LPUART8_RTS_B LPUART4_RX FLEXIO1_FLEXIO15	GPIO2[15]	
66	3V3	**LCD_G4**	GPIO_IO16	FLEXIO1_FLEXIO16 LPUART3_CTS_B LPUART4_CTS_B LPSPI4_PCS2 **MEDIAMIX_DISP_DATA12** SAI3_TX_BCLK PDM_BIT_STREAM02	GPIO2[16]	

PIN	Type	QS Standard	i.MX91 Pad Name	Alternate functions	GPIO	Description (refer to i.MX 91 manuals for details)
67	3V3	**LCD_G5**	GPIO_IO17	FLEXIO1_FLEXIO17 LPUART3_RTS_B LPUART4_RTS_B LPSPI4_PCS1 MEDIAMIX_CAM_DATA08 **MEDIAMIX_DISP_DATA13** SAI3_MCLK	GPIO2[17]	
68	3V3	**LCD_G6**	GPIO_IO18	SAI3_RX_BCLK MEDIAMIX_CAM_DATA09 **MEDIAMIX_DISP_DATA14** LPSPI5_PCS0 LPSPI4_PCS0 TPM5_CH2 FLEXIO1_FLEXIO18	GPIO2[18]	
69	3V3	**LCD_G7**	GPIO_IO19	SAI3_RX_SYNC PDM_BIT_STREAM03 **MEDIAMIX_DISP_DATA15** LPSPI5_SIN LPSPI4_SIN TPM6_CH2, SAI3_TX_DATA00	GPIO2[19]	
70	3V3	**LCD_B1**	GPIO_IO05	FLEXIO1_FLEXIO05 LPUART6_RX LPSPI7_SIN TPM4_CH0 **MEDIAMIX_DISP_DATA01** LPI2C6_SCL PDM_BIT_STREAM00	GPIO2[5]	
71	3V3	**LCD_B2**	GPIO_IO06	FLEXIO1_FLEXIO06 LPUART6_CTS_B LPSPI7_SOUT TPM5_CH0 **MEDIAMIX_DISP_DATA02** LPI2C7_SDA PDM_BIT_STREAM01	GPIO2[6]	
72	3V3	**LCD_B3**	GPIO_IO07	FLEXIO1_FLEXIO07 LPUART6_RTS_B LPSPI3_PCS1 LPSPI7_SCK MEDIAMIX_CAM_DATA01 **MEDIAMIX_DISP_DATA03** LPI2C7_SCL	GPIO2[7]	
73	3V3	**LCD_B4**	GPIO_IO08	LPSPI3_PCS0 MEDIAMIX_CAM_DATA02 **MEDIAMIX_DISP_DATA04** TPM6_CH0 LPUART7_TX LPI2C7_SDA, FLEXIO1_FLEXIO08	GPIO2[8]	
74	3V3	**LCD_B5**	GPIO_IO09	LPSPI3_SIN MEDIAMIX_CAM_DATA03 **MEDIAMIX_DISP_DATA05** TPM3_EXTCLK LPUART7_RX LPI2C7_SCL FLEXIO1_FLEXIO09	GPIO2[9]	
75	3V3	**LCD_B6**	GPIO_IO10	LPSPI3_SOUT MEDIAMIX_CAM_DATA04 **MEDIAMIX_DISP_DATA06** TPM4_EXTCLK LPUART7_CTS_B LPI2C8_SDA FLEXIO1_FLEXIO10	GPIO2[10]	
76	3V3	**LCD_B7**	GPIO_IO11	LPSPI3_SCK MEDIAMIX_CAM_DATA05 **MEDIAMIX_DISP_DATA07** TPM5_EXTCLK LPUART7_RTS_B LPI2C8_SCL FLEXIO1_FLEXIO11	GPIO2[11]	
Display Control						
77	3V3	**LCD_EN**	ENET2_RD1	ENET2_RGMII_RD1 SPDIF_IN SAI2_TX_DATA03 FLEXIO2_FLEXIO25	GPIO4[25]	
78	3V3	**LCD_BL**	UART1_TXD	LPUART1_TX S400_UART_TX LPSPI2_PCS0 **TPM1_CH1**	GPIO1[5]	PWM Output

PIN	Type	QS Standard	i.MX91 Pad Name	Alternate functions	GPIO	Description (refer to i.MX 91 manuals for details)
MISC						
79	3V3	LCD_R0	GPIO_IO20	SAI3_RX_DATA00 PDM_BIT_STREAM00 **MEDIAMIX_DISP_DATA16** LPSPI5_SOUT LPSPI4_SOUT, TPM3_CH1 FLEXIO1_FLEXIO20	GPIO2[20]	
80	3V3	LCD_G0	ENET2_RD2	ENET2_RGMII_RD2 LPUART4_CTS_B, SAI2_MCLK MQS2_RIGHT, FLEXIO2_FLEXIO26	GPIO4[26]	
81	3V3	LCD_G1	ENET2_RD3	ENET2_RGMII_RD3 SPDIF_OUT, SPDIF_IN MQS2_LEFT, FLEXIO2_FLEXIO27	GPIO4[27]	
82	3V3	LCD_B0	GPIO_IO04	TPM3_CH0, PDM_CLK **MEDIAMIX_DISP_DATA00** LPSPI7_PCS0, LPUART6_TX LPI2C6_SDA, FLEXIO1_FLEXIO04	GPIO2[4]	
Tamper & Analog						
83			ADC_IN0			
84			ADC_IN1			
85			ADC_IN2			
86			ADC_IN3			
87			TAMPER0			
88			TAMPER1			
UART						
89	3V3	UARTA_RXD	ENET2_RD0	ENET2_RGMII_RD0 **LPUART4_RX** SAI2_TX_DATA02 FLEXIO2_FLEXIO24	GPIO4[24]	1st application UART Receive Data input signal
90	3V3	UARTA_TXD	ENET2_TD0	ENET2_RGMII_TD0 **LPUART4_TX** SAI2_RX_DATA03 FLEXIO2_FLEXIO19	GPIO4[19]	1st application UART Transmit Data output signal
91	3V3	UARTB_RXD	GPIO_IO13	FLEXIO1_FLEXIO13 **LPUART8_RX** LPSPI8_SIN TPM4_CH2 MEDIAMIX_DISP_DATA09 LPI2C8_SCL PDM_BIT_STREAM03	GPIO2[13]	2nd application UART Receive Data input signal
92	3V3	UARTB_TXD	GPIO_IO12	**LPUART8_TX** LPSPI8_PCS0 TPM3_CH2 MEDIAMIX_DISP_DATA08 SAI3_RX_SYNC LPI2C8_SDA PDM_BIT_STREAM02	GPIO2[12]	2nd application UART Transmit Data output signal
93	3V3	UARTC_RXD	DAP_TDI	FLEXIO2_FLEXIO30 **LPUART5_RX** CAN2_TX MQS2_LEFT JTAG_MUX_TDI	GPIO3[28]	3rd application UART Receive Data input signal
94	3V3	UARTC_TXD	DAP_TDO_TRACESWO	FLEXIO1_FLEXIO31 **LPUART5_TX** CAN2_RX MQS2_RIGHT JTAG_MUX_TDO	GPIO3[31]	3rd application UART Transmit Data output signal
95	3V3	UARTC_CTS	DAP_TCLK_SWCLK	FLEXIO1_FLEXIO30 **LPUART5_CTS_B** JTAG_MUX_TCK	GPIO3[30]	3rd application UART Clear to Send **input** signal
96	3V3	UARTC_RTS	DAP_TMS_SWDIO	FLEXIO2_FLEXIO31 **LPUART5_RTS_B** JTAG_MUX_TMS	GPIO3[29]	3rd application UART Request to Send **output** signal

PIN	Type	QS Standard	i.MX91 Pad Name	Alternate functions	GPIO	Description (refer to i.MX 91 manuals for details)
2nd SPI						
97	3V3	SPIB_NSS	PDM_BIT_STREAM1	**LPSPI2_PCS1** TPM2_EXTCLK PDM_BIT_STREAM01 CCMSRCGPCMIX_EXT_CLK1 LPTMR1_ALT3 NMI_GLUE_NMI	GPIO1[10]	
98	3V3	SPIB_MISO	UART1_RXD	LPUART1_RX, S400_UART_RX **LPSPI2_SIN**, TPM1_CH0	GPIO1[4]	
99	3V3	SPIB_MOSI	UART2_RXD	LPUART2_RX LPUART1_CTS_B **LPSPI2_SOUT** TPM1_CH2 SAI1_MCLK	GPIO1[6]	
100	3V3	SPIB_SCK	UART2_TXD	LPUART2_TX, LPUART1_RTS_B **LPSPI2_SCK**, TPM1_CH3	GPIO1[7]	