Evaluating the ADL5961 9 kHz to 26.5 GHz, Integrated Vector Network Analyzer Front End

FEATURES

- Full featured evaluation board for the ADL5961
- Integrated bidirectional bridge measures forward-coupled and reverse-coupled signal

EQUIPMENT NEEDED

- Power supply
- One or two RF signal generators
- Spectrum analyzer or oscilloscope
- DC2026C (Linduino One) board (included in the ADL5961-KIT-EVALZ kit)
- Experimental impedances such as open, short, and load

ADL5961-EVALZ BOARD PHOTOGRAPH

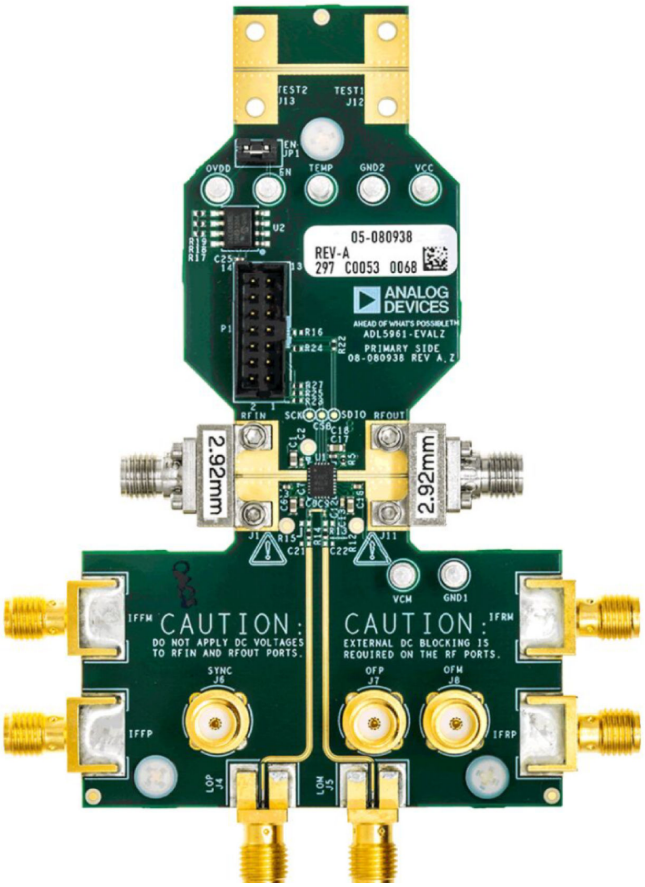

Figure 1. Evaluation Board Photograph

GENERAL DESCRIPTION

The ADL5961-EVALZ allows evaluation of the ADL5961 vector network analyzer (VNA) front-end IC.

The ADL5961 with integrated bridge derives inline incident and reflected power samples at up to 26.5 GHz, while maintaining low insertion loss, approximately 1 dB to 2 dB depending on frequency. Integrated mixers downconvert the incident and reflected samples to IF while preserving phase information. The serial peripheral interface (SPI) port provides access to programmable local oscillator (LO) and offset mixer versatility features, plus programmable IF gain and bandwidth.

For optimal performance, the printed circuit board (PCB) RF transmission lines are 50 Ω-controlled impedance on Rogers RO3003 low loss substrate material.

For full details on the ADL5961, see the ADL5961 data sheet, which must be consulted in conjunction with this user guide when using the ADL5961-EVALZ.

TABLE OF CONTENTS

REVISION HISTORY

10/2024—Revision 0: Initial Version

EVALUATION BOARD TEST SETUP

The ADL5961-EVALZ requires a 5 V power supply with a recommended minimum current rating of 500 mA.

An external 3.3 V for OVDD is not needed because this voltage is supplied by the DC2026C Linduino One board.

The RFIN port requires an RF signal generator capable of operating at up to 26.5 GHz for the full frequency range.

The RFOUT port can be connected to the spectrum analyzer or various impedance standards for demonstration, device calibration, or evaluation of the insertion loss and directivity of the ADL5961.

The LO input port is differential via the LOP and LOM pins. The LO drive also functions well when simply driven single-ended, with the unused side terminated with 50 Ω Subminiture Version A (SMA) termination.

IF outputs are differential, via the IFFP and IFFM pins (forward channel) and the IFRP and IFRM pins (reverse channel), for forward and reverse paths, respectively. All IF outputs are AC-coupled, 50 Ω source impedance, and the outputs can be directly connected to a 50 Ω spectrum analyzer or oscilloscope for single-ended or differential measurement. Unused IF outputs can be either left open or terminated with 50 Ω.

The **ADL5960 Evaluation Software** graphical user interface (GUI) can be used for ADL5961 test and demonstration purposes. This software is available for download at www.analog.com/EVAL-ADL5960 and runs on the Microsoft Windows environment. If not already installed, this GUI must be downloaded and installed before proceeding further. Installing the GUI also installs the USB drivers necessary to support the DC2026C Linduino One hardware. Be sure to install the GUI before connecting the USB of the DC2026C Linduino One board to the PC.

A DC2026C Linduino One is shipped with the ADL5961-KIT-EVALZ kit. The DC2026C Linduino One board has custom firmware preinstalled to support the **ADL5960 Evaluation Software** GUI. The custom firmware installation is signified by an ADL5961 label adhered to the DC2026C Linduino One board, on the outer shell of the USB receptacle.

A 14-conductor ribbon cable provides SPI and regulated 3.3 V connections between the DC2026C Linduino One board and the ADL5961-EVALZ board. The 3.3 V from the DC2026C Linduino One powers the ADL5961 OVDD pin, thus powering the ADL5961 on-chip digital interface. Without this power source, the ADL5961 is not enabled and it is not functional.

An RF test trace is provided near the top edge of the ADL5961-EVALZ. This transmission line is provided for de-embedding purposes, having the same cross sectional dimensions as the RFIN and RFOUT printed transmission lines. The RF test trace connectors are not normally supplied but can be taken from the RFIN and RFOUT locations for test purposes or purchased separately.

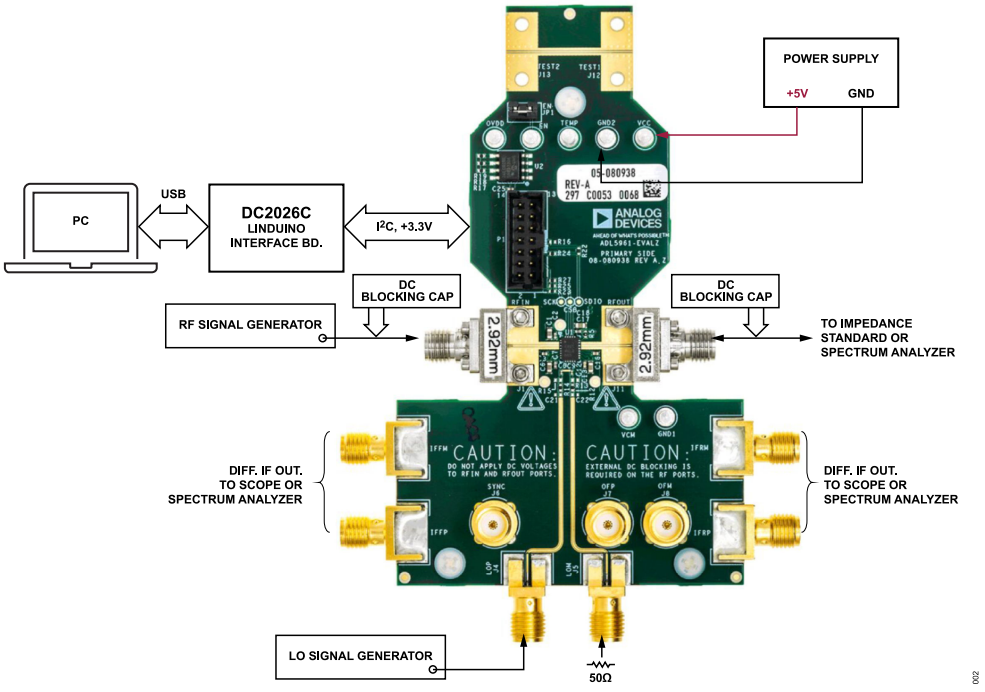

Figure 2. ADL5961-EVALZ Basic Test Setup

TEST PROCEDURE

Test setup begins with basic preparation and a power-up sequence that establishes SPI communications. See the Preparations for Testing section and Power-Up Sequence section for additional details. After setup, see the RF Functional Demonstration section for a functional demonstration procedure.

PREPARATIONS FOR TESTING

To prepare the ADL5961-EVALZ for testing, take the following steps:

1. Confirm that the ADL5961-EVALZ is not connected to the 14-pin ribbon cable. It is important to always turn on the 5 V DC power supply to the ADL5961-EVALZ under test before connecting the ribbon cable.
2. Confirm the DC2026C Linduino One board has the correct firmware installed (as confirmed by the ADL5961-EVALZ label affixed to the DC2026C Linduino One board).
3. On the DC2026C Linduino One board, verify that VCCIO is set to 3.3 V, which is its normal configuration. See Figure 3.

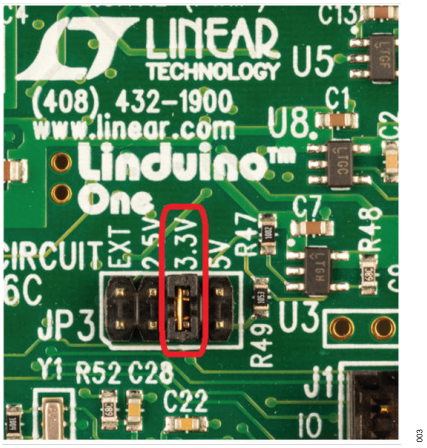

Figure 3. Confirm Linduino 3.3 V, Input and Output Voltage Setting

4. Ensure that the EN jumper on the ADL5961-EVALZ is installed, which is the default setup when the ADL5961-EVALZ ships. This jumper is seen at the top of the ADL5961-EVALZ near the RF test trace.
5. Set up the 5 V power supply for at least 300 mA of current capability. First, turn the power source off. Then, connect the 5 V power supply and a ground return path to the VCC turret.
6. Ensure that the **ADL5960 Evaluation Software** GUI has been downloaded and installed on the PC. If not, download the software from www.analog.com/EVAL-ADL5960.

POWER-UP SEQUENCE

To prevent the ADL5961-EVALZ damage, the following power-up sequence is required:

1. Apply 5 V of power to VCC on the ADL5961-EVALZ.
2. Connect the USB cable from the DC2026C Linduino One to the PC. Wait for the light-emitting diodes (LEDs) to stop blinking. When the LEDs stop blinking, the ADL5961 is enabled. The 5 V power nominally consumes approximately 120 mA of current.
3. Connect the DC2026C Linduino One board to the ADL5961-EVALZ using the supplied 14-pin ribbon cable.
4. Launch the **ADL5961 Evaluation Software** GUI on the PC.

The **ADL5960 Evaluation Software** GUI **Connection** tab shows that the PC automatically discovers the DC2026C Linduino One (see Figure 4). Click **Connect** to connect to the ADL5961 IC under test. The **Main Controls** tab opens, which shows the register settings that can be changed (see Figure 5).

To power down the test setup, follow the power-up sequence in reverse:

1. Close the **ADL5960 Evaluation Software** GUI.
2. Disconnect the USB cable, and the ADL5961 then becomes disabled.
3. Turn off or disconnect the 5 V power source.

TEST PROCEDURE

RF FUNCTIONAL DEMONSTRATION

The most fundamental ADL5961 demonstration occurs when an LO is supplied externally at a frequency offset by the desired IF output frequency, as follows:

1. Connect an RF signal generator to drive the RF port. Set the power level to 10 dBm and the frequency to 1 GHz.
2. Connect a second RF signal generator to the LO port. The unused differential LO port must be terminated with a 50 Ω SMA termination. Set the LO drive power to 0 dBm, and the frequency to 1.01 GHz.
3. Leave the RFOUT port unconnected.
4. Connect both IF port outputs to an oscilloscope. If only a 2-channel oscilloscope is available, drive each oscilloscope channel single-ended with the downconverted IF incident and reflected signals. If the oscilloscope has four channels, connect all four IF output connectors to the oscilloscope and configure the oscilloscope to display two differential signals, incident and reflected.
5. Downconverted incident and reflected output signals can be observed on the oscilloscope at the difference frequency, 10 MHz. Increasing the IF gain register settings to approximately 20 dB typically result in a higher signal-to-noise ratio at the IF outputs without overdrive problems.
6. With the RFOUT port remaining unconnected (open), observe that there are large signals at both incident and reflected IF output ports. The reflected IF port signal is expected to be slightly lower than the incident port signal because of the insertion loss of the ADL5961.
7. Install an RF short onto the RFOUT port. Observe that the IF incident and the reflected port magnitudes remain relatively constant; however, the phase of the reflected IF port signal flips 180° compared to the prior RFOUT = open test condition.
8. Connect a 50 Ω SMA RF load (termination) to the RFOUT port. Observe that the IF incident port magnitude remains relatively constant, while the IF reflected port magnitude drops by a large amount, typically 30 dB, which is the approximate directivity specification of the ADL5961 at 1 GHz. Note that the external SMA 50 Ω load termination on RFOUT must be accurate and wide band for this test. This measurement is never better than the directivity of the ADL5961 or the return loss performance of the 50 Ω termination on RFOUT.

ADL5960 EVALUATION SOFTWARE APPLICATION GUI

Figure 4 shows the **Connection** tab of the **ADL5960 Evaluation Software** GUI, and Figure 5 shows the Main Controls table of the **ADL5960 Evaluation Software** GUI, which can also be used to evaluate the ADL5961-EVALZ.

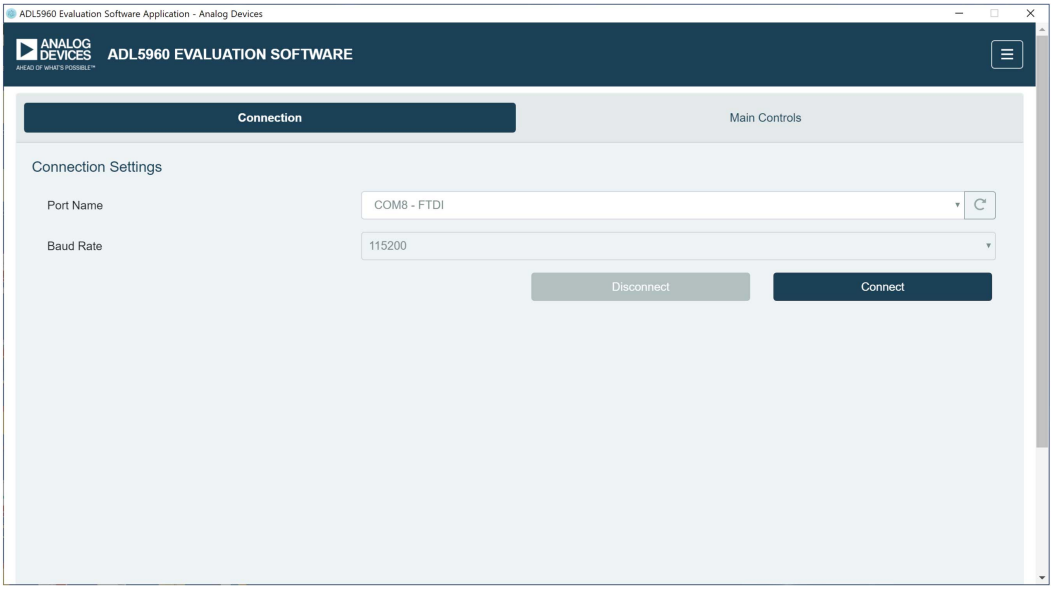

Figure 4. Connection Tab

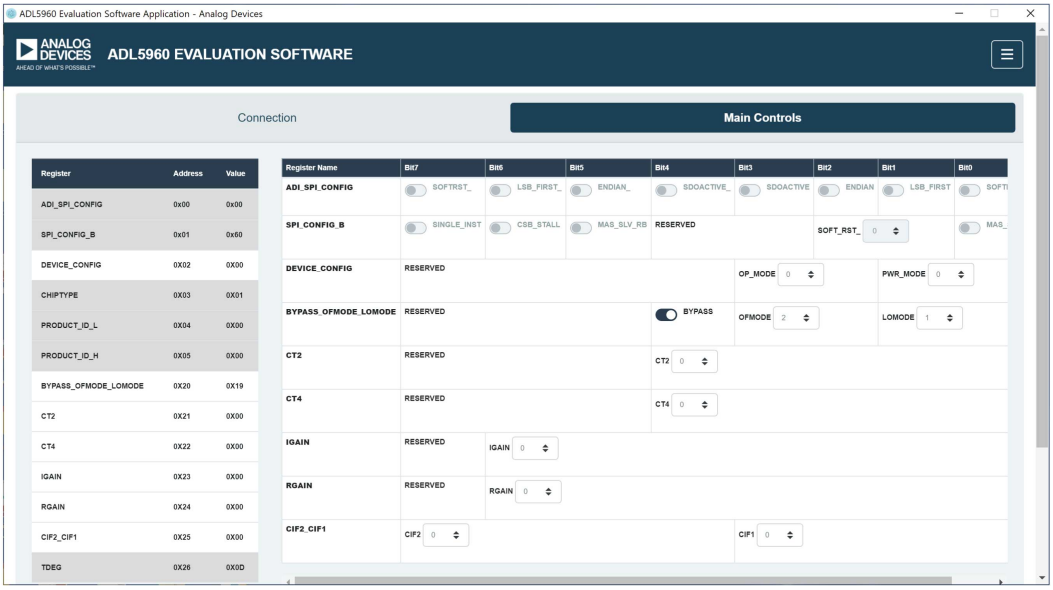

Figure 5. Main Controls Tab

ADL5960 EVALUATION SOFTWARE APPLICATION GUI

QUICK REFERENCE

For full and complete information on the ADL5961, consult the ADL5961 data sheet.

Table 1. ADL5961 Register Quick Reference

Bit Name	Description
BYPASS	When asserted, these bits set the LO path to bypass the LO multipliers or dividers. OFMODE and LOMODE have no effect. When these bits are de-asserted, the LO path is via the selected LO multiplier or divider.
OFMODE	Configures the offset input dividers.
LOMODE	Configures the LO path multipliers and dividers.
CT2, CT4	CT2 and CT4 configure the LO chain ×2 and the ×4 filter frequency settings, respectively.
IGAIN, RGAIN	IGAIN and RGAIN configure the forward and reverse path IF gain settings, respectively.
CIF1, CIF2	CIF1 and CIF2 configure the first and second IF filter stage settings, respectively.
PWR_MODE	Mode 2 and Mode 3 disable the device.

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.