2A Bidirectional Power Backup Supply

FEATURES

- **Bidirectional Synchronous Boost Capacitor Charger/Buck Regulator for System Backup**
- **Wide Input Voltage Range: 3V to 17V**
- **Up to 40V Capacitor Voltage Storage for High Energy Backup**
- **2A Maximum CAP Charge Current**
- Integrated Power N-Channel MOSFETs (150mΩ Top and 75mΩ Bottom)
- Integrated Power N-Channel MOSFET for Output/CAP Disconnect (50mΩ)
- Input Current Limit During Charging
- Fast 1MHz Switching Frequency
- ±1% Reference Accuracy for System Voltage Regulation
- Indicator Outputs for Charge Status and Input Power Fail
- Low Profile 24-lead 3mm × 5mm QFN Package

APPLICATIONS

- Backup Capacitor Systems
- Power Failure Backup Systems
- Solid-State Drives
- Automotive

DESCRIPTION

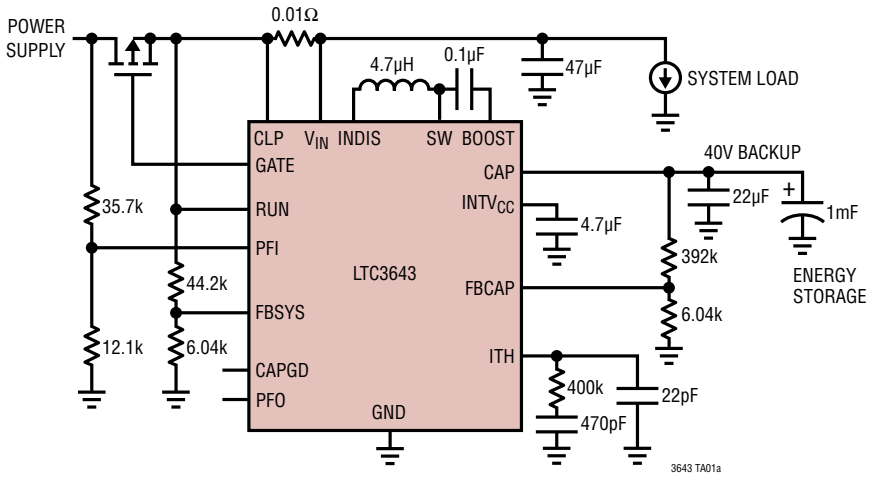
The LTC®3643 is a bidirectional synchronous step-up charger and step-down converter which efficiently charges a capacitor array up to 40V from an input supply between 3V to 17V. When the input supply falls below the programmable power-fail threshold, the step-up charger operates in reverse as a synchronous step-down regulator to power the system rail from the backup capacitor during this power interruption/failure condition.

When charging the backup capacitor, an external low-value sense resistor may be used to maintain an accurate current limit from the input supply or implement PowerPath™ functionality.

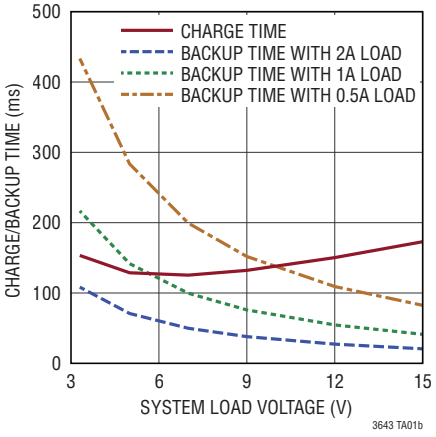
The step-down converter operates at a 1MHz switching frequency, allowing small external components to be used. Low quiescent current during regulation maximizes the energy usage from the backup capacitor.

TYPICAL APPLICATION

40V Backup System Regulating System Supply to 5V



Approximate Charge/Backup Time per 1mF of Storage Cap (40V Backup)

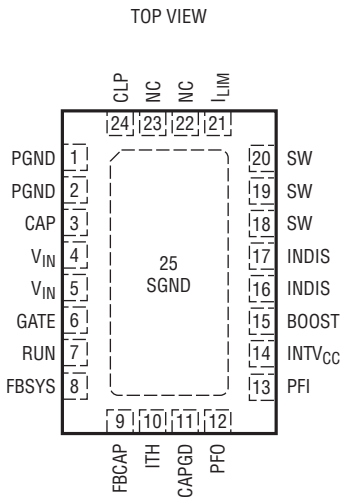


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} ..... –0.3V to 17V
RUN ..... –0.3V to V_{IN}+0.3V
CLP ..... –0.3V to 17V
CAP ..... –0.3V to 42V
BOOST-SW ..... –0.3V to 4V
$INTV_{CC}$, FBSYS, FBCAP ..... –0.3V to 4V
PFI ..... –0.3V to 4V
I_{LIM} ..... –0.3V to V_{INTVCC}+0.3V
PFO, CAPGD ..... –0.3V to 6V
Operating Junction Temperature Range
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10sec) ..... 260°C

PIN CONFIGURATION



UDD PACKAGE
24-LEAD (3mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 46°C/W, θ_{JC} = 5.0°C/W
EXPOSED PAD (PIN 25) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3643EUDD#PBF	LTC3643EUDD#TRPBF	LGSX	24-Lead (3mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3643IUDD#PBF	LTC3643IUDD#TRPBF	LGSX	24-Lead (3mm × 5mm) Plastic QFN	–40°C to 125°C
AUTOMOTIVE PRODUCTS**				
LTC3643IUDD#WPBF	LTC3643IUDD#WTRPBF	LGSX	24-Lead (3mm × 5mm) Plastic QFN	–40°C to 125°C

Contact Analog Devices for parts specified with wider operating temperature ranges.

*The temperature grade is identified by a label on the shipping container.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

For more information on lead-free part marking, go to: www.analog.com/leadfree.
For more information on tape-and-reel specifications, go to: www.analog.com/tapeandreel. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 5V, V_{RUN} = 2V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Voltage	V_{IN} CAP		3.0		17 40	V V
I_{Q-IN}	Input Quiescent Current	Active Mode Burst Mode® Operation Shutdown Mode; RUN = 0V			800 400 10	 800 20	µA µA µA
$R_{DS(ON)}$	Switch A On Resistance Switch B On Resistance Switch C On Resistance	V_{CAP} >= V_{IN} V_{INTVCC} = 3.3V V_{BOOST} = 8.3V			50 75 150		mΩ mΩ mΩ
I_{SW}	Top Switch Leakage Bottom Switch Leakage	V_{CAP} = 40V, V_{SW} = 0 V_{CAP} = V_{SW} = 40V			0.1 0.1	1 1	µA µA
Boost Charger Regulation							
V_{CAP}	Cap Voltage					40	V
V_{FBCAP}	Regulated Output Feedback Voltage		●	0.594	0.6	0.606	V
I_{FBCAP}	FBCAP Input Current					±10	nA
g_m(EA)	Error Amplifier Transconductance	ITH = 1.2V		210	270	330	µS
$I_{LIM-BOOST}$	Peak Inductor Current Limit (Bottom Switch Peak Limit)		 ●	3.0 2.8	3.2	3.4	A A
$t_{OFF(MIN)-BOOST}$	Minimum Off-Time				70		ns
f_{SW}	Switching Frequency				1		MHz
	Input Current Limit Amplifier Regulated Voltage	$V_{CLP-VIN}$	 ●	48.5 46	50 50	51.5 54	mV mV
Buck Regulator Voltage Regulation							
V_{FBSYS}	Regulated System Feedback Voltage		●	0.594	0.6	0.606	V
I_{FBSYS}	FBSYS Input Current					±10	nA
$I_{LIM-BUCK}$	Valley Inductor Current Limit (Bottom Switch Valley Limit)	I_{LIM} = FLOAT I_{LIM} = 0V I_{LIM} = V_{INTVCC}	 ● ● ●	 2.0 2.9 3.8	2.6 3.7 4.7	3.2 4.5 5.6	A A A A A A
$t_{ON(MIN)-BUCK}$	Minimum On-Time				30		ns
$INTV_{CC}$ Regulator							
	$INTV_{CC}$ Regulated Voltage			3.0	3.2	3.4	V
	$INTV_{CC}$ UVLO	$INTV_{CC}$ Rising		2.6	2.75	2.9	V
I/O Pins							
V_{RUN}	RUN High Rising RUN Hysteresis		●	1.12	1.2 100	1.28	V mV
	RUN Input Current	V_{RUN} = 12V, V_{IN} = 12V			0	±10	nA
V_{PFI}	PFI Input Threshold	Falling Rising (100mV hysteresis)	● ●	0.95 1.05	1.0 1.1	1.05 1.15	V V
	PFI Delay Time	Falling Rising			3 20	6 40	µs µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 5V, V_{RUN} = 2V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	GATE Turn-on Time	To CLP-GATE > 2.5V, C_{GATE} = 1nF			70	100	µs
	GATE Turn-off Time	To CLP-GATE < 1V, C_{GATE} = 1nF			3	6	µs
	GATE Pull-Down Current		●	45	70	95	µA
	CAPGD Threshold	FBCAP Rising Hysteresis		550	570 15	590	mV mV
	CAPGD Resistance				170	250	Ω
	/PFO Resistance				170	250	Ω

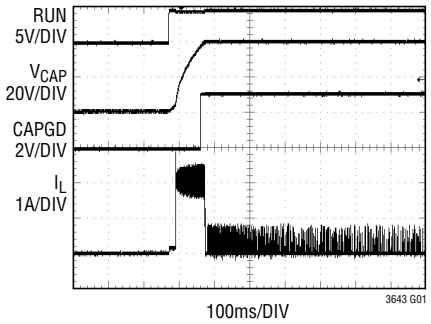
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. The LTC3643 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3643E is guaranteed to meet specified performance from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3643I is guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

T_J is calculated from the ambient T_A and power dissipation P_D according to the following formula: $T_J = T_A + (P_D \bullet \theta_{JA})$.

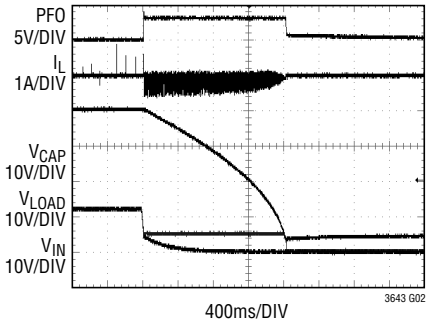
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Step-Up Charging Waveform



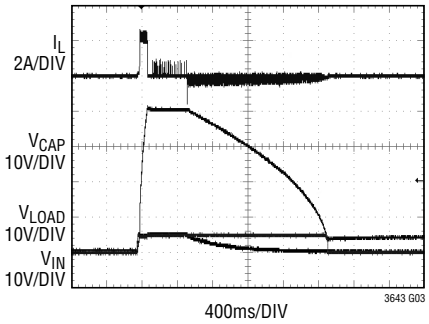
V_{IN} = 5V
V_{CAP} = 40V
NO LOAD
START-UP FROM RUN

Step-Down Discharge Waveform



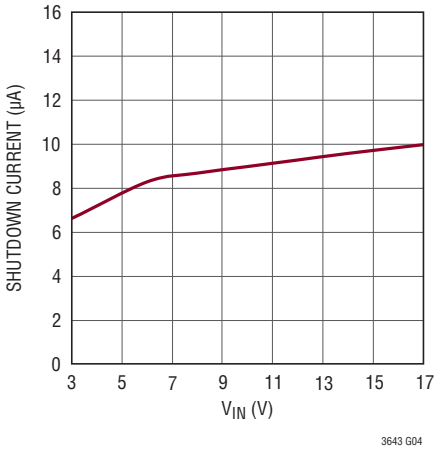
V_{IN} = 12V
V_{CAP} = 40V
V_{LOAD} = 5V
I_{LOAD} = 100mA

Step-Up to Step-Down Handoff Waveform

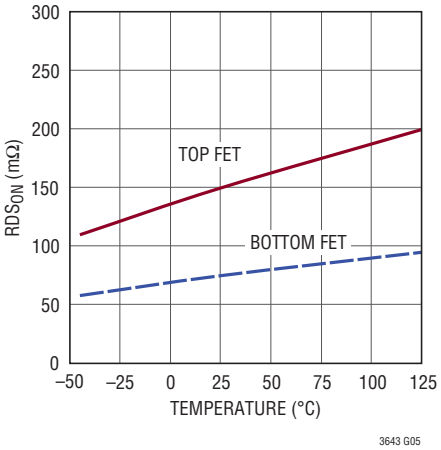


V_{IN} = 5V
V_{CAP} = 40V
V_{LOAD} = 5V, (SYSTEM LOAD)
I_{LOAD} = 100mA

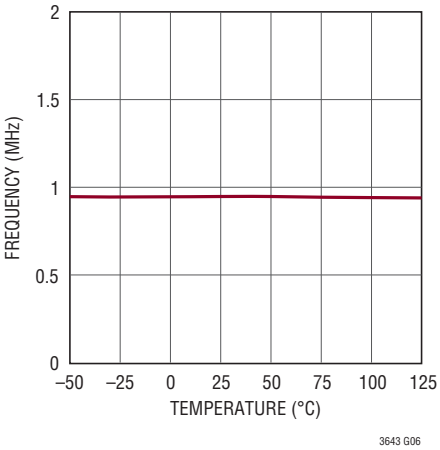
Shutdown Current vs V_{IN}



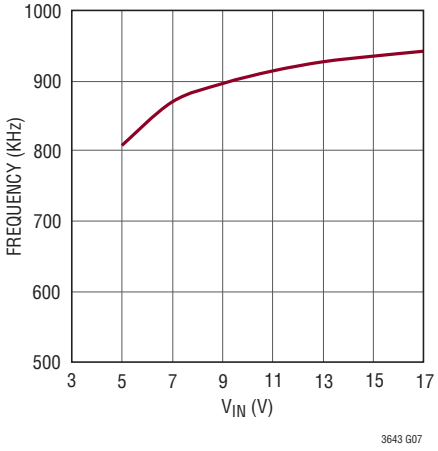
$R_{DS(ON)}$ vs Temperature



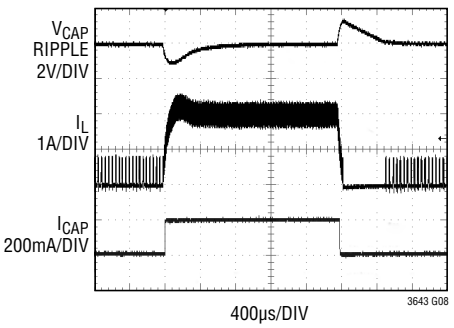
Frequency vs Temperature



Frequency vs V_{IN}

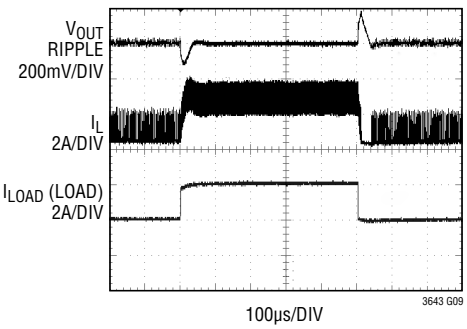


Step-Up Regulator Transient Response



V_{IN} = 5V
V_{CAP} = 40V
I_{CAP} = 14mA TO 200mA
L = 7.2µH
C_{OUT} = 47µF

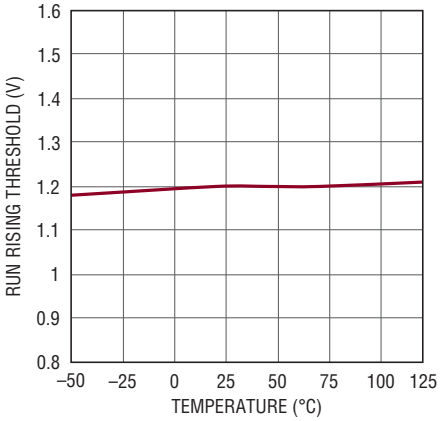
Step-Down Regulator Transient Response



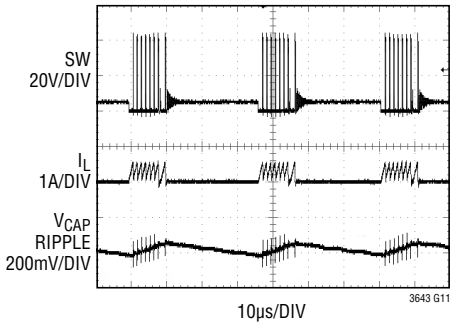
V_{CAP} = 40V
V_{LOAD} = 5V
L = 2.2µH
I_{LOAD} = 400mA TO 2.4A (SYSTEM LOAD)

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Run Rising Threshold vs Temperature

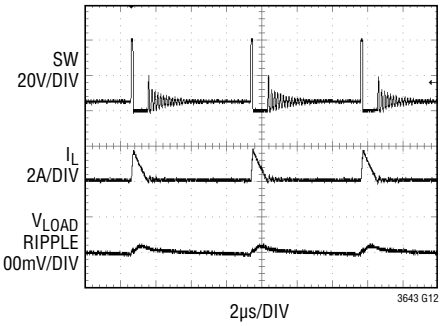


Step-Up Regulator Light Load Switching Waveform



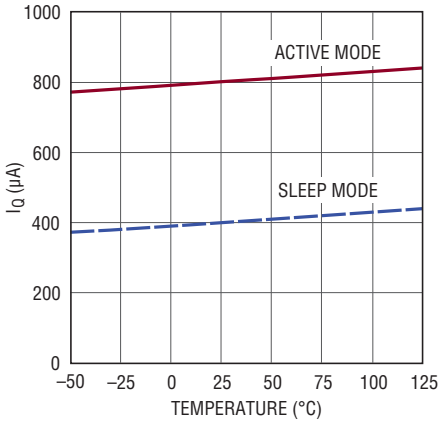
V_{IN} = 5V
V_{CAP} = 40V
I_{LOAD} (CAP) = 14mA
C_{CAP} = 40µF
L = 7.2µH

Step-Down Regulator Light Load Switching Waveform

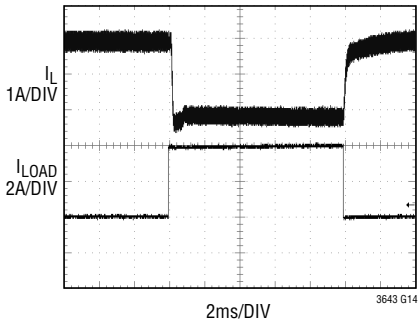


V_{CAP} = 40V
V_{LOAD} = 5V
V_{IN} = 4.5V
I_{LOAD} (LOAD) = 110mA
L = 2.2µH

Quiescent Current vs Temperature

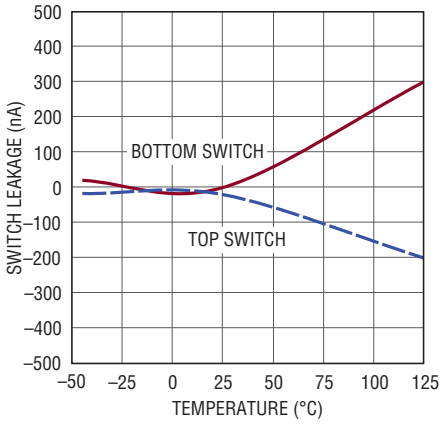


Charging Waveform with Programmed Current Limit

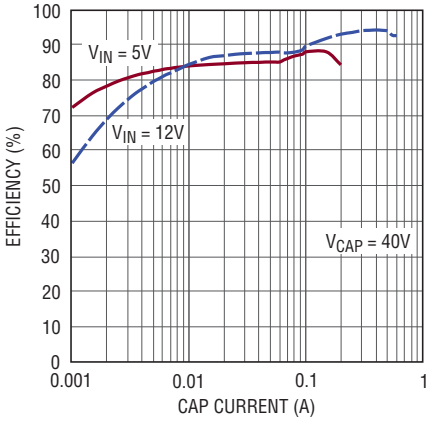


R_{SENSE} = 10mΩ

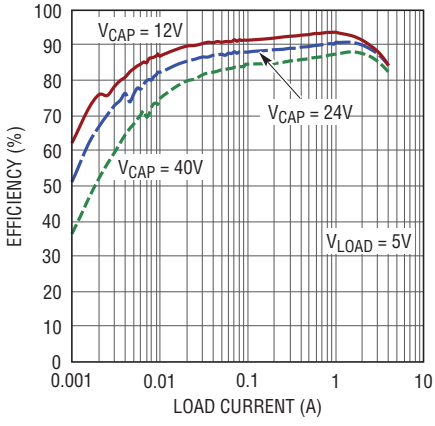
Switch Leakage Current vs Temperature



Step-Up Regulator Efficiency vs Cap Current



Step-Down Regulator Efficiency vs Load



PIN FUNCTIONS

PGND (Pins 1-2): Ground Pins for the Power Switch.

CAP (Pin 3): Storage Capacitor Connection. This pin is the power input to the step-down regulator's main switch (boost regulator's synchronous switch) and connects directly to the backup energy storage capacitor.

V_{IN} (Pins 4-5): Input Supply of Boost Charger and Regulated Output Voltage of Step-Down Regulator. This input also powers the $INTV_{CC}$ LDO and input to the current regulation amplifier.

GATE (Pin 6): Gate Driver for PowerPath Switch. This pin drives the gate of an external PMOS switch that connects the main power supply to the system load. This output swings from V_{IN} to GND.

RUN (Pin 7): Logic Controlled RUN Input. Do not leave this pin floating. Place a resistor divider from V_{IN} to GND for an accurate V_{IN} Undervoltage threshold.

FBSYS (Pin 8): Feedback Input to Step-Down Regulator Control Loop. Connect a resistor divider tap to this pin. The V_{IN} voltage can be adjusted such that V_{IN} = 0.6V (1+R2/R1) (See Figure 4).

FBCAP (Pin 9): Feedback Input to the Error Amplifier of the Cap Voltage Regulation Loop. Connect a resistor divider tap to this pin. The CAP voltage can be adjusted such that V_{CAP} = 0.6V (1+R4/R3) (See Figure 5).

ITH (Pin 10): Error Amplifier Output and Switching Regulator Compensation Point for the Boost Regulator. The current comparator's trip threshold is linearly proportional to this voltage. The Buck Regulator's compensation is set internally by the part.

CAPGD (Pin 11): Capacitor Good Open Drain Status Output. This output is pulled down when the LTC3643 is charging the storage capacitor. It becomes high impedance when the output cap reaches 95% of the programmed charge voltage.

PFO (Pin 12): Power Fail Open Drain Status Output. This pin pulls down when the main supply voltage is above the threshold set by the PFI pin.

PFI (Pin 13): Power Fail Input. This pin sets the threshold at which the converter switches from boost charger mode to buck regulator mode. Connect with a resistor divider from the main power supply in order to switch to buck regulator mode when the supply voltage drops below a set threshold.

$INTV_{CC}$ (Pin 14): Low Dropout Regulator. Bypass with a low ESR capacitor of at least 1µF to ground.

BOOST (Pin 15): Boost Rail. Connect a 0.1µF capacitor between this pin and SW node to power the gate driver of the synchronous boost switch.

INDIS (Pins 16-17): Input Disconnect Pin. The Internal power switch that allows for Output Disconnect feature is placed between the V_{IN} and INDIS pins.

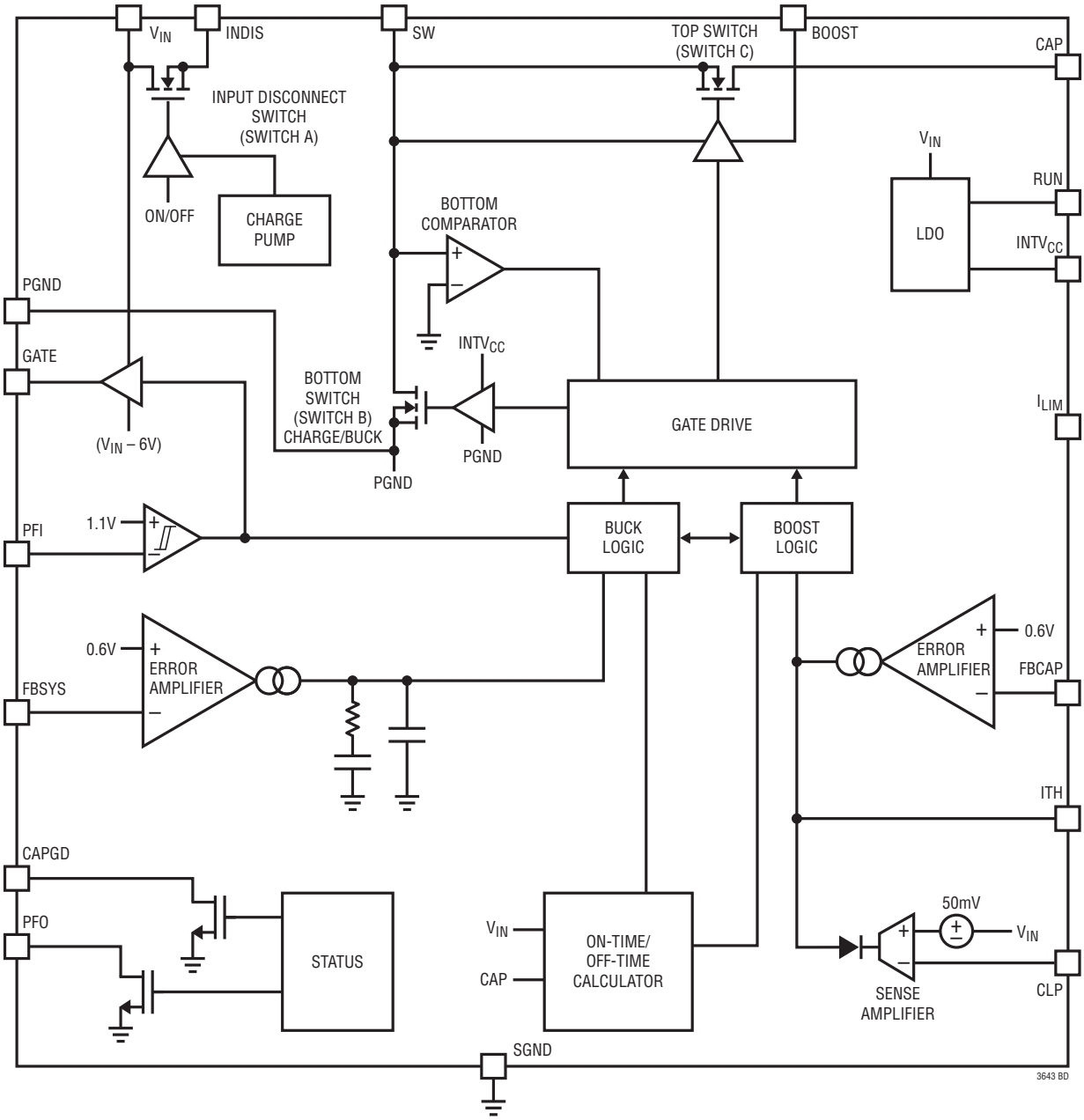
SW (Pins 18-20): Switch Node Connection to the Power Regulator.

I_{LIM} (Pin 21): Buck Mode Peak Current Program Pin. Leave this pin floating for 2A current limit, ground it for 3A current limit, and tie it to $INTV_{CC}$ for 4A current limit during buck mode.

CLP (Pin 24): Input to Current Regulation Amplifier. This pin is the inverting input to a current regulation amplifier that reduces the charging current when CLP rises more than 50mV above V_{IN}.

SGND (Exposed Pad Pin 25): Signal Ground Pin of the Regulator. Tie to PGND at a single point. Connect to PCB ground plane for rated thermal performance.

BLOCK DIAGRAM



OPERATION

The LTC3643 is a bidirectional regulator capable of delivering power from V_{IN} to CAP (storage capacitor) as well as from CAP back to V_{IN}, depending on the state of the PFI voltage.

When the PFI voltage is high, signifying that the power supply is good, power is delivered from V_{IN} to CAP as illustrated in Figure 1. In this mode, LTC3643 operates as a peak current mode constant off-time boost regulator with input disconnect. In this mode, power can be directly delivered from the power supply to the system load, and be used to charge the energy storage element on CAP.

When the PFI Voltage is low, signifying that the power supply is below the necessary threshold, power delivery is reversed, it operates as a valley current mode constant on-time buck regulator, and delivers power from CAP to power V_{IN} for as long as possible. The power path is illustrated in Figure 2.

The duration for which power can be held up at V_{IN} depends on the amount of system load, the size of the energy storage CAP, and the voltage at which the CAP node was charged to.

The LTC3643 operates with pseudo-constant frequency, which is set solely by the on-time/off-time, which is internally calculated based on the V_{IN} and CAP voltages and set to be 1MHz. Under light output load conditions, the LTC3643 operates in Burst Mode and skips pulses to minimize system power loss. As the output load current increases, the LTC3643 seamlessly transitions to continuous PWM switching to deliver output power. Though the LTC3643 can be configured to operate as a standalone boost regulator with input disconnect, it is primarily targeted at applications where a high voltage energy storage capacitor needs to be charged for the purposes of delivering power back to V_{IN} to maintain system regulation in “dying gasp” situations when the system supply is removed.

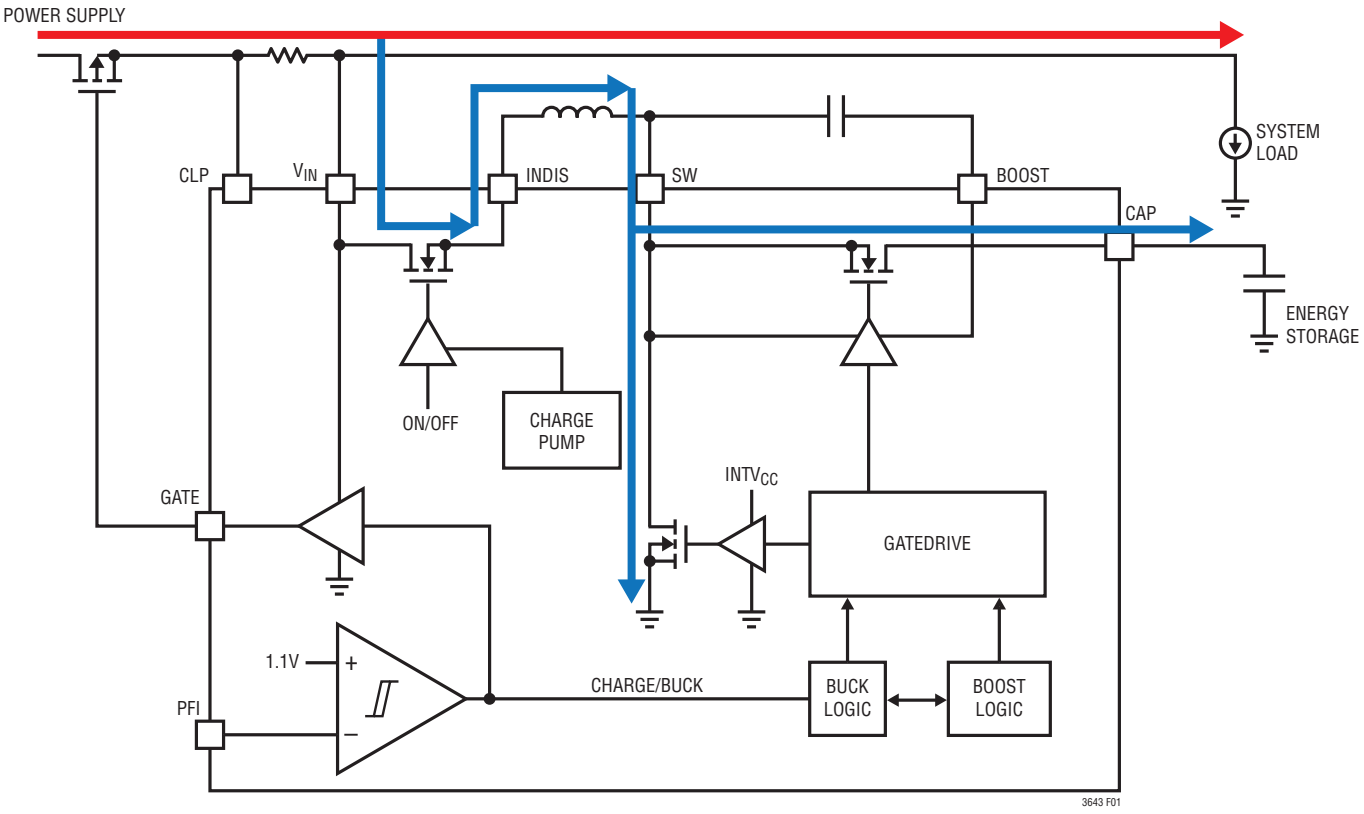


Figure 1. Power Path Block – Power Available from Power Source

OPERATION

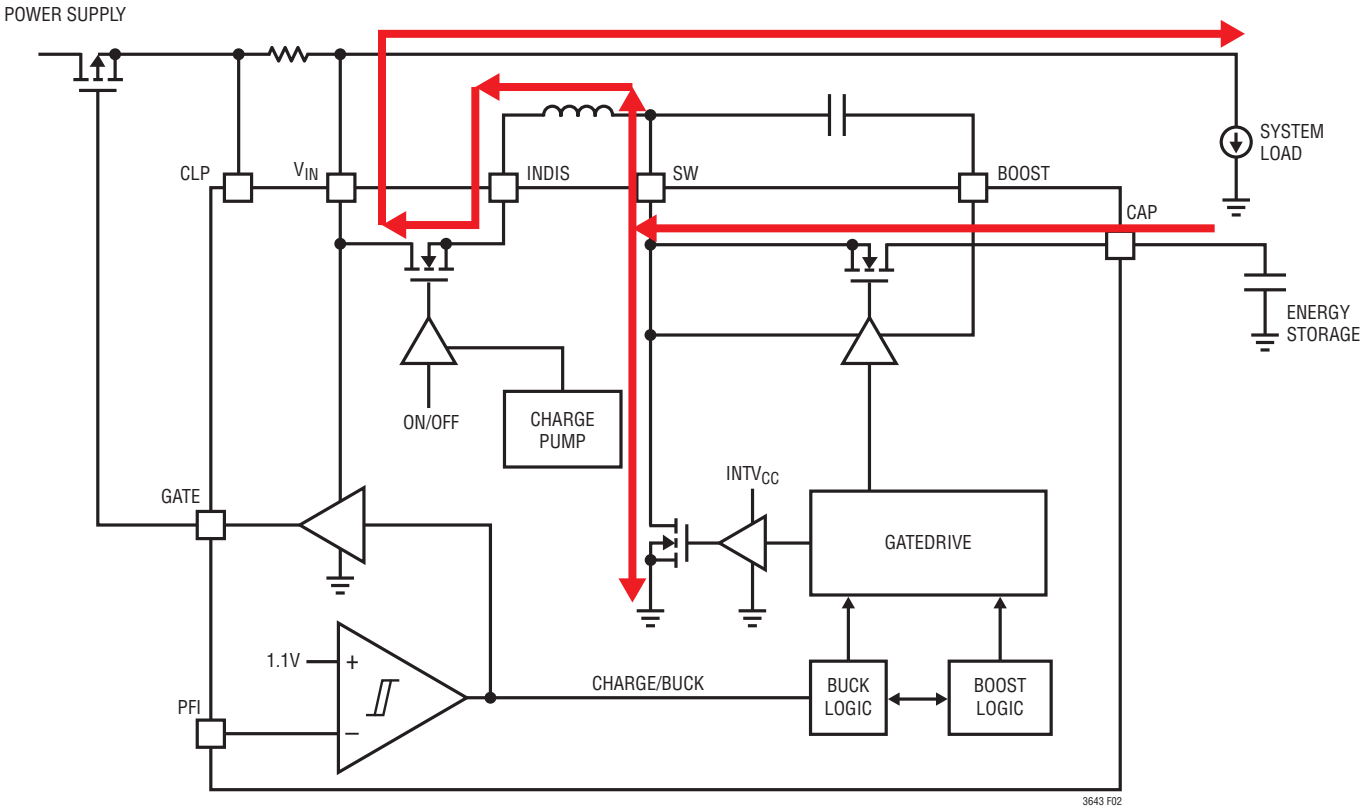


Figure 2. Power Path Block – Power Available from Energy Storage Element

Boost Mode Control Loop

When the PFI voltage is above 1.1V, the input power source is deemed to be good, and power will be delivered from V_{IN} to CAP. If there is sufficient load on CAP or if the CAP voltage has yet to reach its final programmed value, the step-up regulator will switch continuously to deliver the necessary power. Under these circumstances, the bottom switch will turn on, thus ramping up the current in the inductor. Once that current reaches a certain level, which is set by the I_{TH} voltage, the switch will turn off and allow the top (synchronous) switch to turn on. The top switch will remain on for a fixed duration (off-time) before shutting off to allow for the cycle to repeat.

The off-time is calculated such that in steady state, the regulator will operate at a frequency around 1MHz. Thus, the off-time is equal to:

$$t_{OFF-BOOST} = 1\mu s \bullet \frac{V_{IN}}{V_{CAP}}$$

The boost mode control loop is compensated through the external ITH pin, and the method of compensating the loop will be discussed in more detail in the applications information section.

Boost Mode Low Current Operation

Once the CAP voltage has reached its programmed voltage, and the load is minimal, the LTC3643 will automatically transition from continuous mode operation to Burst Mode operation. In this mode, the I_{TH} voltage will transition above and below the sleep threshold depending on the CAP voltage. If the CAP voltage decreases slightly below its regulation point, the regulator will wake up from sleep, and the bottom switch will turn on until the inductor current reaches the burst current clamp of 800mA. Once that value is reached, the bottom switch turns off and the top switch turns on for a fixed duration, $t_{OFF-BOOST}$. This switching cycle will repeat until the CAP has replenished enough to force the I_{TH} voltage below the sleep threshold. Once that happens, both switches are turned off and the quiescent current is decreased to 400µA.

OPERATION

Boost Mode Startup

The LTC3643 will begin to operate if the RUN voltage is raised above 1.2V and V_{IN} is greater than 3V. In order to prevent conduction from the V_{IN} to CAP through the body diode of the top switch, an input disconnect switch is placed between V_{IN} and INDIS. The body diode of the disconnect switch and that of the top switch are opposite in polarity in order to prevent conduction of current when CAP is less than V_{IN}. The gate of the disconnect switch remains grounded until the regulator begins to operate.

Once started, an internal charge pump will slowly charge up the gate of the disconnect switch and regulate that gate voltage such that only 100mA of current is flowing through the switch. That 100mA will thus conduct through the inductor between INDIS and SW, and the body diode of the top switch to charge up the capacitor at the CAP node. The 100mA limit is set as a way to limit the power dissipation through the disconnect switch and the top switch, and protect those switches from overheating. During this period, the voltage at INDIS and SW will be clamped at a diode above CAP.

Once the INDIS voltage approaches V_{IN}, and it is sensed that the internal disconnect switch is fully enhanced, an internal signal is issued to allow the top and bottom switches to operate as needed to charge the CAP voltage up to its programmed value.

Boost Output Over-Current/Short Operation

The current through the disconnect switch is constantly being monitored to resolve overcurrent situations. Once the switch is fully enhanced, if the current through the disconnect switch ever exceeds 4.8A, a signal is sent to the control circuitry to keep the top switch on indefinitely until that current level subsides.

During an output short situation, if the CAP voltage were to ever collapse below the V_{IN} voltage, then simply leaving the top switch on to discharge the inductor current would not work. In these situations, if the current through the disconnect switch ever exceeds 8A, the gate of the disconnect switch is immediately pulled down, thus effectively shutting off the disconnect switch. At the same time, both the top and bottom switches are shut off. The current in the inductor will then conduct through the body diode of the top switch and decrease down to 0A. From there, the internal charge pump will slowly charge back up the gate of the disconnect switch and regulate the current through the switch to 100mA, much like the case in startup.

Buck Mode Control Loop

If the PFI voltage falls below 1V, power will be delivered from CAP to V_{IN}. If the system load at V_{IN} is high enough, the regulator will switch continuously. In a typical cycle, the top switch is turned on for a fixed duration (on-time). Once that duration expires, the top switch turns off and the bottom switch is turned on; inductor current is allowed to discharge until a valley current level is reached, at a threshold set by an internally compensated I_{TH} voltage. Once that current level is reached, the bottom switch turns off and the top switch turns back on again and the cycle repeats.

The on-time is once again calculated such that in steady state, the regulator will operate at a frequency around 1MHz. Thus, the on-time is equal to:

$$t_{ON-BUCK} = 1\mu s \bullet \frac{V_{IN}}{V_{CAP}}$$

The buck mode control loop is compensated by an internal RC network and the external ITH pin is grounded through an internal switch.

Buck Mode Low Current Operation

When V_{IN} reaches the programmed regulation voltage and a minimal load is present, the regulator will automatically transition into Burst Mode operation. In this mode, the ITH voltage will transition above and below the sleep threshold depending on the V_{IN} voltage. If the V_{IN} voltage decreases slightly below its regulation point, the regulator will wake up from sleep, and the top switch will turn on for a fixed duration, $t_{ON-BUCK}$. Then, the top switch will turn off and the bottom switch will turn on until the inductor current reaches 0A. This switching cycle will repeat until the V_{IN} voltage has replenished enough to force the I_{TH} voltage below the sleep threshold. Once that happens, both switches are turned off and the quiescent current is decreased to 400µA.

OPERATION

Buck Mode End of Charge Operation

The energy reservoir on CAP will continue to supply energy to keep V_{IN} at the regulation point for as long as possible. However, at some point, if the system load at V_{IN} continues to be present, the CAP voltage will drop low enough such that the V_{IN} regulation voltage can no longer be maintained due to minimum off-time restrictions. The minimum off-time restriction is present because during every cycle, the bottom switch needs to turn on. Once such a condition is reached, the V_{IN} voltage will regulate to roughly 93% of the CAP voltage. The switching regulator will continue to operate in such a manner until either the RUN voltage falls below 1.1V or the V_{IN} voltage falls below what is necessary for the regulator to operate (typically 2.8V). When either of those situations is reached, both the top and bottom switches are turned off, and the gate of the disconnect switch is pulled low.

Boost/Buck Switchover Operation

The LTC3643 transitions between boost and buck modes of operation depending on the PFI voltage. If the PFI voltage goes above 1.1V, it is deemed that power at the input supply is good and the boost phase is engaged. If the PFI voltage falls below 1V, it is deemed that the input supply is no longer high enough to supply the system load, and buck phase is engaged. The PFO pin is an indicator pin that will display if there is an input power fail. Connect a pull-up resistor from that pin to a known rail (<6V). A high on that pin indicates the input supply is insufficient.

The transition from boost to buck mode is relatively fast (~2µs) in order to prevent the voltage on V_{IN} to deplete too much before the buck regulator engages, whereas the transition from buck to boost is somewhat slower (~20µs). This time delay, combined with the 50mV hysteresis on the PFI threshold voltage, helps eliminate momentary glitches on the PFI pin, and prevents unnecessary mode transitions.

Gate Control for External PMOS Switch

Often times, when the V_{IN} voltage falls below the PFI threshold and buck mode is engaged, it is required to have a blocking element present to prevent back conduction of current into the depleted power supply. Placing a Schottky between the power supply and CLP will achieve that result, but would result in significant power dissipation through the diode when the power supply is present at high load.

To mitigate this power loss, an external power PMOS device with low RDS_{ON} can be used in place of the Schottky with its gate connected to the GATE pin of the LTC3643. When the application transitions from boost mode to buck mode, the GATE voltage will instantaneously get pulled up to V_{IN}, thus shutting off the external PMOS. When the power supply becomes ready again, the GATE voltage will get pulled low slowly with a 70µA current source, and that voltage will be internally clamped to go no lower than 6V below V_{IN}.

Boost Mode Current Limiting

If the power supply is current limited, the LTC3643 has the capability of limiting the input current of the boost regulator to ensure that the cumulative current of the boost regulator and the system load does not exceed a programmed amount. That current limit is programmed by the sense resistor between the CLP and V_{IN} pins.

In the application example of figure 3, a 10mΩ resistor is placed between CLP and V_{IN}. The voltages across those pins are designed to not exceed 50mV. Thus, a cumulative 5A is allowed to flow through the boost regulator (I1) and the system load (I2). If I2 in the application is 4A, then a maximum of 1A of current can flow through the boost regulator. If I2 is minimal, then I1 will be limited by the maximum current of the boost regulator. Furthermore, if I2 exceeds the 5A limit, the I_{TH} voltage of the regulator will get pulled low and the part will enter its sleep mode.

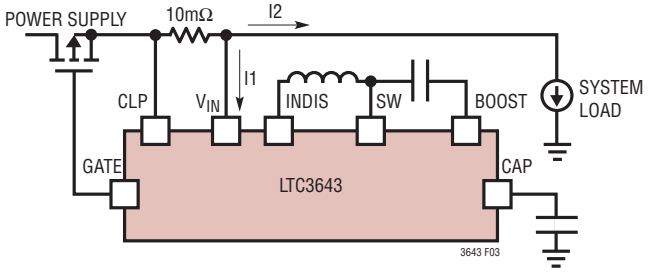


Figure 3. PowerPath of Boost Regulator with CLP Programmability

OPERATION

$INTV_{CC}$ Regulator

The LTC3643 has an onboard Low Dropout Regulator powered from V_{IN}, and the $INTV_{CC}$ voltage is regulated to 3.3V. The power dissipated across this LDO would thus be equal to $(V_{IN} – 3.3V) • I_{INTVCC}$. For a typical application, if the regulator is running in continuous mode, the current draw from the $INTV_{CC}$ by the chip is roughly 10mA.

V_{IN} Undervoltage Programming

The LTC3643 offers an accurate RUN threshold to start the regulator. As a result, a resistor divider from V_{IN} to GND can be placed with the intermediate node fed back to RUN to set an accurate V_{IN} Undervoltage threshold. As the input voltage rises, the RUN voltage will increase above the V_{RUN} rising threshold (1.2V), and the regulator will turn on. Similarly, once on, if the input voltage decreases below the V_{RUN} falling threshold (1.1V), the regulator will turn off.

Output Voltage Programming

The step down converter output V_{IN} and the step-up charger output V_{CAP} are set by an external resistive divider according to the following equations:

$$V_{IN} = 0.6V \left(1 + \frac{R2}{R1}\right)$$

$$V_{CAP} = 0.6V \left(1 + \frac{R4}{R3}\right)$$

To improve the frequency response, a feedforward capacitor C_{FF} may also be used. Great care should be taken to route the FBSYS or FBCAP line away from noise sources, such as the inductor or the SW trace.

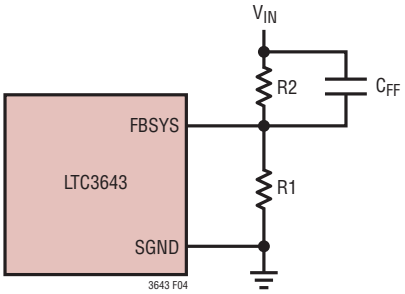


Figure 4. Setting The V_{IN} Voltage In Step-Down Mode

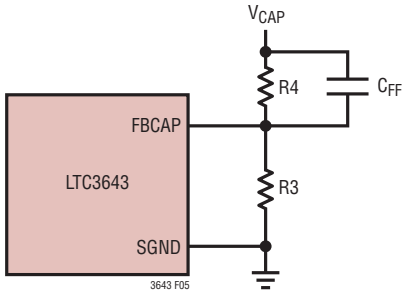


Figure 5. Setting The V_{CAP} Voltage In Step-Up Mode

APPLICATIONS INFORMATION

Input Capacitor (C_{IN}) Selection

If the LTC3643 is only used in the boost direction, then the input filter capacitor is only required to reduce peak currents drawn from the input source and reduce input switching noise. A low ESR bypass capacitor with a value of at least 4.7µF should be located as close to the V_{IN} pin as possible.

However, in applications where buck mode is engaged, more bypass capacitance is required. The selection of C_{IN} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The Input ripple, ΔV_{IN}, is determined by:

$$\Delta V_{IN} < \Delta I_L \left(\frac{1}{8 \bullet f \bullet C_{IN}} + ESR \right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors are very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics and small footprints.

Using Ceramic V_{IN} and CAP Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the V_{CAP} input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{CAP} large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R and X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. In both the buck mode and boost mode cases, during a load step, the V_{IN} and CAP capacitor respectively must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load.

Typically in buck mode, ~5 cycles are required to respond to a load step but only in the first cycle does the V_{IN} voltage drop linearly. The V_{IN} voltage droop, V_{DROOP}, is usually about 3 times the linear drop of the first cycle. Thus, a good place to start with the V_{IN} capacitor value is approximately:

$$C_{IN} = 3 \frac{\Delta I_{IN}}{f_0 \bullet V_{DROOP}}$$

The boost mode response is typically much slower than that of the buck and has a dependency on the duty cycle of the application. Typically, the loop response will be at least 3 times slower than that of the buck. Thus, more ceramic capacitance at CAP may be required. However, in most applications, the LTC3643 will be used to charge a bulk capacitor in which case placing the 22µF ceramic capacitor in parallel to the bulk capacitor just to filter out the square wave current is sufficient.

Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency (1MHz) determine the ripple current:

$$\Delta I_L = \frac{V_{IN}}{10^6 \bullet L} \left(1 - \frac{V_{IN}}{V_{CAP(MAX)}} \right)$$

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Lower ripple current reduces core losses in the inductor and reduces V_{IN} voltage ripple. However, at extremes, low ripple causes inductor current sensing issues. Highest efficiency operation is obtained at low frequency with reasonably small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency and operating frequency.

A reasonable starting point is to choose a ripple current that is about 50% of $I_{OUT(MAX)}$. To guarantee that ripple current does not exceed specified inductor saturation current ratings, the inductance should be chosen according to:

$$L = \frac{V_{IN}}{10^6 \bullet \Delta I_{L(MAX)}} \left(1 - \frac{V_{IN}}{V_{CAP(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. Core loss is very dependent on the material, frequency and inductance selected. Higher inductance reduces ripple. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite materials have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard”, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don’t radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Toko, Vishay, NEC/Tokin, Cooper, TDK and Wurth Electronik. Refer to Table 1 for more details.

Boost Mode Transient Response

The LTC3643 in boost mode uses peak current mode control compensated with an RC network on the external ITH pin. The ITH external component network shown in Figure 6 will provide an adequate starting point for most applications. The RC filter sets the dominant pole-zero loop compensation. The values can be modified to optimize transient response once the PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because their various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Table 1. Inductor Selection Table

Vendor	P/N	L (µH)	I (A)	L (mm)	W (mm)	H (mm)
Coilcraft	XAL5030(50)-XXX	0.16-22	31-3.6	5.28	5.48	3.1-5.1
Coilcraft	XAL6030(60)-XXX	0.18-22	39-5.6	6.36	6.56	3.1-6.1
SUMIDA	CDEP1Ø5NP-XXX	0.15-8.8	55-4	10	10	5.6
SUMIDA	CEP125NP-XXX	0.8-10	35-5	12.9	12.9	5.6
Wurth Elekt.	744393580XX	1-10	17-5.8	8.3	8.8	7.8
Wurth Elekt.	7440280000XX	0.056-6.8	6-0.55	2.8	2.8	1.1
Coiltronics	DR73-XXX-R	0.33-1000	14.4-0.25	6.0	7.6	3.55

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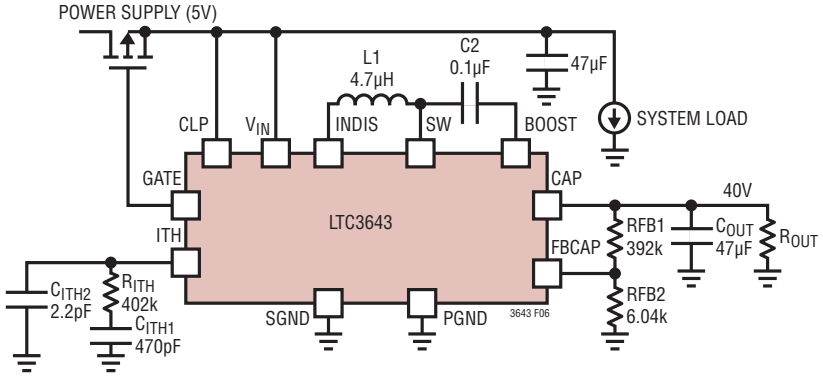

Figure 6. 5V to 40V Boost Application

Figure 7 shows a simplified block diagram for the application in Figure 6, and can be used to analyze the stability of the application with the given compensation components.

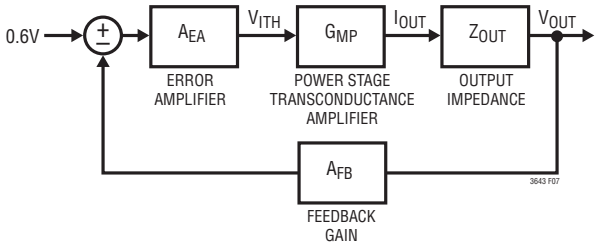

Figure 7. Block Diagram of the Boost Regulator

A_{EA} signifies the voltage gain of the internal error amplifier. It translates a difference of FB input error to the output I_{TH} voltage. The g_m of the error amplifier, $g_m(EA)$, is fixed to the regulator and is typically 210µmho. With the compensation network on ITH, for frequencies above the error amplifier zero, Z1, the gain is roughly $A_{EA(FLATBAND)}$.

$$Z_1 = \frac{1}{2\pi \bullet R_{ITH} \bullet C_{ITH1}} = 0.85kHz$$

$$A_{EA(FLATBAND)} = g_m(EA) \bullet R_{ITH1} = 82.8V / V$$

C_{ITH2} is used purely to filter out high frequency signals and as long as it is sized significantly smaller than C_{ITH1}, it should not affect the loop stability of the regulator.

G_{MP} is the transconductance gain from V_{ITH} to I_{OUT}. Because of the architecture of the regulator, the gain from V_{ITH} to I_L (inductor current) is fixed internally to be 3mmho. Furthermore, the DC gain from I_L to I_{OUT} is equal to A_{MP}:

$$A_{MP} = \frac{\eta \bullet V_{IN}}{V_{CAP}} A / A$$

Where η is the efficiency of the regulator. Assuming a 90% efficiency and a 5V in to 40V out application:

$$A_{MP} = 0.1125\ A/A$$

The AC component of the G_{mp} can be mainly attributed to the RHP zero of the boost regulator, Z_2:

$$Z_2 = \frac{V_{IN}^2}{2\pi \bullet P_{OUT(MAX)} \bullet L_1} Hz$$

Since $P_{OUT(MAX)} = V_{IN} \bullet I_{L(MAX)} \bullet \eta$,

$$Z_2 = \frac{V_{IN}}{2\pi \bullet \eta \bullet I_{L(MAX)} \bullet L_1} = 94kHz$$

The total loop must be compensated such that the crossover frequency is at least 10× slower than that of Z_2.

Z_{OUT} is the output impedance of the application. It has a DC gain of R_{OUT} and a pole at P_1:

$$P_1 = \frac{1}{2\pi \bullet R_{OUT} \bullet C_{OUT}} Hz$$

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As a result, the load pole has a unity gain impedance at:

$$\frac{1}{2\pi \bullet C_{OUT}} = 3.4kHz$$

The last component of the loop is A_{FB}, which is the gain from V_{OUT} to V_{FB}, and in this application, it is simply 0.015 V/V.

For a rough estimation of the crossover frequency of the entire loop, analysis can be done at frequency Z_1. At that frequency:

$$A_{EA} \approx A_{EA(FLATBAND)} = 82.8V / V$$

$$G_{MP} \approx 3 \bullet A_{MP} = 0.33\Omega$$

$$Z_{OUT} \approx \frac{P_Z}{Z_1} = 4\Omega$$

$$A_{FB} = 0.015V / V$$

The total loop gain at Z1 is thus equal to the product of all the components which is 1.64V/V. In addition, at that frequency, since the zero frequency of the error amplifier has already been reached, the system looks like a single pole system, thus making the crossover frequency roughly:

1.64 • Z1 = 1.4kHz.

For applications where a large energy reservoir capacitor is placed in parallel to the C_{OUT}, the Z_{OUT} component of the block diagram needs to be remodeled, but often times, the zero frequency of the ESR of the large capacitor and its capacitance is well below the crossover frequency of the loop, and can be ignored in analyzing the stability of the loop.

Buck Mode Transient Response

The buck mode transient response can be checked by looking at the load response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{IN} immediately shifts by an amount equal to the ΔI_{LOAD} • ESR, where ESR is the effective series resistance of C_{IN}. ΔI_{LOAD} also begins to charge or discharge C_{IN} generating a feedback error signal used by the regulator to return V_{IN} to its steady-state value. During this recovery time, V_{IN} can be monitored for overshoot or ringing that would indicate a stability problem. The compensation for the buck mode of the LTC3643 is implemented internal to the IC.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

In some applications, a more severe transient can be caused by switching in loads with large (>1µF) input capacitors. The discharged input capacitors are effectively put in parallel with C_{IN}, causing a rapid drop in V_{IN}. No regulator can deliver enough current to prevent this problem if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection and soft-starting.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

% Efficiency = 100% – (L1 + L2 + L3 +…)

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where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LTC3643 circuits: 1) I^2R losses, 2) switching and biasing losses, and 3) other losses.

1. I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average input current flows through inductor L and front end disconnect switch but is "chopped" between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

   $$R_{SW} = (R_{DS(ON)TOP})(1\text{-}DC) + (R_{DS(ON)BOT})\,(DC) + R_{DS(ON)BLKFET}$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus to obtain I^2R losses:

   $$I^2R \text{ losses} = I_L{}^2(R_{SW} + R_L)$$

2. The switching current is the sum of the MOSFET driver and control currents. The power MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} that is typically much larger than the DC control bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs and f is the switching frequency. The power loss is thus:

   $$\text{Switching Loss} = I_{GATECHG} \bullet V_{IN}$$

3. Other "hidden" losses such as transition loss and copper trace and internal load resistances can account for additional efficiency degradations in the overall power system. It is very important to include these "system" level losses in the design of a system. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. The LTC3643 internal power devices switch quickly enough that these losses are not significant compared to other sources. Other losses including diode conduction losses during dead-time and inductor core losses which generally account for less than 2% total additional loss.

Thermal Conditions

In a majority of applications, the LTC3643 does not dissipate much heat due to its high efficiency and low thermal resistance of its exposed-back QFN package. However, in applications where the LTC3643 is running at high ambient temperature, high V_{IN}, and maximum output load current, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 160°C, both power switches will be turned off until the temperature drops about 15°C cooler.

To avoid the LTC3643 from exceeding the maximum junction temperature, some thermal analysis must be done. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$t_{RISE} = P_D \bullet \theta_{JA}$$

As an example, consider the case when the LTC3643 is used in applications where V_{IN} = 5V, I_L = 2A, and V_{CAP} = 40V. The equivalent power MOSFET resistance R_{SW} is:

$$R_{SW} = R_{DS(ON)TOP} \bullet \frac{V_{IN}}{V_{CAP}} + R_{DS(ON)BOT} \bullet \left(1 - \frac{V_{IN}}{V_{CAP}}\right) + R_{DS(ON)BLKFET}$$

$$= 150m\Omega \bullet \frac{5V}{40V} + 75m\Omega \bullet \left(1 - \frac{5V}{40V}\right) + 50m\Omega$$

$$= 134m\Omega$$

Typically, the current drawn from $INTV_{CC}$ will be 10mA.

Therefore, the total power dissipated by the part is:

$$P_D = I_{OUT}{}^2 \bullet R_{SW} + V_{IN} \bullet I_{INTVCC}$$

$$= 4A^2 \bullet 134m\Omega + 5V \bullet 10mA$$

$$= 587.5mW$$

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The QFN package junction-to-ambient thermal resistance, θ_{JA}, is around 46°C/W. Therefore, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately:

$T_J = 0.587W \bullet 46°C/W + 25°C = 52°C$

Remembering that the above junction temperature is obtained from an $R_{DS(ON)}$ at 25°C, we might recalculate the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature. Redoing the calculation assuming that R_{SW} increased 10% at 52°C yields a new junction temperature of 54.4°C. If the application calls for a higher ambient temperature and/or higher switching frequency, care should be taken to reduce the temperature rise of the part by using a heat sink or air flow.

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3643. Check the following in your layout:

1. Do the capacitors C_{CAP} connect to the CAP and GND terminals as close as possible?
2. Are C_{IN} and L closely connected? The (–) plate of C_{IN} returns current to GND and the (–) plate of C_{CAP}.
3. Solder the Exposed Pad (Pin 25) on the bottom of the package to the GND plane. Connect this GND plane to other layers with thermal vias to help dissipate heat from the LTC3643.
4. Keep sensitive components away from the SW pin. The compensation components C_{ITH} and R_{ITH}, all resistor dividers, and the $INTV_{CC}$ bypass caps should be routed away from the SW trace and the inductor.
5. A ground plane is required.
6. Flood all unused areas on all layers with copper, which reduces the temperature rise of power components. These copper areas should be connected to GND.

Holdup Time Calculation

The amount of energy available in the energy reservoir capacitor before the voltage droops below the desired backup voltage is equal to:

$$E_{CAP} = \frac{1}{2} C_{CAP} \left(V_{CAP}^2 - V_{IN}^2 \right)$$

The amount of energy necessary to complete the backup is equal to:

$E_{LOAD} = I_{SYS} \bullet V_{IN} \bullet t_{HT}$

Where t_{HT} is the amount of backup time needed.

Assuming an efficiency of η (this number will vary depending on the application), the total amount of backup time will be equal to:

$$t_{HT} = \frac{E_{CAP} \bullet \eta}{I_{SYS} \bullet V_{IN}} = \frac{C_{CAP} \left(V_{CAP}^2 - V_{IN}^2 \right) \bullet \eta}{2 \bullet I_{SYS} \bullet V_{IN}}$$

Where I_{SYS} is the system load during backup.

Design Example

As a design example, consider the LTC3643 in an application with the following specifications:

V_{IN} = 4V to 8V

V_{CAP} = 40V

I_{CAP} (Input) = 2A

Given the internally programmed switching frequency of 1MHz, we can calculate the inductor value for about 40% ripple current (800mA based on an average of 2A output current) at maximum V_{IN}:

$$L = \left(\frac{8V}{1MHz \bullet 0.8A} \right) \left(1 - \frac{8V}{40V} \right) = 8\mu H$$

Given this, an 8.2µH inductor would suffice.

C_{CAP} and C_{IN} will be selected based on what is required to satisfy the output voltage ripple requirement for the boost and buck modes respectively. A 22µF or 47µF capacitor on both nodes is adequate for most applications.

APPLICATIONS INFORMATION

C_{CAP} Size Selection for System Backup Power Applications

This section of the data sheet will discuss how large to size the CAP capacitor, C_{CAP}, to insure that there is sufficient energy to hold up the Input supply when power is removed. Consider the design example where:

V_{IN} = 5V

V_{CAP} = 40V

Holdup Time (t_{HT}) = 10msec

System Current Load (I_{SYS}) = 2A

The total Energy required during holdup time is equal to:

$E_{DISS} = V_{IN} \bullet I_{SYS} \bullet t_{HT}$ = 100mW-sec

Total energy available is equal to:

$$E_{AVAL} = \frac{C_{CAP}}{2}\left(V_{CAP}^2 - V_{IN}^2\right) = 787.5 \bullet C_{CAP}\,(\text{W-sec})$$

Since the regulator is not lossless, the efficiency needs to be taken into consideration, such that:

$E_{AVAL} \bullet eff > E_{DISS}$

$$C_{CAP} = \frac{E_{DISS}}{eff \bullet E_{AVAL}}$$

Assuming an efficiency of 90%, with 100mW-sec required by the system, C_{CAP} needs to be at least 141µF.

To be conservative, and to account for some voltage coefficient and tolerance of the capacitors, the capacitor is recommended to be at least 30% larger than required. In this particular case, four 47µF capacitors (188µF total) would be recommended.

CAP Capacitor (C_{CAP}) Selection

When selecting CAP capacitors, the magnitude of the peak inductor current, together with the ripple voltage specifications, determine the choice of the capacitor. Both the ESR (equivalent series resistance) of the capacitor and the charge stored in the capacitor each cycle contribute to the output voltage ripple.

The ripple due to the charge is approximately:

$$V_{RIPPLE(CHARGE)} \cong \frac{I_P \bullet V_{IN}}{C_{CAP} \bullet V_{CAP} \bullet f}$$

where I_P is the peak inductor current.

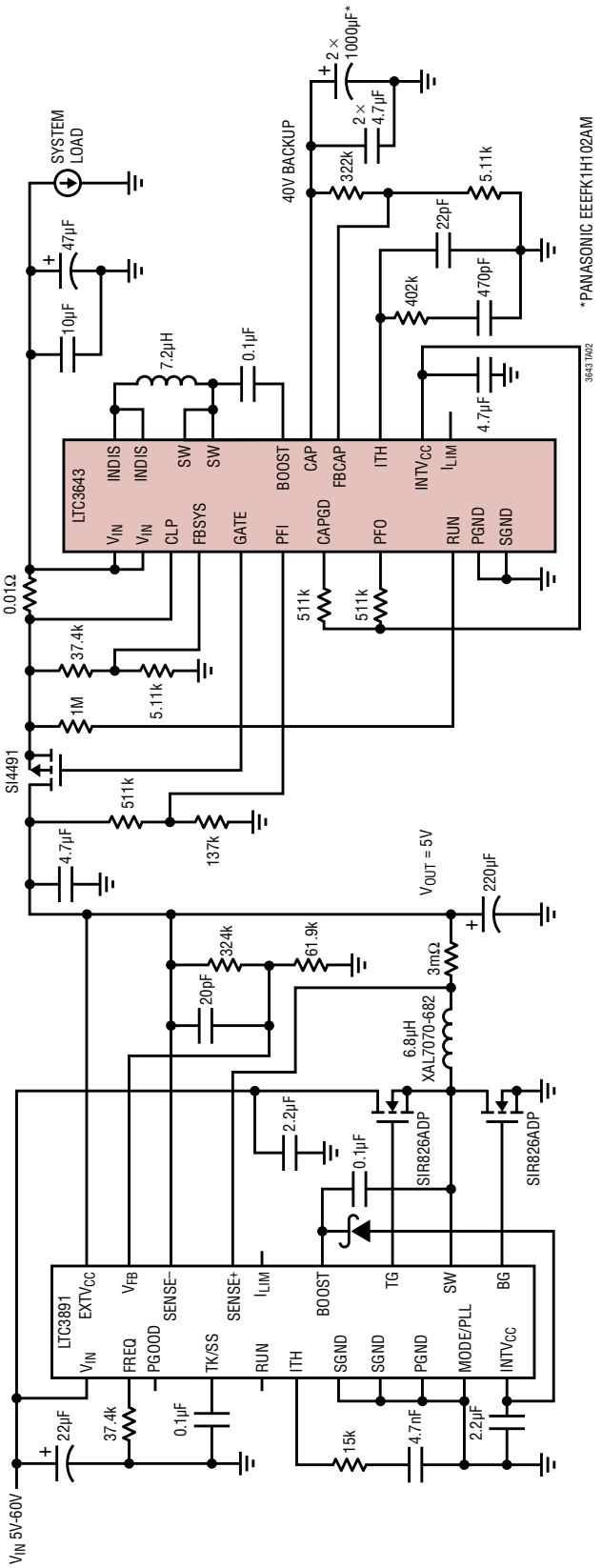
The ESR of the C_{CAP} is usually the most dominant factor for ripple in most power converters. The ripple due to the capacitor ESR is:

$$V_{RIPPLE(ESR)} = I_{LOAD} \bullet R_{ESR} \bullet \frac{V_{OUT}}{V_{IN}}$$

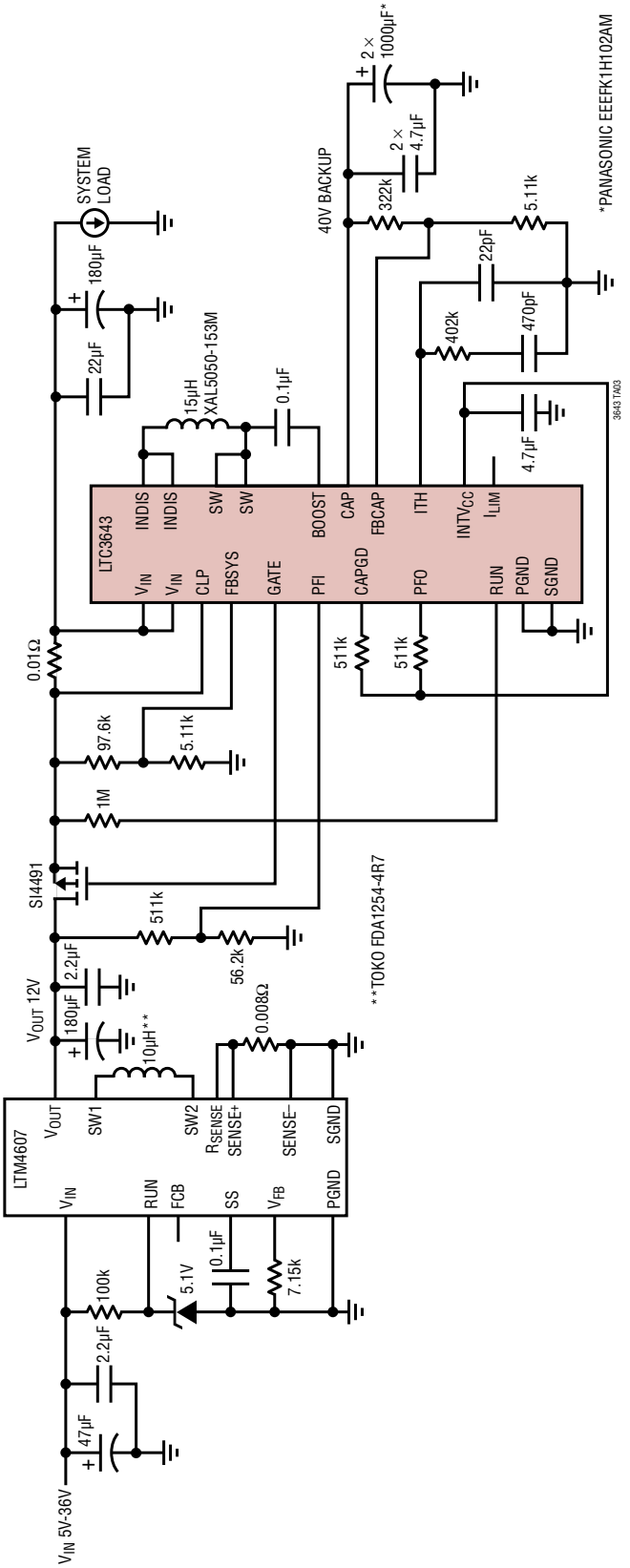
where R_{ESR} is equal to the capacitor ESR.

In applications where a large energy storage capacitor is used, a smaller ceramic bypass capacitor is still required close to the regulator due to its low ESR. Typically, a 22µF ceramic capacitor is sufficient for most applications.

TYPICAL APPLICATIONS



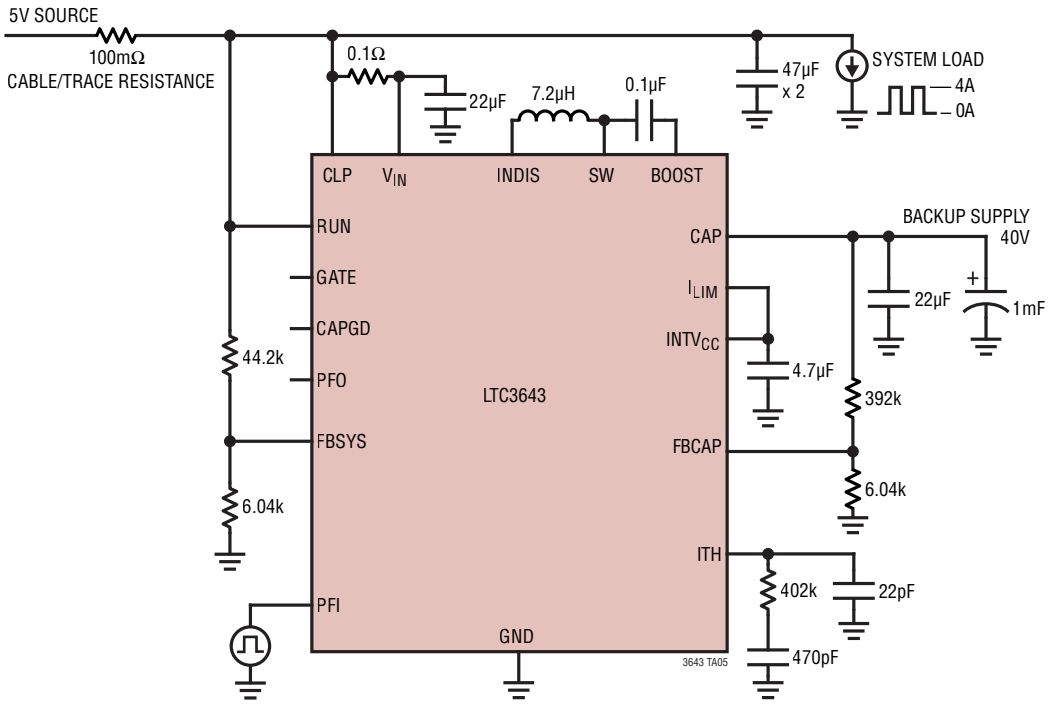
TYPICAL APPLICATIONS



12V Backup System for Automotive Applications

TYPICAL APPLICATIONS

Temporary Supply Booster

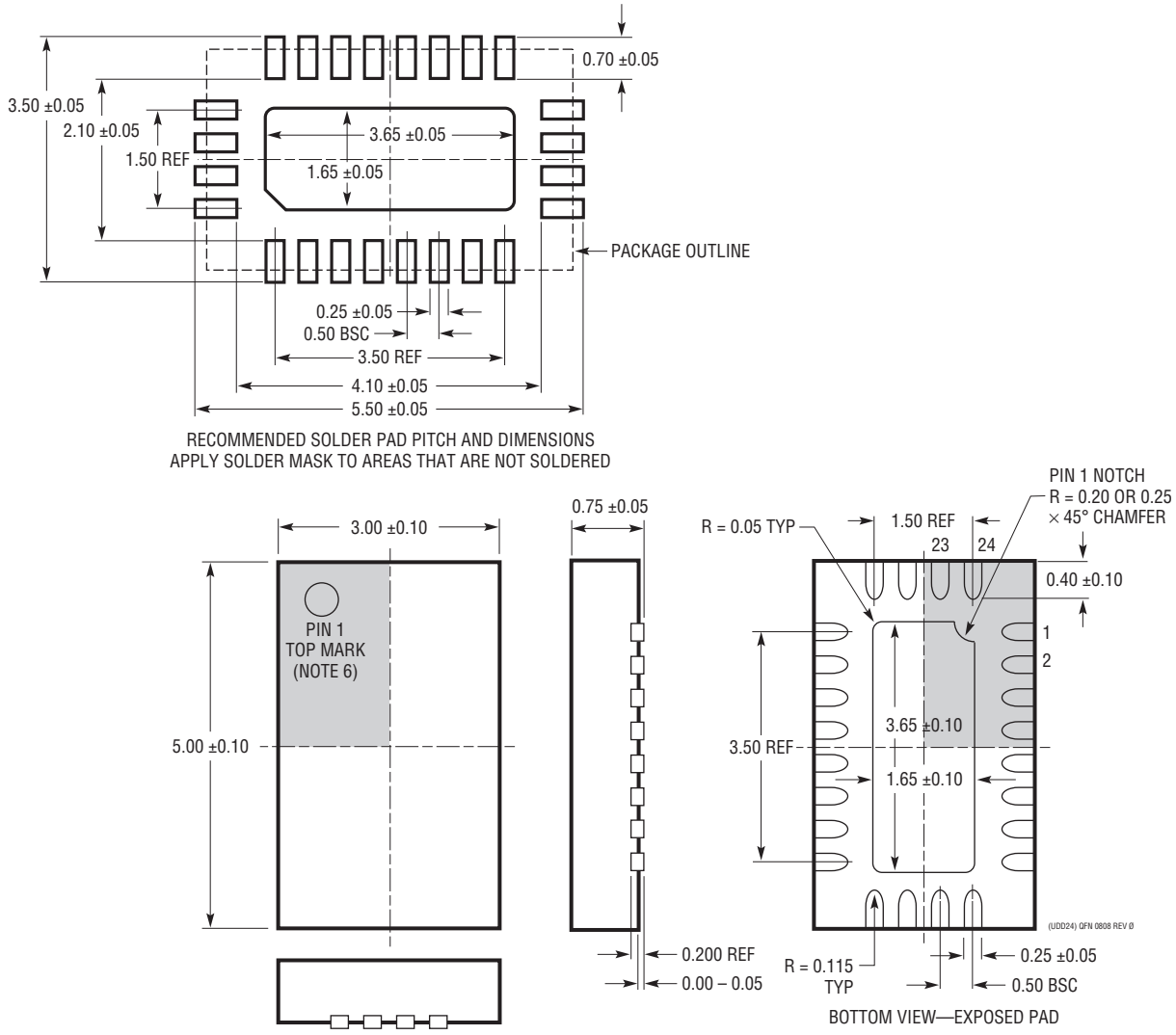


NOTE: DRIVE PFI PIN HIGH WHEN HIGH LOAD IS PRESENT TO MAINTAIN DESIRED VOLTAGE AT THE SYSTEM LOAD

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3643#packaging for the most recent package drawings.

UDD Package
24-Lead Plastic QFN (3mm × 5mm)
(Reference LTC DWG # 05-08-1833 Rev Ø)



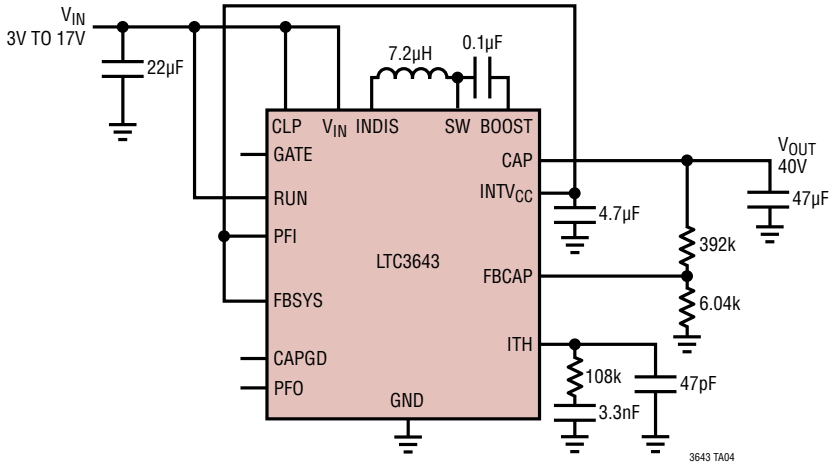
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/15	Changed Typical Application graph	1
B	02/16	Updated I_{LIM} pin description wording	7
		Updated voltage from 1.2V to 1.1V on PFI comparator of Figure 1	9
		Updated voltage from 1.2V to 1.1V on PFI comparator of Figure 2	10
C	05/17	Updated I_{LIM} pin text description	7
		Corrected PFI falling threshold from 1.15V to 1V	11
		Corrected PFI rising/falling threshold to 1.1V and 1V, respectively (Boost/Buck Switchover)	12
		Updated number calculations in Applications Information section	17
		Updated pin label from IN to V_{IN}	21, 22
D	04/25	Updated Applications	1
		Updated Order Information	2

TYPICAL APPLICATION

40V Synchronous Boost Regulator with Input Disconnect



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3110	2A Bidirectional Buck-Boost DC/DC Regulator and Charger/Balancer	V_{CAP} Range: 0.1V to 5.5V V_{SYS} Range 1.71V to 5.25V, Automatic Switchover from Charge to Backup Mode. 24-Lead TSSOP and 4mm × 4mm QFN Packages.
LTC3128	3A Monolithic Buck-Boost Supercapacitor Charger and Balancer with Accurate Input Current Limit	±2% Accurate Average Input Current Limit Programmable to 3A, Active Charge Balancing, Charges 1 or 2 Capacitors, V_{IN} Range: 1.73V to 5.5V, V_{OUT} Range: 1.8V to 5.5V, 20-Lead 4mm × 5mm QFN and 24-Lead TSSOP Packages.
LTC3226	2-Cell Supercapacitor Charger with Backup PowerPath Controller	1x/2x Multimode Charge Pump Supercapacitor Charger, Automatic Cell Balancing, PowerPath, 2A LDO Backup Supply, Automatic Main/Backup Switchover, 2.5V to 5.5V, 16-Lead 3mm × 3mm QFN Package.
LTC3350	High Current Supercapacitor Backup Controller and System Monitor	High Efficiency Charging of 1 to 4 Series Supercapacitors. Step-Up Mode in Backup, System Health Monitoring. 38-Lead 5mm × 7mm QFN Package.
LTC3355	20V, 1A Buck DC/DC with Integrated SCAP Charger and Backup Regulator	V_{IN}: 3V to 20V, V_{OUT}: 2.7V to 5V, 1A Main Buck Regulator, 5A Boost Backup Regulator Powered from Single Supercapacitor, Overvoltage Protection. 20-Lead 4mm × 4mm QFN Package.
LTC3625	1A High Efficiency 2-Cell Supercapacitor Charger with Automatic Cell Balancing	High Efficiency Step-Up/Step-Down Charging of Two Series Supercapacitors. Automatic Cell Balancing. Programmable Charging Current to 500mA (Single Inductor), 1A (Dual Inductor). 12-Lead 3mm × 4mm DFN Package.
LTC4425	Linear SuperCap Charger with Current-Limited Ideal Diode and V/I Monitor	Constant-Current/Constant-Voltage Linear Charger for 2-Cell Series Supercapacitor Stack. V_{IN}: Li-Ion/Polymer Battery, a USB Port, or a 2.7V to 5.5V Current-Limited Supply. 2A Charge Current, Automatic Cell Balancing, Shutdown Current <2µA. 12-Pin 3mm × 3mm DFN or 12-Lead MSOP Package.
LTC4040	2.5A Battery Backup Power Manager	V_{IN}: 3.5V to 55V Contains a High Current Step-Up DC/DC Regulator to Back-Up the Supply from a Single Cell Li-Ion $LiFePO_4$ Battery, 24-Lead 4mm × 5mm QFN Package.