

Silicon Carbide (SiC) Combo JFET – EliteSiC, Power N-Channel, H-PDSO-F8, 750 V, 5.4 mohm

UG4SC075005L8S

Description

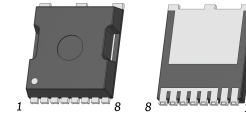
onsemi's UG4SC075005L8S "Combo-FET" integrates both a 750 V SiC JFET and a Low Voltage Si MOSFET into a single H-PDSO-F8 package. This innovative approach allows users to create circuitry that would enable a normally-off switch while leveraging the benefits of a normally-on SiC JFET. These benefits include ultra-low on-resistance ($R_{DS(on)}$) to minimize conduction losses and the exceptional robustness characteristic of a simplified JFET device structure, making it capable of handling the high-energy switching required in circuit protection applications. For switch-mode power conversion application, this device provides separate access to the JFET and MOSFET gates for improved speed control and ease of paralleling multiple devices.

Features

- Single Digit $R_{DS(on)}$
- Normally-off Capability
- Improved Speed Control
- Improved Parallel Device Operation (3+ FETs)
- Operating Temperature: 175 °C (Max)
- High Pulse Current Capability
- Excellent Device Robustness
- Silver-Sintered Die Attach for Excellent Thermal Resistance
- Short Circuit Rated
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

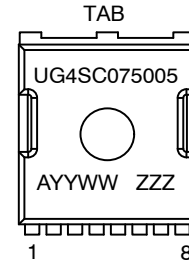
Typical Applications

- Solid State / Semiconductor Circuit Breaker
- Solid State / Semiconductor Relay
- Battery Disconnects
- Surge Protection
- Inrush Current Control
- High Power Switch Mode Converters (>25 kW)



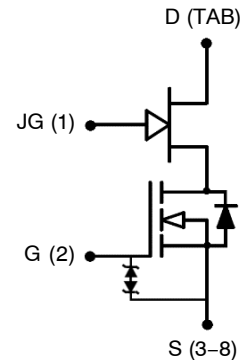
H-PDSO-F8
CASE 740AA

MARKING DIAGRAM



UG4SC075005	= Specific Device Number
A	= Assembly Location
YY	= Year
WW	= Work Week
ZZZ	= Lot ID

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

UG4SC075005L8S

MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Value	Unit
V_{DS}	Drain-Source Voltage		750	V
V_{JGS}	JFET Gate (JG) to Source Voltage	DC	-30 to +3	V
		AC (Note 1)	-30 to +30	V
V_{GS}	MOSFET Gate (G) to Source Voltage	DC	-20 to +20	V
		AC ($f > 1$ Hz)	-25 to +25	V
I_D	Continuous Drain Current (Note 2)	$T_C < 144$ °C	120	A
I_{DM}	Pulsed Drain Current (Note 3)	$T_C = 25$ °C	588	A
E_{AS}	Single Pulsed Avalanche Energy (Note 4)	$L = 15$ mH, $I_{AS} = 6.5$ A	316	mJ
t_{SC}	Short Circuit Withstand Time	$V_{DS} = 400$ V, $T_{J(START)} = 175$ °C	5	μs
dv/dt	SiC FET dv/dt Ruggedness	$V_{DS} < 500$ V	100	V/ns
P_{tot}	Power Dissipation	$T_C = 25$ °C	1153	W
$T_{J,max}$	Maximum Junction Temperature		175	°C
T_J, T_{STG}	Operating and Storage Temperature		-55 to 175	°C
T_{solder}	Reflow Soldering Temperature	Reflow MSL 1	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. +30 V AC rating applies for turn-on pulses < 200 ns applied with external $R_G > 1$ Ω.
2. Limited by Bondwires
3. Pulse width t_p limited by $T_{J,max}$.
4. Starting $T_J = 25$ °C

THERMAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		-	0.10	0.13	°C/W

ELECTRICAL CHARACTERISTICS ($T_J = +25$ °C and $V_{JGS} = 0$ V unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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TYPICAL PERFORMANCE - STATIC

BV_{DS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 1$ mA	750	-	-	V
I_{DSS}	Total Drain Leakage Current	$V_{DS} = 750$ V, $V_{GS} = 0$ V, $T_J = 25$ °C	-	6	130	μA
		$V_{DS} = 750$ V, $V_{GS} = 0$ V, $T_J = 175$ °C	-	45	-	
I_{JGSS}	Total JFET Gate Leakage Current	$V_{GS} = -20$ V, $V_{DS} = 12$ V	-	0.1	100	μA
I_{GSS}	Total MOSFET Gate Leakage Current	$V_{GS} = -20$ V / +20 V	-	6	20	μA
$R_{DS(on)}$	Drain-Source On-resistance	$V_{GS} = 15$ V, $V_{JGS} = 2$ V, $I_D = 80$ A, $T_J = 25$ °C	-	5.0	-	mΩ
		$V_{GS} = 15$ V, $V_{JGS} = 0$ V, $I_D = 80$ A, $T_J = 25$ °C	-	5.4	7.2	
		$V_{GS} = 15$ V, $V_{JGS} = 0$ V, $I_D = 80$ A, $T_J = 125$ °C	-	9.3	-	
		$V_{GS} = 15$ V, $V_{JGS} = 0$ V, $I_D = 80$ A, $T_J = 175$ °C	-	12.2	-	
$V_{JG(th)}$	JFET Gate Threshold Voltage	$V_{DS} = 5$ V, $V_{GS} = 12$ V, $I_D = 180$ mA	-8.3	-6.0	-3.7	V
$V_{G(th)}$	MOSFET Gate Threshold Voltage	$V_{DS} = 5$ V, $I_D = 10$ mA	4	4.7	6	V
R_{JG}	JFET Gate Resistance	$f = 1$ MHz, open drain	-	0.8	-	Ω
R_G	MOSFET Gate Resistance	$f = 1$ MHz, open drain	-	0.8	-	Ω

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ELECTRICAL CHARACTERISTICS ($T_J = +25\text{ }^{\circ}\text{C}$ and $V_{JGS} = 0\text{ V}$ unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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TYPICAL PERFORMANCE - REVERSE DIODE

I_S	Diode Continuous Forward Current (Note 1)	$T_C < 144\text{ }^{\circ}\text{C}$	–	–	120	A
$I_{S,pulse}$	Diode Pulse Current (Note 2)	$T_C = 25\text{ }^{\circ}\text{C}$	–	–	588	A
V_{FSD}	Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 50\text{ A}, T_J = 25\text{ }^{\circ}\text{C}$	–	1.03	1.16	V
		$V_{GS} = 0\text{ V}, I_S = 50\text{ A}, T_J = 175\text{ }^{\circ}\text{C}$	–	1.06	–	
Q_{rr}	Reverse Recovery Charge	$V_{DS} = 400\text{ V}, I_S = 80\text{ A},$ $V_{GS} = 0\text{ V}, V_{JGS} = 0\text{ V},$ $R_{JG} = 0.7\text{ }\Omega,$ $di/dt = 2400\text{ A}/\mu\text{s}, T_J = 25\text{ }^{\circ}\text{C}$	–	377	–	nC
t_{rr}	Reverse Recovery Time		–	70	–	ns
Q_{rr}	Reverse Recovery Charge	$V_{DS} = 400\text{ V}, I_S = 80\text{ A},$ $V_{GS} = 0\text{ V}, V_{JGS} = 0\text{ V},$ $R_{JG} = 0.7\text{ }\Omega,$ $di/dt = 2400\text{ A}/\mu\text{s}, T_J = 150\text{ }^{\circ}\text{C}$	–	427	–	nC
t_{rr}	Reverse Recovery Time		–	78	–	ns

TYPICAL PERFORMANCE - DYNAMIC WITH MOSFET GATE AS CONTROL TERMINAL AND $V_{JGS} = 0\text{ V}$

C_{iss}	MOSFET Input Capacitance	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V},$ $f = 100\text{ kHz}$	–	8374	–	pF
C_{oss}	Output Capacitance		–	362	–	
C_{rss}	Reverse Transfer Capacitance		–	4	–	
$C_{oss(er)}$	Effective Output Capacitance, Energy Related	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	–	475	–	pF
$C_{oss(tr)}$	Effective Output Capacitance, Time Related		–	950	–	pF
Q_G	Total Gate Charge	$V_{DS} = 400\text{ V}, I_D = 80\text{ A},$ $V_{GS} = 0\text{ V to } 15\text{ V}$	–	164	–	nC
Q_{GD}	Gate-Drain Charge		–	24	–	
Q_{GS}	Gate-Source Charge		–	46	–	

TYPICAL PERFORMANCE - DYNAMIC WITH JFET GATE AS CONTROL TERMINAL AND $V_{GS} = +12\text{ V}$

C_{Jiss}	JFET Input Capacitance	$V_{DS} = 400\text{ V}, V_{JGS} = -20\text{ V},$ $f = 100\text{ kHz}$	–	3028	–	pF
C_{Joss}	JFET Output Capacitance		–	364	–	
C_{Jrss}	JFET Reverse Transfer Capacitance		–	360	–	
Q_{JG}	JFET Total Gate Charge	$V_{DS} = 400\text{ V}, I_D = 80\text{ A},$ $V_{JGS} = -18\text{ V to } 0\text{ V}$	–	400	–	nC
Q_{JGD}	JFET Gate-drain Charge		–	270	–	
Q_{JGS}	JFET Gate-source Charge		–	60	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE DIAGRAMS - MOSFET GATE AS CONTROL TERMINAL AND $V_{JGS} = 0$ V

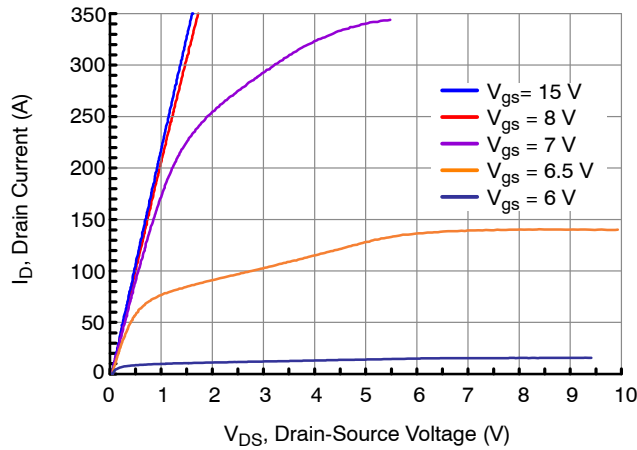


Figure 1. Typical Output Characteristics at $T_J = -55\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

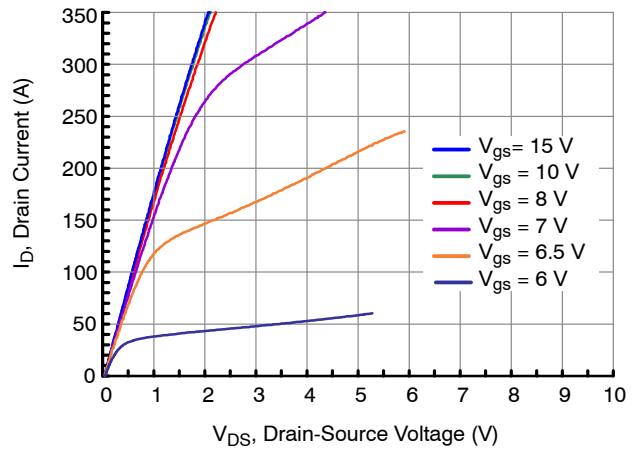


Figure 2. Typical Output Characteristics at $T_J = 25\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

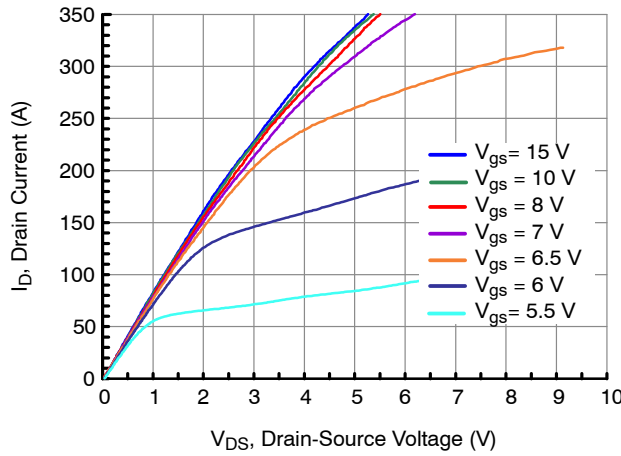


Figure 3. Typical Output Characteristics at $T_J = 175\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

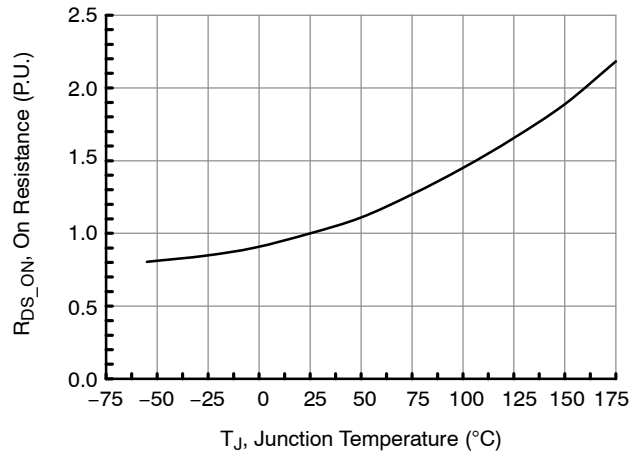


Figure 4. Normalized On-Resistance vs. Temperature at $V_{GS} = 12$ V and $I_D = 80$ A

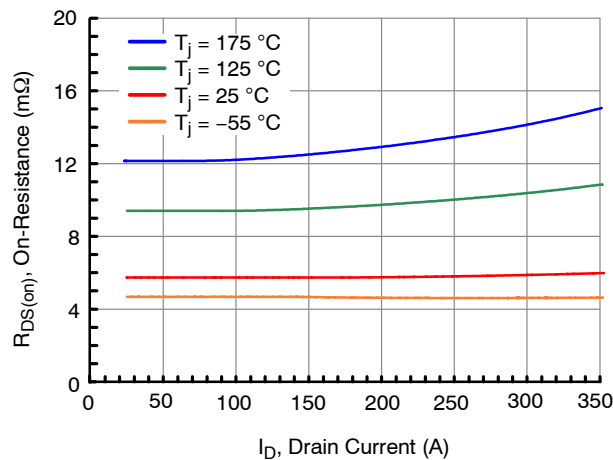


Figure 5. Typical Drain-Source On-Resistances at $V_{GS} = 12$ V

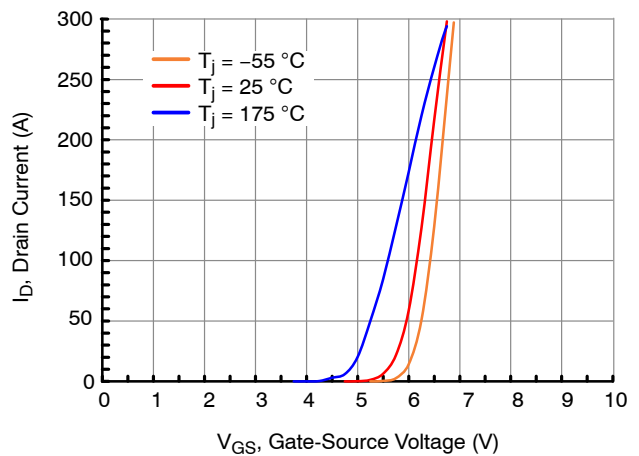


Figure 6. Typical Transfer Characteristics at $V_{DS} = 5$ V

TYPICAL PERFORMANCE DIAGRAMS - MOSFET GATE AS CONTROL TERMINAL AND $V_{JGS} = 0\text{ V}$

(continued)

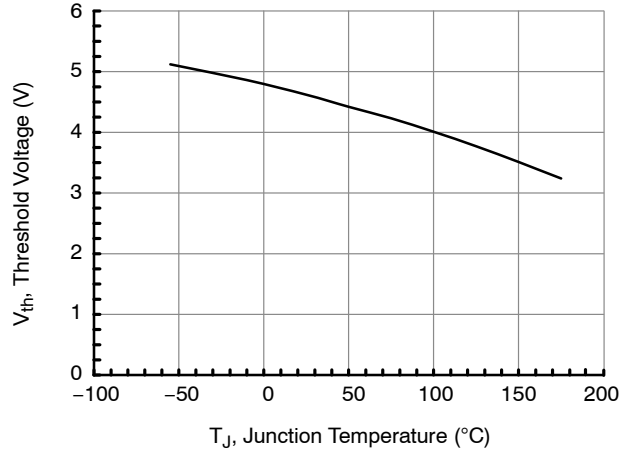


Figure 7. Threshold Voltage vs Junction Temperature at $V_{DS} = 5\text{ V}$ and $I_D = 10\text{ mA}$

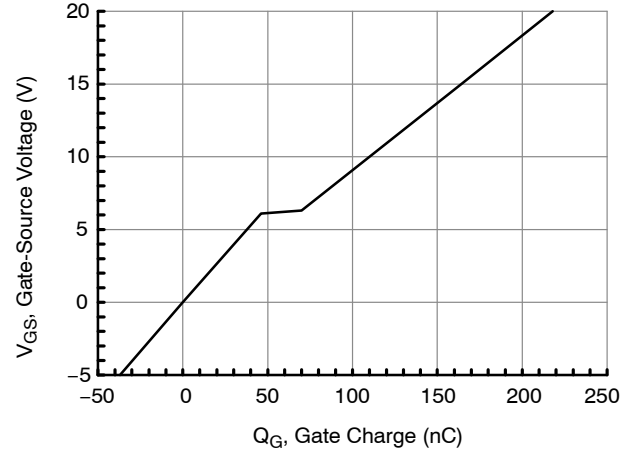


Figure 8. Typical Gate Charge at $V_{DS} = 400\text{ V}$ and $I_D = 80\text{ A}$

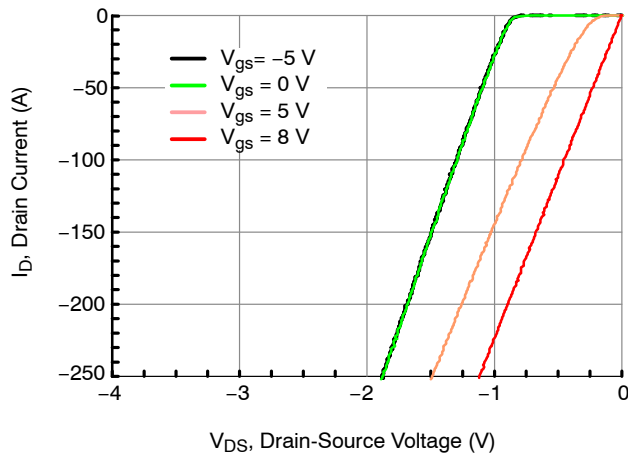


Figure 9. 3rd Quadrant Characteristics at $T_J = -55\text{ °C}$

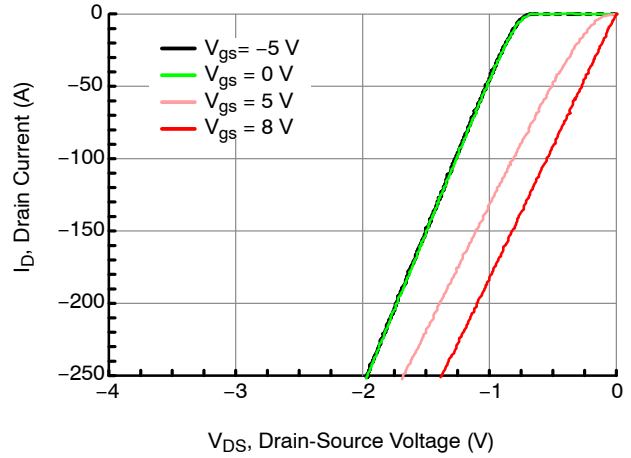


Figure 10. 3rd Quadrant Characteristics at $T_J = 25\text{ °C}$

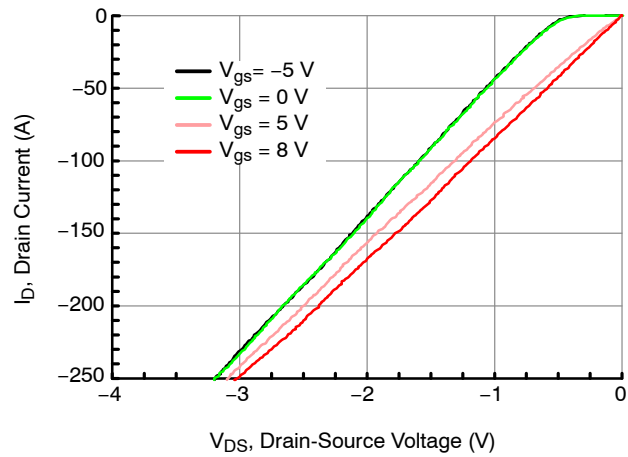


Figure 11. 3rd Quadrant Characteristics at $T_J = 175\text{ °C}$

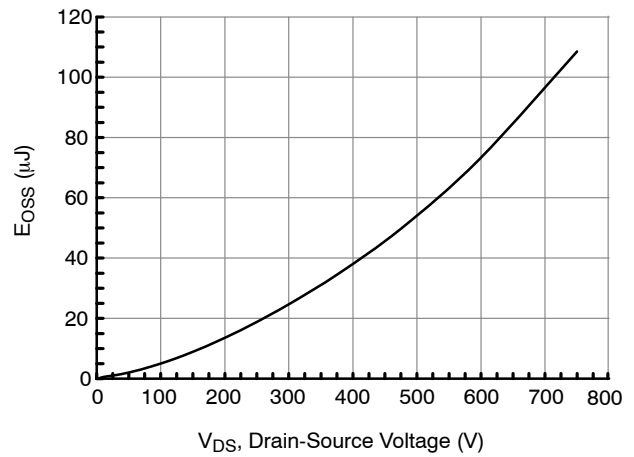


Figure 12. Typical Stored Energy in C_{OSS} at $V_{GS} = 0\text{ V}$

TYPICAL PERFORMANCE DIAGRAMS - MOSFET GATE AS CONTROL TERMINAL AND $V_{JGS} = 0 \text{ V}$

(continued)

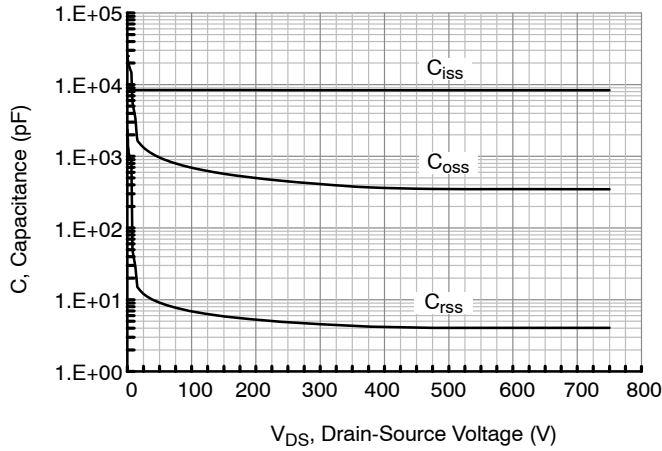


Figure 13. Typical Capacitances at $f = 100 \text{ kHz}$ and $V_{GS} = 0 \text{ V}$

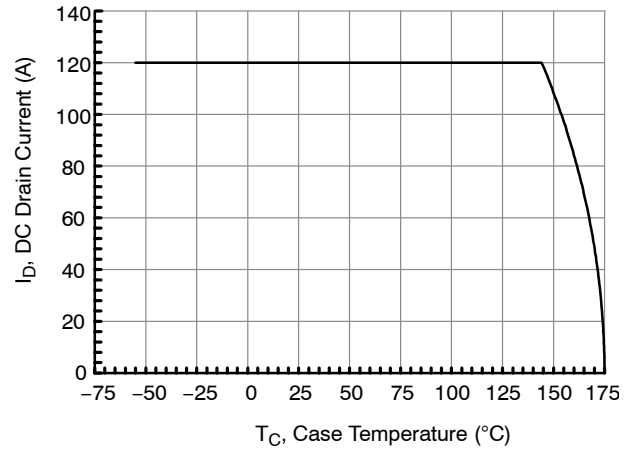


Figure 14. DC Drain Current Derating

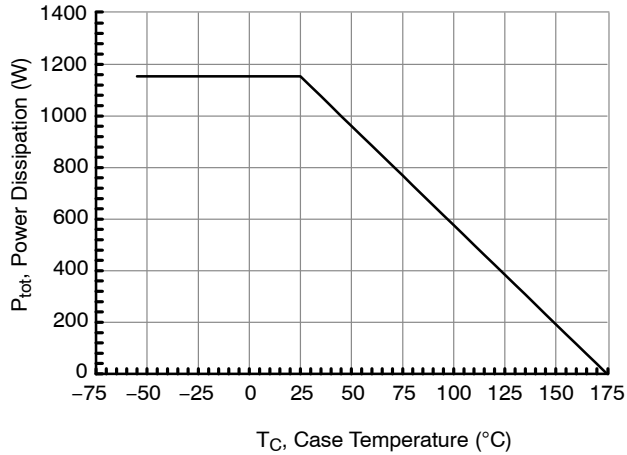


Figure 15. Total Power Dissipation

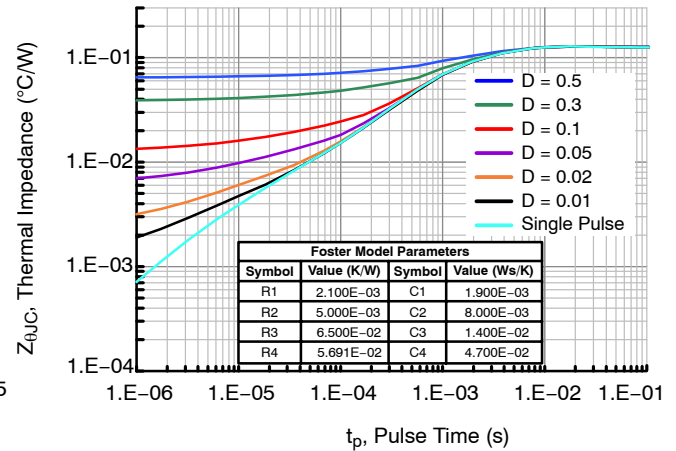


Figure 16. Maximum Transient Thermal Impedance

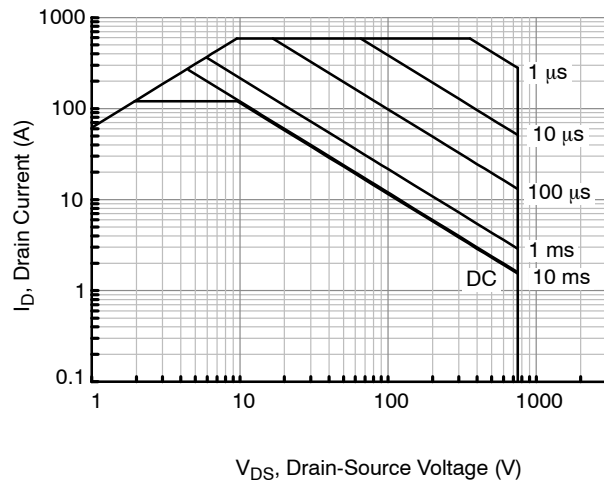


Figure 17. Safe Operation Area at $T_C = 25 \text{ °C}$, $D = 0$, Parameter t_p

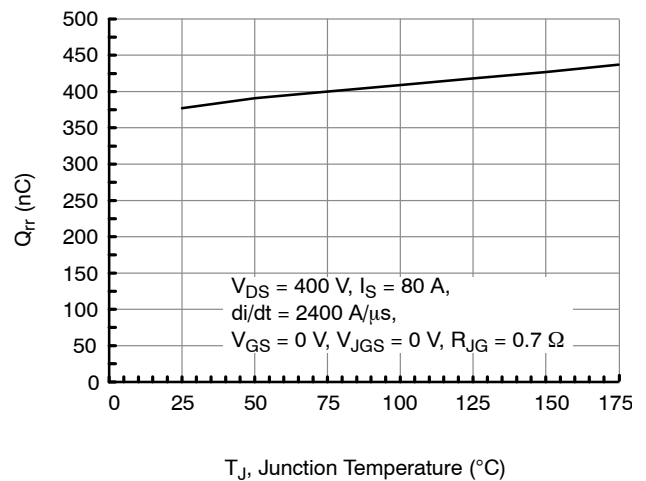


Figure 18. Reverse Recovery Charge Q_{rr} vs. Junction Temperature

TYPICAL PERFORMANCE DIAGRAMS - JFET GATE AS CONTROL TERMINAL AND $V_{GS} = +12\text{ V}$

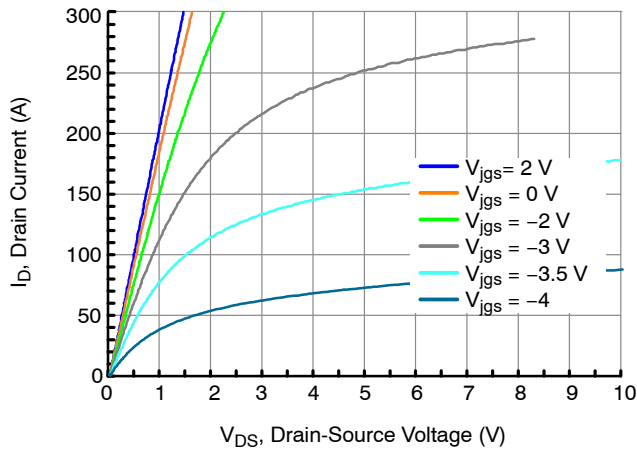


Figure 19. Typical Output Characteristics with JFET Gate as Control at $T_J = -55\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

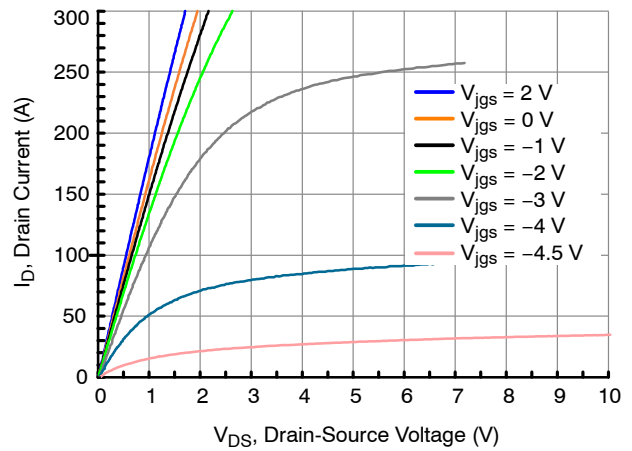


Figure 20. Typical Output Characteristics with JFET Gate as Control at $T_J = 25\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

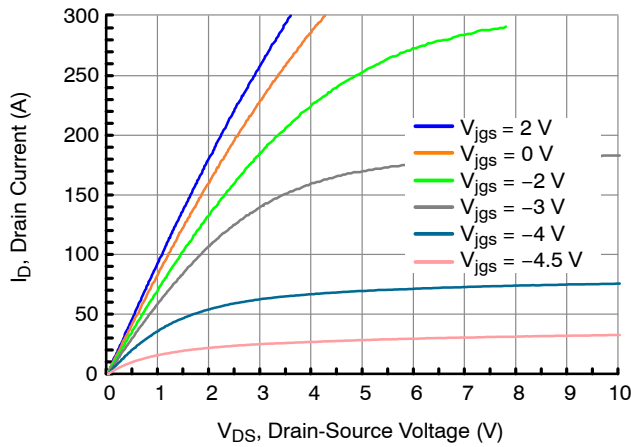


Figure 21. Typical Output Characteristics with JFET Gate as Control at $T_J = 175\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

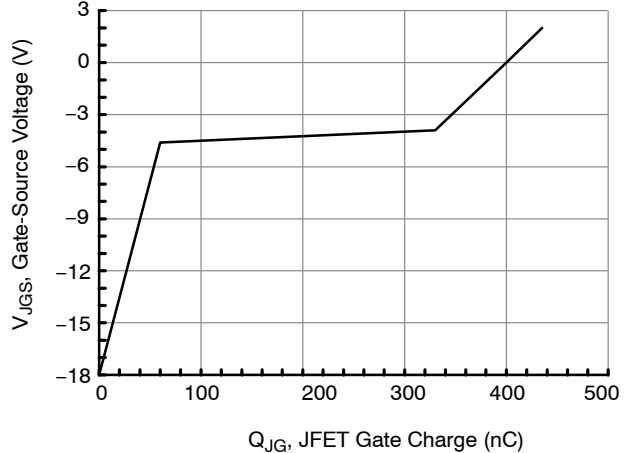


Figure 22. Typical JFET Gate Charge at $V_{DS} = 400\text{ V}$ and $I_D = 80\text{ A}$

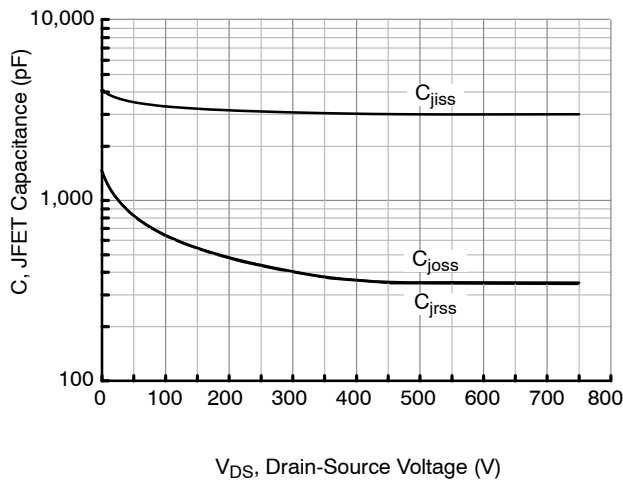


Figure 23. Typical JFET Capacitances at $f = 100\text{ kHz}$ and $V_{GS} = -20\text{ V}$

UG4SC075005L8S

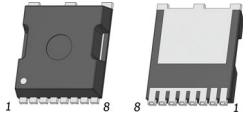
ORDERING INFORMATION

Part Number	Marking	Package	Shipping [†]
UG4SC075005L8S	UG4SC075005	H-PDSO-F8 (Pb-Free, Halogen Free)	2,000 / Tape and Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

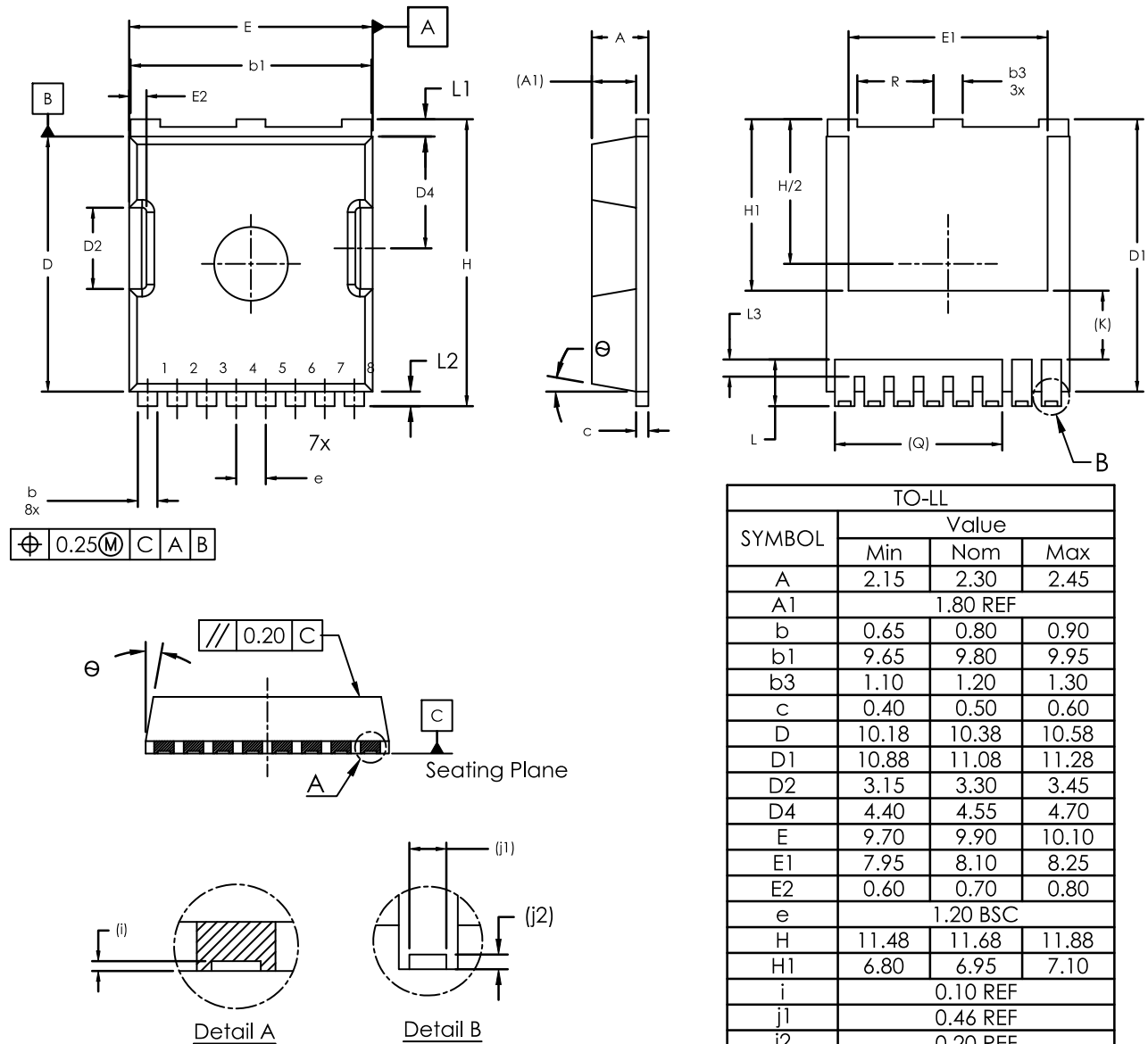
REVISION HISTORY

Revision	Description of Changes	Date
B	Acquired the original Qorvo JFET Division Data Sheet and updated the main document title to comply with onsemi standards for SiC products.	1/15/2025
2	Converted the Data Sheet to onsemi format.	5/26/2025



H-PDSO-F8 9.90x10.38x2.30, 1.20P
CASE 740AA
ISSUE A

DATE 22 APR 2025



Note:

1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling dimension : millimeters
3. Dimensions does not include Burrs and Mold Flashes

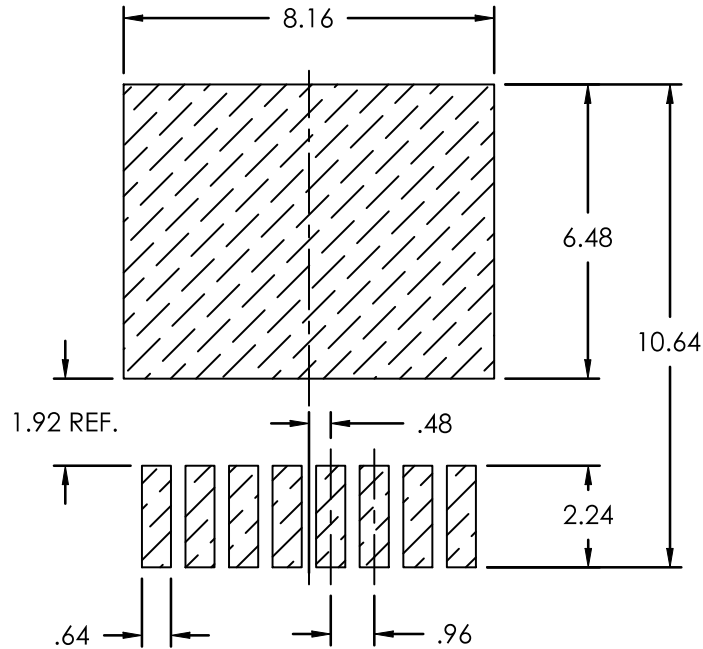
DOCUMENT NUMBER:	98AON26704H	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	H-PDSO-F8 9.90x10.38x2.30, 1.20P	PAGE 1 OF 2

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H-PDSO-F8 9.90x10.38x2.30, 1.20P
CASE 740AA
ISSUE A

DATE 22 APR 2025

RECOMMENDED PCB LAND PATTERN



NOTE: LAND PATTERN AND THROUGH HOLE DIMENSIONS SERVE ONLY AS AN INITIAL GUIDE.
END-USER PCB DESIGN RULES AND TOLERANCES SHOULD ALWAYS PREVAIL.

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