MOSFET – Power, N-Channel with ESD Protection

100 V, 1.33 A

NVNJWS0K9N10MCL

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D Max
100 V	1170 mΩ @ 10 V	1.33 A
	1820 mΩ @ 4.5 V	

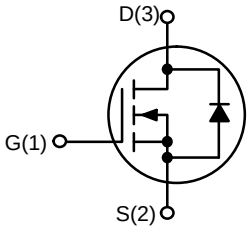
Features

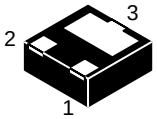
- Low $R_{DS(on)}$
- ESD Protected Gate
- AEC−Q101 Qualified and PPAP Capable
- Wettable Flank for Enhanced Optical Inspection
- This is a Pb−Free Device

Applications

- Load Switch

N−Channel





XDFNW3
CASE 521AC

MARKING DIAGRAM



M5 = Specific Device Code
M = Month Code

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	100	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	T_C = 25°C	I_D	1.33	A
		T_C = 100°C		0.94	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	4.66	W
		T_C = 100°C		2.33	
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	I_D	0.85	A
		T_A = 100°C		0.60	
Power Dissipation $R_{\theta JA}$ (Note 1)		T_A = 25°C	P_D	1.91	W
		T_A = 100°C		0.95	
Pulsed Drain Current	t_p = 10 μs		I_{DM}	10.18	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 175	°C
Source Current (Body Diode)			I_S	3.88	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Ambient – Steady State	$R_{\theta JA}$	79	°C/W
Junction−to−Case − Steady State	$R_{\theta JC}$	32.2	°C/W

1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		100	−	−	V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, ref to 25°C		−	73	−	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 80 V	T_J = 25°C	−	−	1.0	μA
			T_J = 125°C	−	−	100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V		−	−	±10	μA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 2 μA		1.0	−	3	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			−	−6.7	−	mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 370 mA		−	810	1170	mΩ
		V_{GS} = 4.5 V, I_D = 300 mA		−	1010	1820	
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 370 mA		−	0.88	−	S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 50 V		−	31	−	pF
Output Capacitance	C_{OSS}			−	7.9	−	
Reverse Transfer Capacitance	C_{RSS}			−	0.3	−	
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 50 V, I_D = 370 mA		−	0.9	−	nC
Threshold Gate Charge	$Q_{G(TH)}$			−	0.3	−	
Gate−to−Source Charge	Q_{GS}			−	0.4	−	
Gate−to−Drain Charge	Q_{GD}			−	0.2	−	
SWITCHING CHARACTERISTICS (Note 3)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DD} = 50 V, I_D = 370 mA, R_G = 2.5 Ω		−	3.4	−	ns
Rise Time	t_r			−	2.3	−	
Turn−Off Delay Time	$t_{d(off)}$			−	6.5	−	
Fall Time	t_f			−	9.2	−	
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 370 mA	T_J = 25°C	−	0.85	1.2	V
			T_J = 125°C	−	0.71	−	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

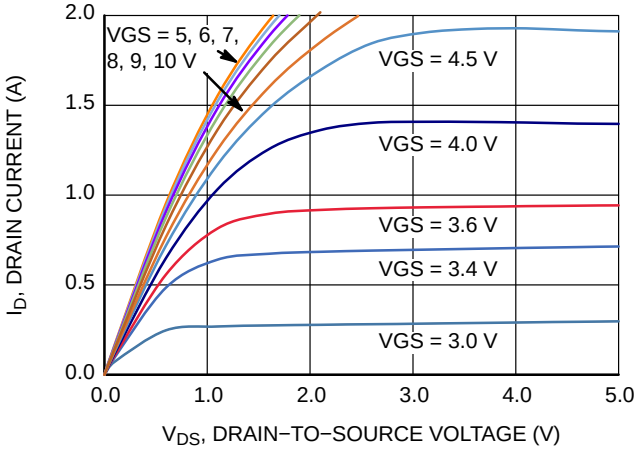


Figure 1. On−Region Characteristics

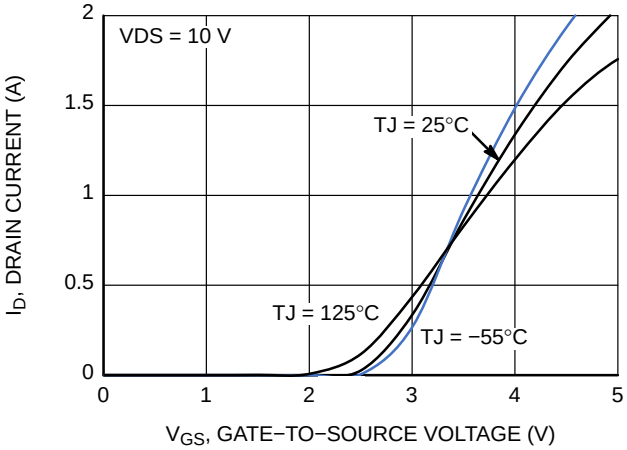


Figure 2. Transfer Characteristics

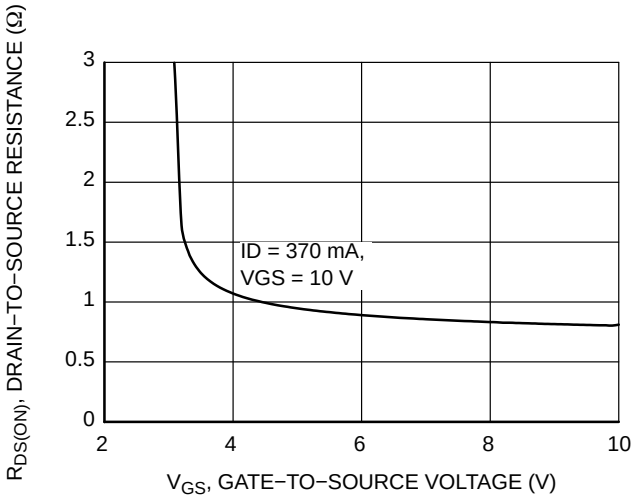


Figure 3. On−Resistance vs. Gate−to−Source Voltage

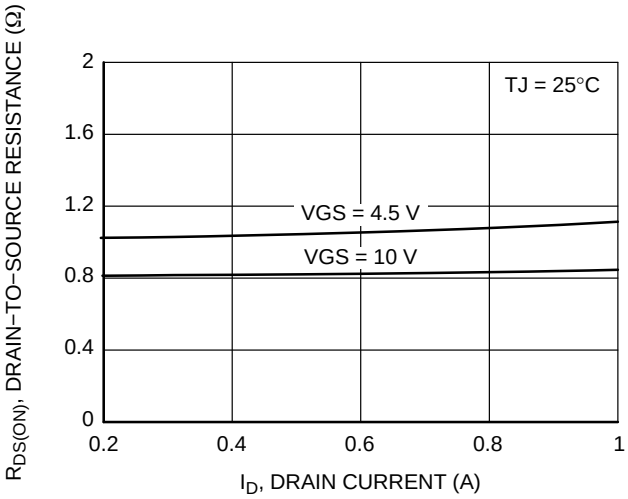


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

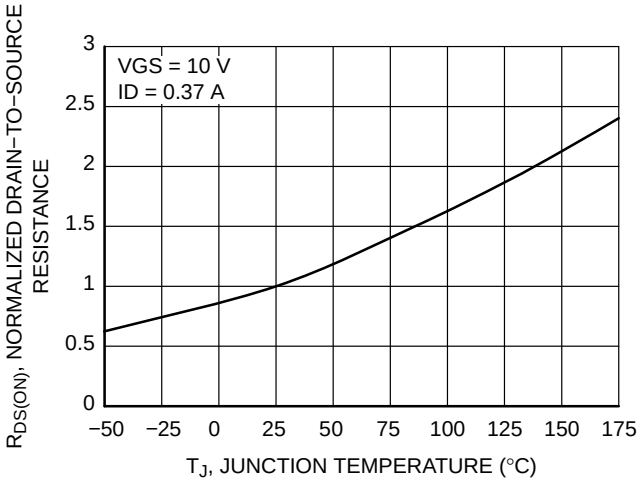


Figure 5. On−Resistance Variation with Temperature

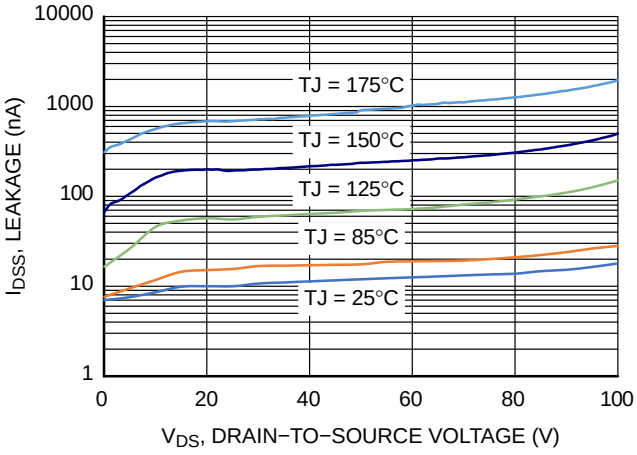


Figure 6. Drain−to−Source Leakage Current vs. Voltage

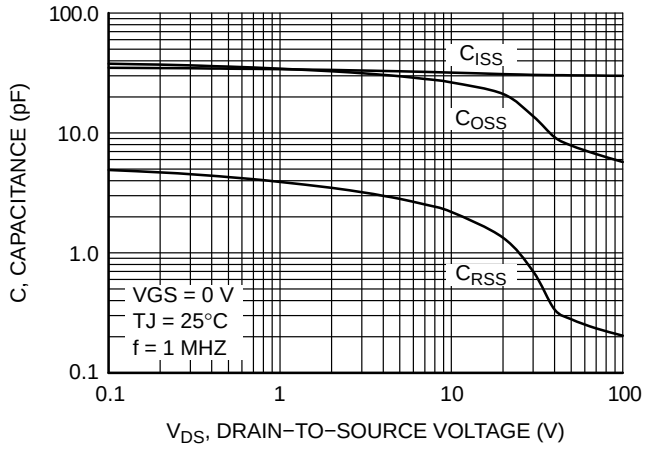


Figure 7. Capacitance Variation

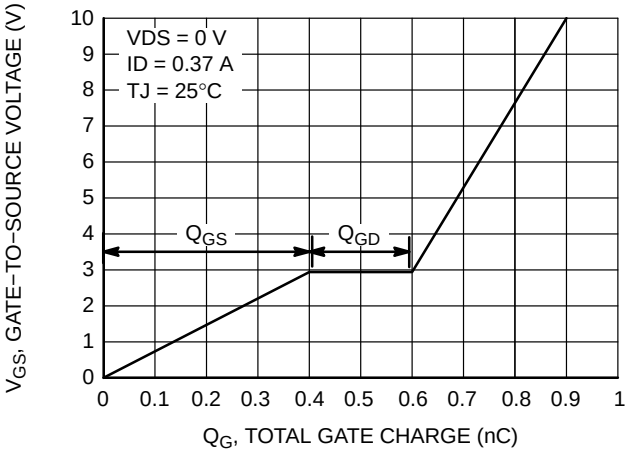


Figure 8. Gate−to−Source vs. Total Charge

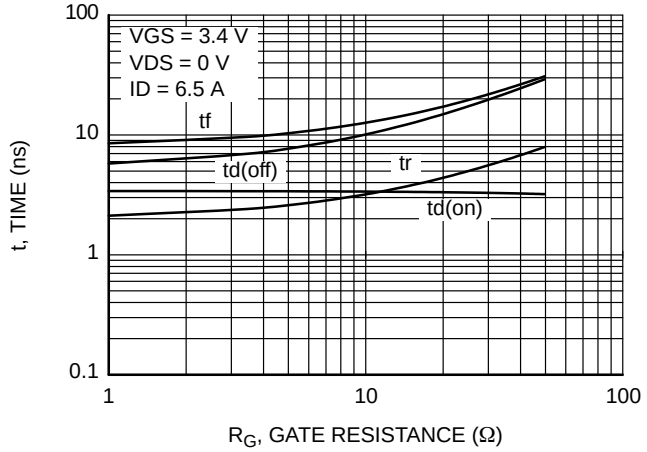


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

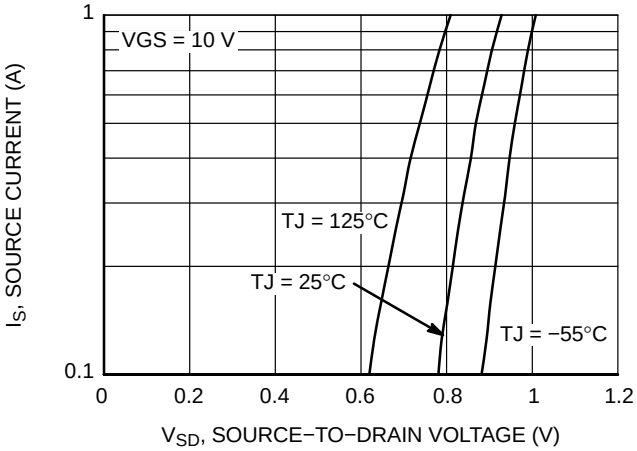


Figure 10. Diode Forward Voltage vs. Current

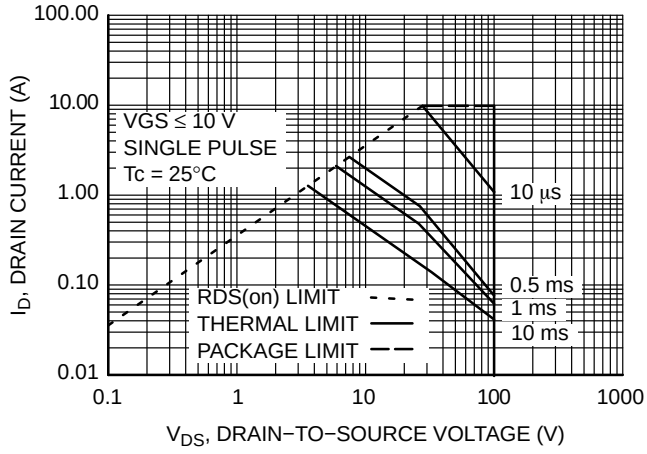


Figure 11. Maximum Rated Forward Biased Safe Operating Area

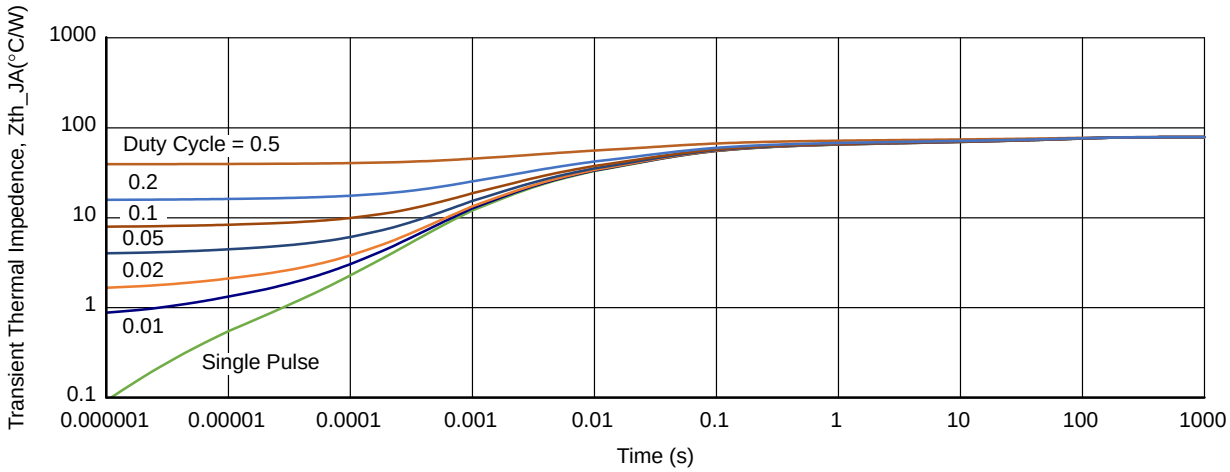
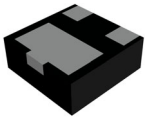


Figure 12. Thermal Characteristic

Table 1. ORDERING INFORMATION

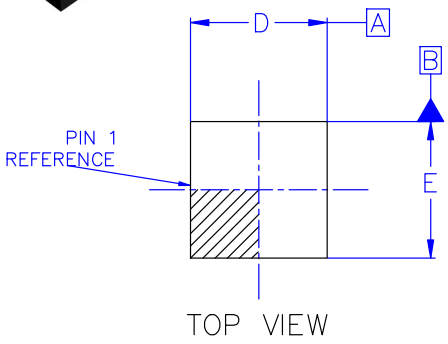
Part Number	Marking	Package	Shipping†
NVNJWS0K9N10MCLTAG	M5	XDFNW3 (Pb−Free)	3000 / Tape & Reel

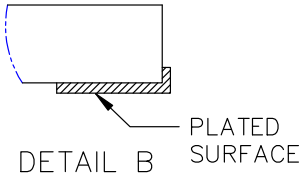
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

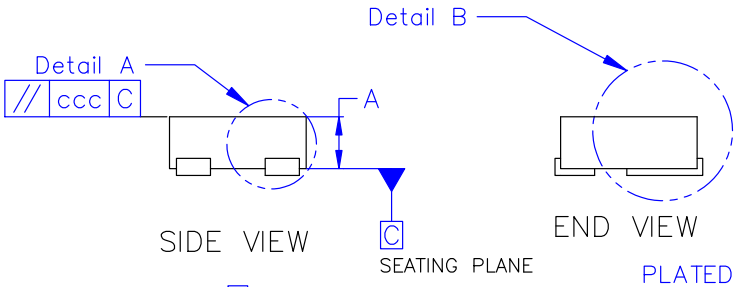


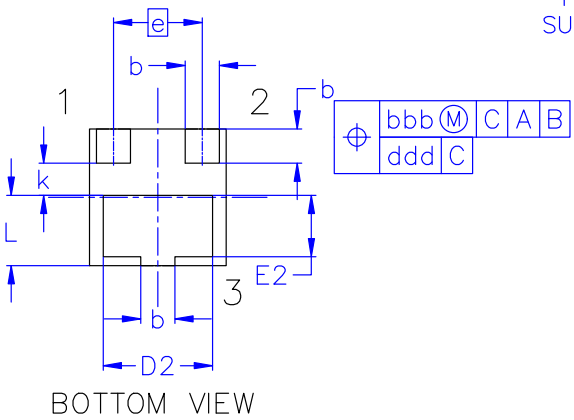
XDFNW−3 1.00x1.00x0.38 0.65P
CASE 521AC
ISSUE C

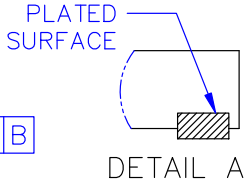
DATE 28 SEP 2026







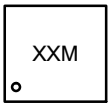




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS

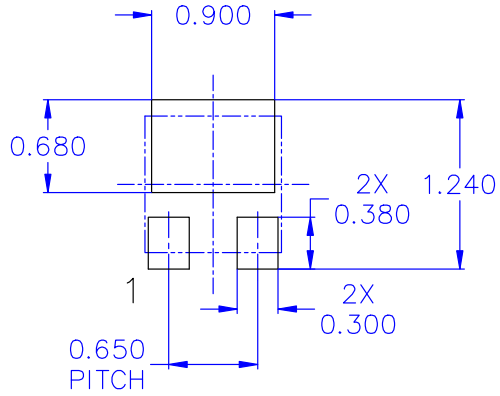
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.32	0.38	0.44
A1	0.00	---	0.04
A3		0.125 REF	
b	0.20	0.25	0.30
D	0.90	1.00	1.10
D1	0.00	---	0.04
D2	0.75	0.80	0.85
E	0.90	1.00	1.10
E2	0.40	0.45	0.50
e		0.65 BSC	
L	0.465	0.515	0.565
K		0.23 REF	
POSITION FORM & TOLERANCE			
ccc		0.05	
bbb		0.05	
ddd		0.03	

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT*

* For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON11341H**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**XDFNW−3 1.00x1.00x0.38 0.65P**		**PAGE 1 OF 1**

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