High Current IGBT Gate Driver

NCV5700

The NCV5700 is a high−current, high−performance stand−alone IGBT driver for high power applications that include solar inverters, motor control and uninterruptable power supplies. The device offers a cost−effective solution by eliminating many external components. Device protection features include Active Miller Clamp, accurate UVLO, EN input, DESAT protection and Active Low FAULT output. The driver also features an accurate 5.0 V output and separate high and low (VOH and VOL) driver outputs for system design convenience. The driver is designed to accommodate a wide voltage range of bias supplies including unipolar and bipolar voltages. It is available in a 16−pin SOIC package.

Features

- High Current Output (+4/−6 A) at IGBT Miller Plateau Voltages
- Low Output Impedance of VOH & VOL for Enhanced IGBT Driving
- Short Propagation Delays with Accurate Matching
- Direct Interface to Digital Isolator/Opto−coupler/Pulse Transformer for Isolated Drive, Logic Compatibility for Non−isolated Drive
- Active Miller Clamp to Prevent Spurious Gate Turn−on
- DESAT Protection with Programmable Delay
- Enable Input for Independent Driver Control
- Tight UVLO Thresholds for Bias Flexibility
- Wide Bias Voltage Range including Negative VEE Capability
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable, Grade 1
- This Device is Pb−Free, Halogen−Free and RoHS Compliant

Typical Applications

- Motor Control
- Uninterruptible Power Supplies (UPS)
- Automotive Power Supplies
- HEV/EV Powertrain
- HEV/EV PTC Heaters

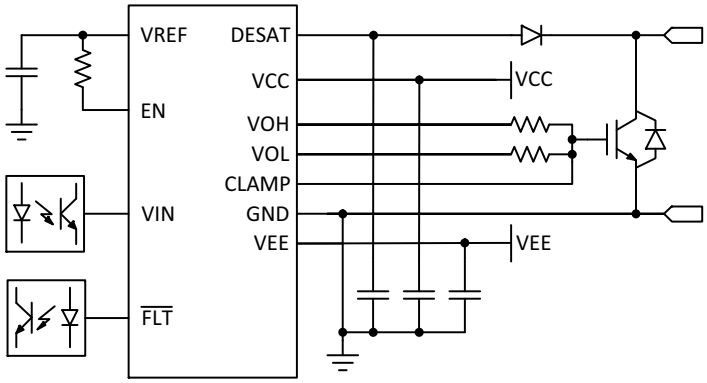
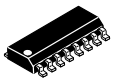


Figure 1. Simplified Application Schematic



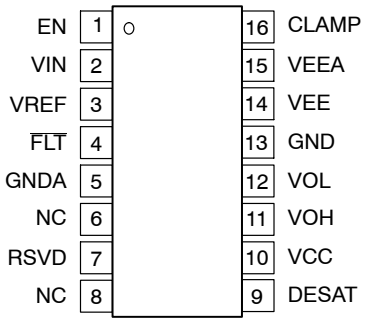
SOIC−16
D SUFFIX
CASE 751B

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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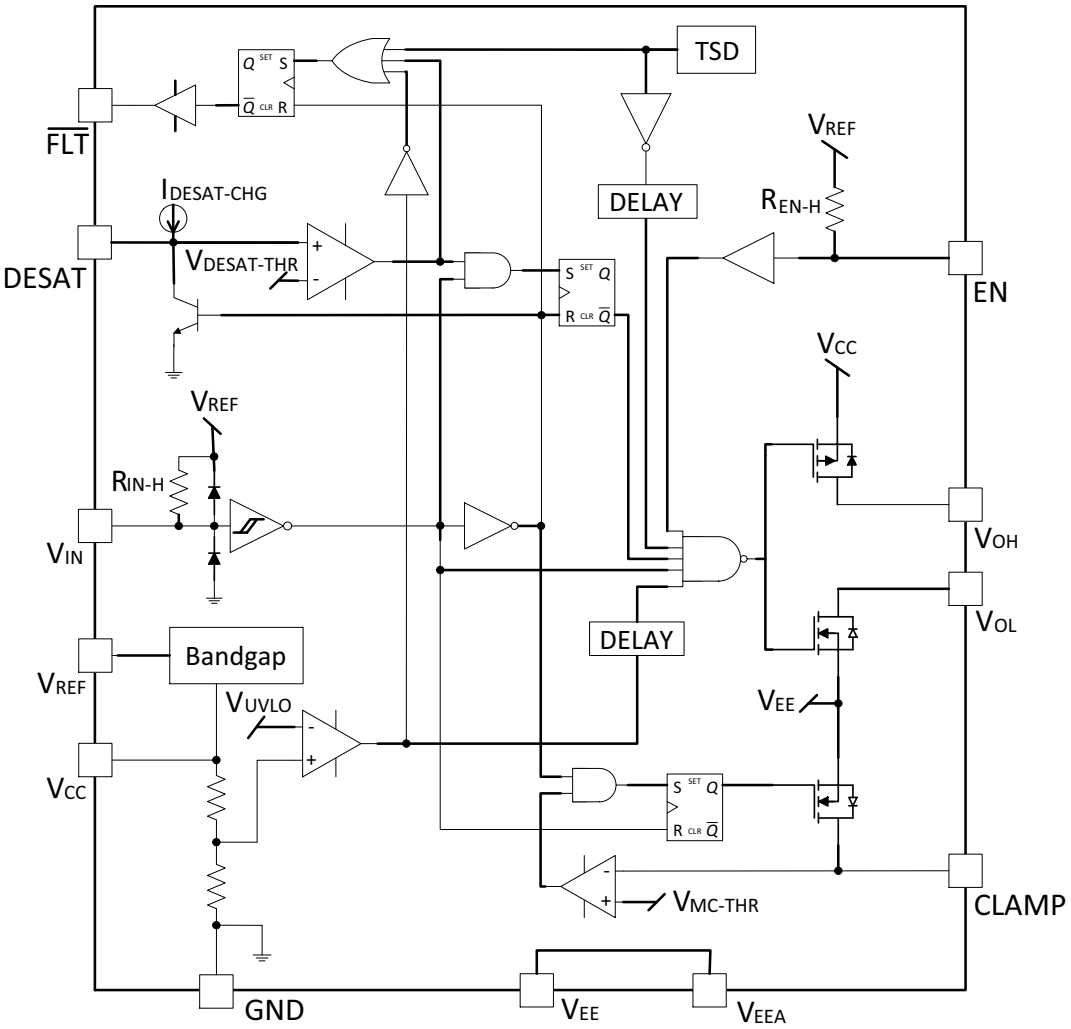

Figure 2. Detailed Block Diagram

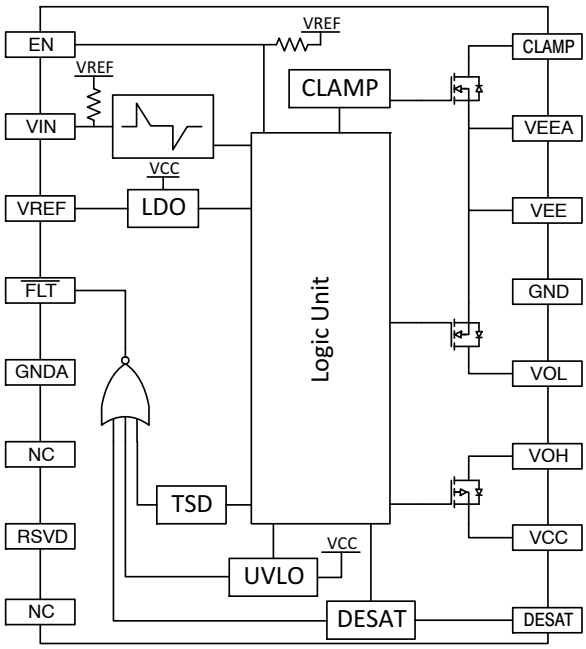

Figure 3. Simplified Block Diagram

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Table 1. PIN FUNCTION DESCRIPTION

Pin Name	No.	I/O/x	Description
EN	1	I	Enable input allows additional gating of VOH and VOL, and can be used when the driver output needs to be turned off independent of the Microcontroller input.
VIN	2	I	Input signal to control the output. In applications which require galvanic isolation, VIN is generated at the opto output, the pulse transformer secondary or the digital isolator output. There is a signal inversion from VIN to VOH/VOL. VIN is internally clamped to 5.5 V and has a pull−up resistor of 1 MΩ to ensure that output is low in the absence of an input signal. A minimum pulse−width is required at VIN before VOH/VOL are activated.
VREF	3	O	5 V Reference generated within the driver is brought out to this pin for external bypassing and for powering low bias circuits (such as digital isolators).
$\overline{\text{FLT}}$	4	O	Fault output (active low) that allows communication to the main controller that the driver has encountered a fault condition and has deactivated the output. Truth Table is provided in the datasheet to indicate conditions under which this signal is asserted. Capable of driving optos or digital isolators when isolation is required.
GNDA	5	x	This pin provides a convenient connection point for bypass capacitors (e.g REF) on the left side of the package.
NC	6,8	x	Pins not internally connected.
RSVD	7	x	Reserved. No connection is allowed.
DESAT	9	I	Input for detecting the desaturation of IGBT due to a fault condition. A capacitor connected to this pin allows a programmable blanking delay every ON cycle before DESAT fault is processed, thus preventing false triggering.
VCC	10	x	Positive bias supply for the driver. The operating range for this pin is from UVLO to the maximum. A good quality bypassing capacitor is required from this pin to GND and should be placed close to the pins for best results.
VOH	11	O	Driver high output that provides the appropriate drive voltage and source current to the IGBT gate.
VOL	12	O	Driver low output that provides the appropriate drive voltage and sink current to the IGBT gate. VOL is actively pulled low during start−up and under Fault conditions.
GND	13	x	This pin should connect to the IGBT Emitter with a short trace. All power pin bypass capacitors should be referenced to this pin and kept at a short distance from the pin.
VEE	14	x	A negative voltage with respect to GND can be applied to this pin and that will allow VOL to go to a negative voltage during OFF state. A good quality bypassing capacitor is needed from VEE to GND. If a negative voltage is not applied or available, this pin must be connected to GND.
VEEA	15	x	Analog version of the VEE pin for any signal trace connection. VEE and VEEA are internally connected.
CLAMP	16	I/O	Provides clamping for the IGBT gate during the off period to protect it from parasitic turn−on. To be tied directly to IGBT gate with minimum trace length for best results.

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Table 2. ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Minimum	Maximum	Unit
Differential Power Supply	V_{CC}–V_{EE} (V_{max})	0	36	V
Positive Power Supply	V_{CC}–GND	–0.3	22	V
Negative Power Supply	V_{EE}–GND	–18	0.3	V
Gate Output High	V_{OH}–GND		V_{CC} + 0.3	V
Gate Output Low	V_{OL}–GND	V_{EE} – 0.3		V
Input Voltage	V_{IN}–GND	–0.3	5.5	V
Enable Voltage	V_{EN}–GND	–0.3	5.5	V
DESAT Voltage	V_{DESAT}–GND	–0.3	V_{CC} + 0.3	V
$\overline{FLT}$ Current Sink Source	 $I_{\overline{FLT}-SINK}$ $I_{FLT-SRC}$		 20 25	mA
Power Dissipation SO–16 package	PD		 900	mW
Maximum Junction Temperature	$T_{J(max)}$		150	°C
Storage Temperature Range	TSTG		–65 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESDHBM		4	kV
ESD Capability, Machine Model (Note 2)	ESDMM		200	V
Moisture Sensitivity Level	MSL		1	–
Lead Temperature Soldering Reflow (SMD Styles Only), Pb–Free Versions (Note 3)	T_{SLD}		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC–Q100–002 (EIA/JESD22–A114)
   ESD Machine Model tested per AEC–Q100–003 (EIA/JESD22–A115)
   Latchup Current Maximum Rating: ≤ 100 mA per JEDEC standard: JESD78, 125°C
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 3. THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Characteristics, SOIC–16 (Note 4) Thermal Resistance, Junction–to–Air (Note 5)	 $R_{\theta JA}$	 145	°C/W

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
5. Values based on copper area of 100 mm^2 (or 0.16 in^2) of 1 oz copper thickness and FR4 PCB substrate.

Table 4. OPERATING RANGES (Note 6)

Parameter	Symbol	Min	Max	Unit
Differential Power Supply	V_{CC}–V_{EE} (V_{max})		30	V
Positive Power Supply	V_{CC}	UVLO	20	V
Negative Power Supply	V_{EE}	–15	0	V
Input Voltage	V_{IN}	0	5	V
Enable Voltage	V_{EN}	0	5	V
Input Pulse Width	t_{on}	40		ns
Ambient Temperature	T_A	–40	125	°C

6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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Table 5. ELECTRICAL CHARACTERISTICS V_{CC} = 15 V, V_{EE} = 0 V, Kelvin GND connected to V_{EE}. For typical values T_A = 25°C, for min/max values, T_A is the operating ambient temperature range that applies, unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
LOGIC INPUT and OUTPUT						
Input Threshold Voltages	Pulse−Width = 150 ns, V_{EN} = 5 V					V
High−state (Logic 1) Required	Voltage applied to get output to go low	V_{IN-H1}	4.3			
Low−state (Logic 0) Required	Voltage applied to get output to go high	V_{IN-L1}			0.75	
No state change	Voltage applied without change in output state	V_{IN-NC}	1.2		3.7	
Enable Threshold Voltages	V_{IN} = 0 V					V
High−state	Voltage applied to get output to go high	V_{EN-H}	4.3			
Low−state	Voltage applied to get output to go low	V_{EN-L}			0.75	
Input/Enable Internal Pull−Up Resistance to VREF		R_{IN-H}/ R_{EN-H}		1		MΩ
Input/Enable Current						μA
High−state	V_{IN-H}/V_{EN-H} = 4.5 V	I_{IN-H}/I_{EN-H}			1	
Low−state	V_{IN-L}/V_{EN-L} = 0.5 V	I_{IN-L}/I_{EN-L}			10	
Input Pulse−Width	Voltage thresholds consistent with input specs					ns
No Response at the Output		$t_{on-min1}$			10	
Guaranteed Response at the Output		$t_{on-min2}$	30			
$\overline{FLT}$ Threshold Voltage						V
Low State	($I_{\overline{FLT}-SINK}$ = 15 mA)	$V_{\overline{FLT}-L}$		0.5	1.0	
High State	($I_{\overline{FLT}-SRC}$ = 20 mA)	$V_{\overline{FLT}-H}$	12	13.9		
DRIVE OUTPUT						
Output Low State						V
	I_{sink} = 200 mA, T_A = 25°C	V_{OL1}		0.1	0.2	
	I_{sink} = 200 mA, T_A = −40°C to 125°C	V_{OL2}		0.2	0.5	
	I_{sink} = 1.0 A, T_A = 25°C	V_{OL3}		0.8	1.2	
Output High State						V
	I_{src} = 200 mA, T_A = 25°C	V_{OH1}	14.5	14.8		
	I_{src} = 200 mA, T_A = −40°C to 125°C	V_{OH2}	14.2	14.7		
	I_{src} = 1.0 A, T_A = 25°C	V_{OH3}	13.8	14.1		
Peak Driver Current, Sink (Note 7)	R_G = 0.1 Ω, V_{CC} = 15 V, V_{EE} = −8 V					A
	V_O = 13 V	$I_{PK-snk1}$		6.8		
	V_O = 9 V (near Miller Plateau)	$I_{PK-snk2}$		6.1		
Peak Driver Current, Source (Note 7)	R_G = 0.1 Ω, V_{CC} = 15 V, V_{EE} = −8 V					A
	V_O = −5 V	$I_{PK-src1}$		7.8		
	V_O = 9 V (near Miller Plateau)	$I_{PK-src2}$		4.0		
DYNAMIC CHARACTERISTICS						
Turn−on Delay (see timing diagram)	Negative input pulse width = 10 μs	t_{pd-on}	45	56	75	ns
Turn−off Delay (see timing diagram)	Positive input pulse width = 10 μs	t_{pd-off}	45	63	75	ns
Propagation Delay Distortion ($=t_{pd-on} - t_{pd-off}$)	For input or output pulse width > 150 ns,					ns
	T_A = 25°C	$t_{distort1}$	−15	−7	5	
	T_A = −40°C to 125°C	$t_{distort2}$	−25		25	
Prop Delay Distortion between Parts (Note 7)		$t_{distort\ -tot}$	−30	0	30	ns
Rise Time (Note 7) (see timing diagram)	C_{load} = 1.0 nF	t_{rise}		9.2		ns
Fall Time (Note 7) (see timing diagram)	C_{load} = 1.0 nF	t_{fall}		7.9		ns

7. Values based on design and/or characterization.

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Table 5. ELECTRICAL CHARACTERISTICS V_{CC} = 15 V, V_{EE} = 0 V, Kelvin GND connected to V_{EE}. For typical values T_A = 25°C, for min/max values, T_A is the operating ambient temperature range that applies, unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS						
Delay from $\overline{FLT}$ under UVLO/ TSD to VOL		t_{d1-OUT}	9	12	15	µs
Delay from DESAT to VOL (Note 7)		t_{d2-OUT}		220		ns
Delay from UVLO/TSD to $\overline{FLT}$ (Note 7)		$t_{d3-\overline{FLT}}$		7.3		µs
MILLER CLAMP						
Clamp Voltage	I_{sink} = 500 mA, T_A = 25°C I_{sink} = 500 mA, T_A = −40°C to 125°C	V_{clamp}		1.2	1.4 2.2	V
Clamp Activation Threshold		V_{MC-THR}	1.8	2.0	2.2	V
DESAT PROTECTION						
DESAT Threshold Voltage		$V_{DESAT-THR}$	6.0	6.35	7.0	V
Blanking Charge Current		$I_{DESAT-CHG}$	0.20	0.24	0.28	mA
Blanking Discharge Current		$I_{DESAT-DIS}$		30		mA
UVLO						
UVLO Startup Voltage		$V_{UVLO-OUT-ON}$	13.2	13.5	13.8	V
UVLO Disable Voltage		$V_{UVLO-OUT-OFF}$	12.2	12.5	12.8	V
UVLO Hysteresis		$V_{UVLO-HYST}$		1.0		V
VREF						
Voltage Reference	I_{REF} = 10 mA	V_{REF}	4.85	5.00	5.15	V
Reference Output Current (Note 7)		I_{REF}			20	mA
Recommended Capacitance		C_{VREF}	100			nF
SUPPLY CURRENT						
Current Drawn from V_{CC}	V_{CC} = 15 V Standby (No load on output, $\overline{FLT}$, VREF)	I_{CC-SB}		0.9	1.5	mA
Current Drawn from V_{EE}	V_{EE} = −10 V Standby (No load on output, $\overline{FLT}$, VREF)	I_{EE-SB}	−0.2	−0.14		mA
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 7)		T_{SD}		188		°C
Thermal Shutdown Hysteresis (Note 7)		T_{SH}		33		°C

7. Values based on design and/or characterization.

ORDERING INFORMATION

Device	Package	Shipping†
NCV5700DR2G	SO−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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TYPICAL CHARACTERISTICS

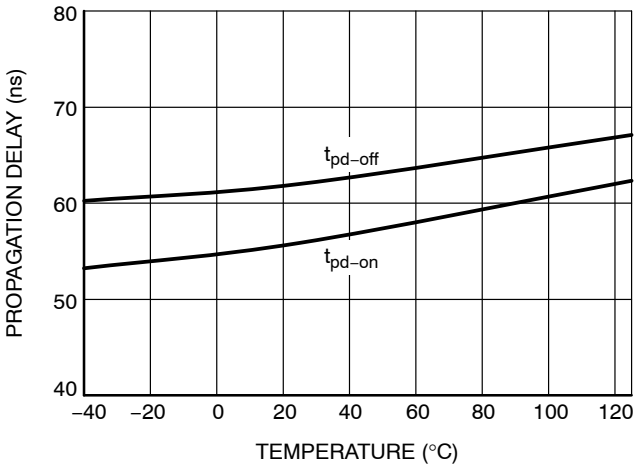

Figure 4. Propagation Delay vs. Temperature

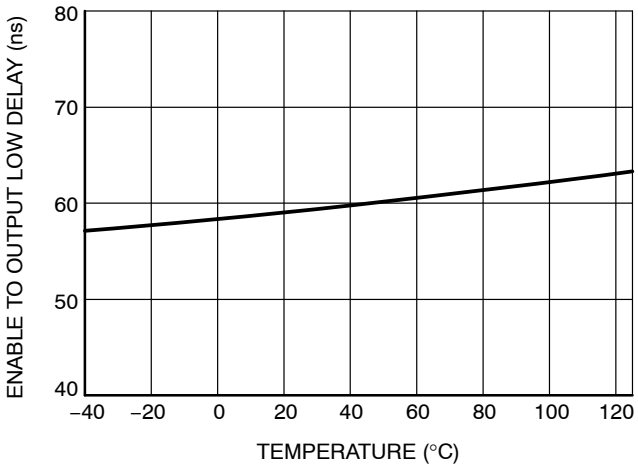

Figure 5. Enable to Output Low Delay

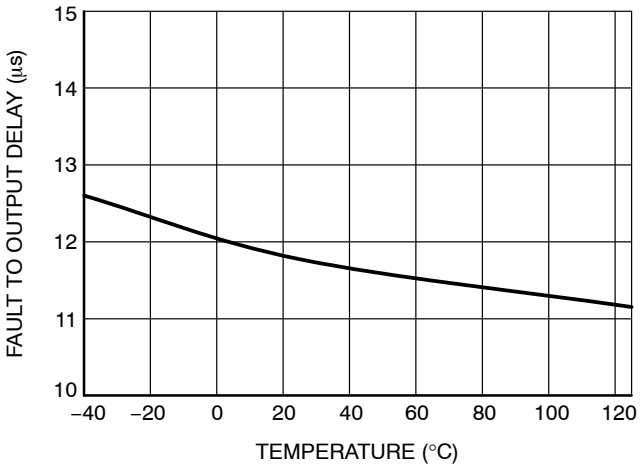

Figure 6. Fault to Output Low Delay

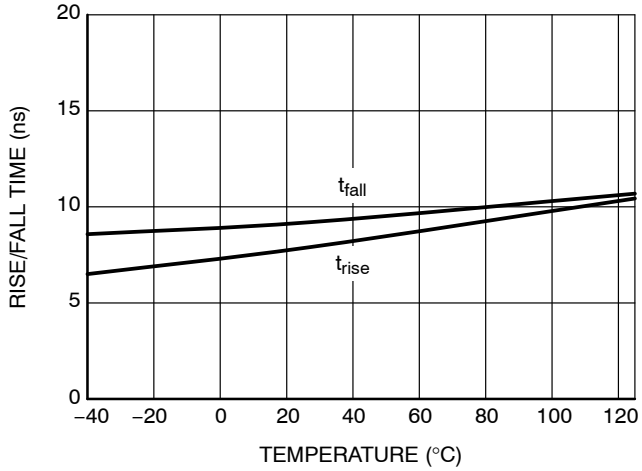

Figure 7. Output Rise/Fall Time

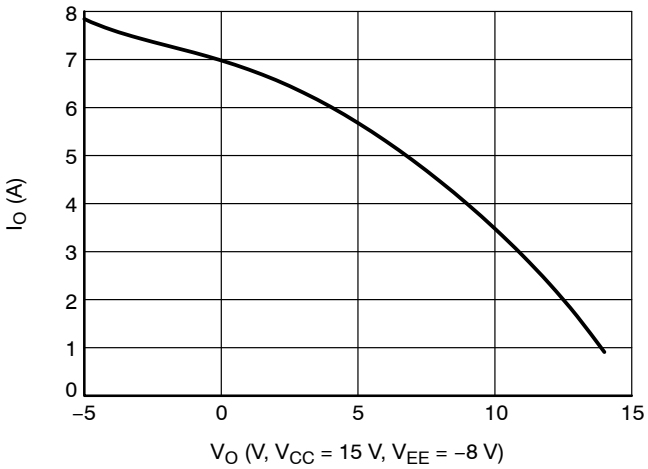

Figure 8. Output Source Current vs. Output Voltage

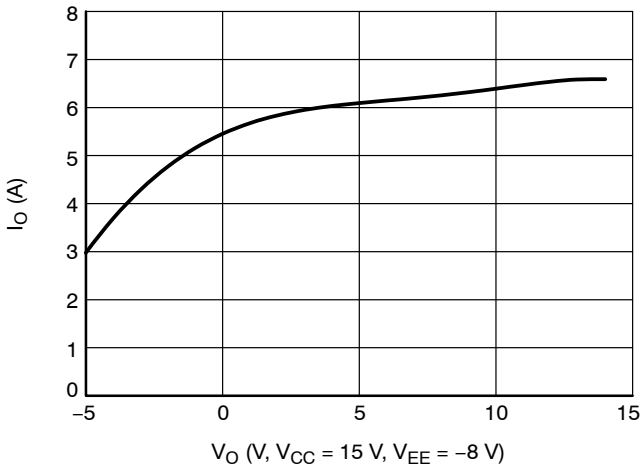

Figure 9. Output Sink Current vs. Output Voltage

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TYPICAL CHARACTERISTICS

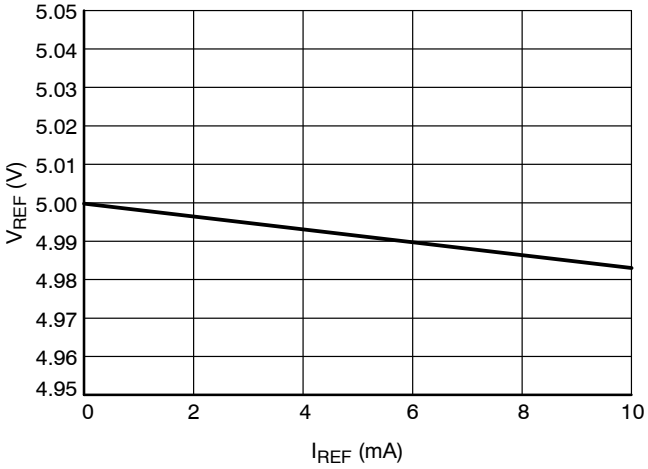

Figure 10. V_{REF} Voltage vs. Current

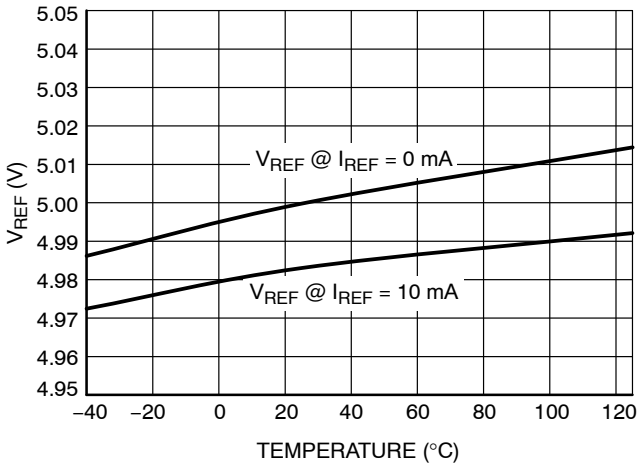

Figure 11. V_{CLAMP} at 0.5 A

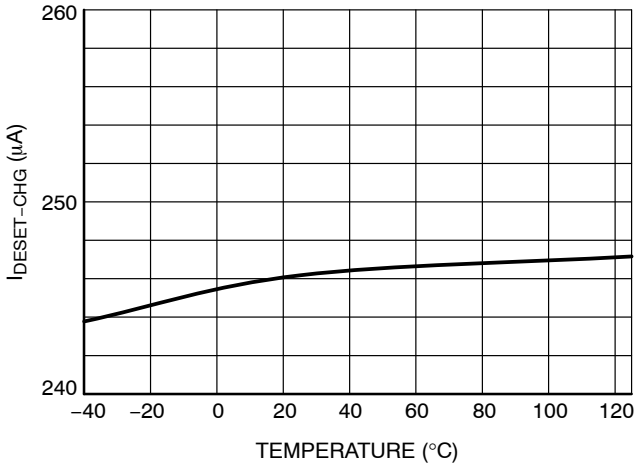

Figure 12. DESAT Charge Current vs. Temperature

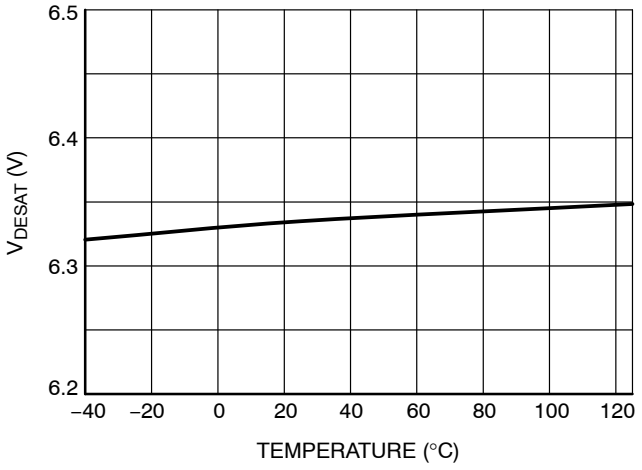

Figure 13. DESAT Threshold Voltage vs. Temperature

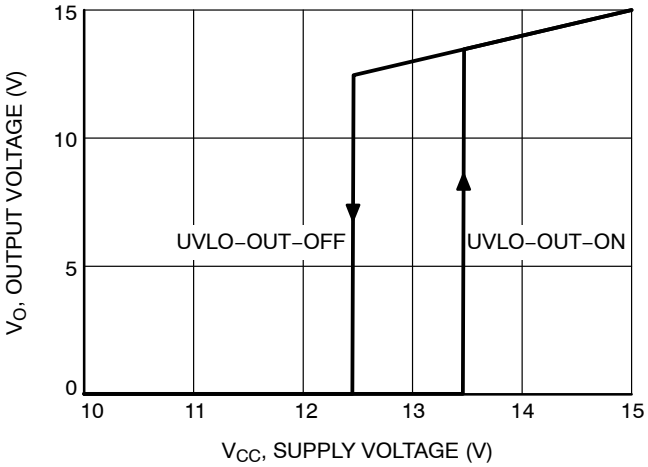

Figure 14. UVLO Threshold Voltages

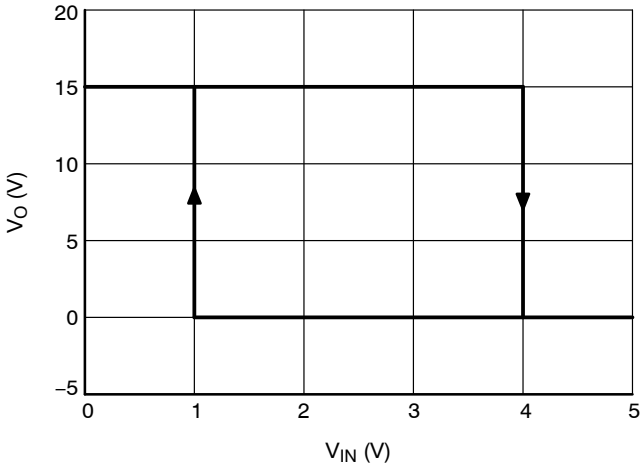

Figure 15. V_O vs. V_{IN} at 25°C (V_{CC} = 15 V, V_{EE} = 0 V)

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TYPICAL CHARACTERISTICS

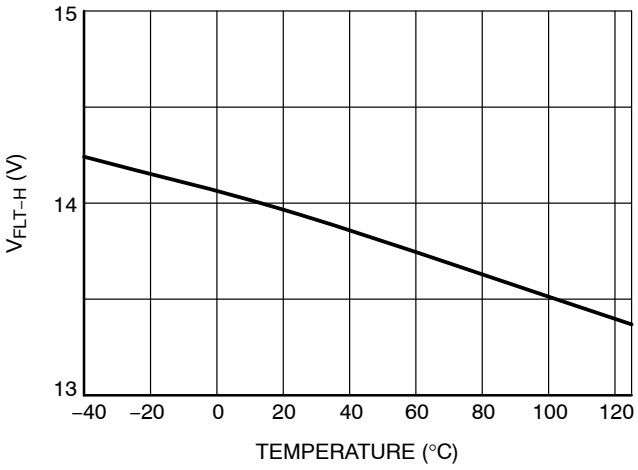

Figure 16. Fault Output, Sourcing 20 mA

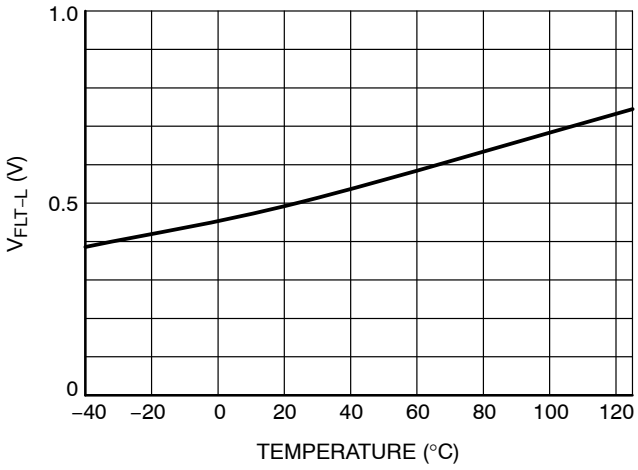

Figure 17. Fault Output, Sinking 15 mA

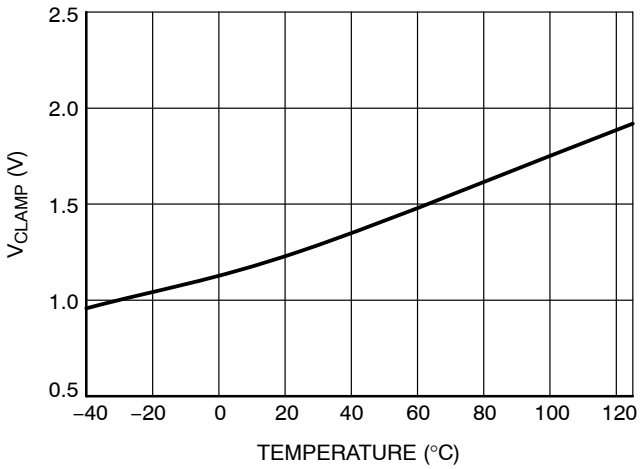

Figure 18. V_{CLAMP} at 0.5 A

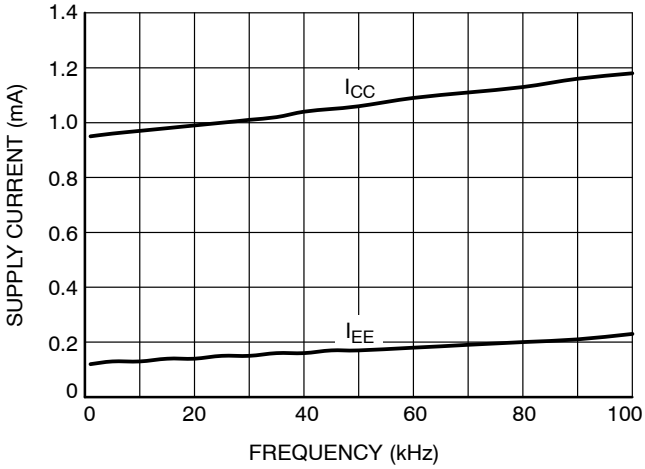

Figure 19. Supply Current vs. Switching Frequency (V_{CC} = 15 V, V_{EE} = −10 V, 25°C)

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APPLICATIONS AND OPERATING INFORMATION

This section lists the details about key features and operating guidelines for the NCV5700.

High Drive Current Capability

The NCV5700 driver family is equipped with many features which facilitate a superior performance IGBT driving circuit. Foremost amongst these features is the high drive current capability. The drive current of an IGBT driver is a function of the differential voltage on the output pin (V_{CC}−VOH for source current, VOL−V_{EE} for sink current) as shown in Figure 20. Figure 20 also indicates that for a given VOH/VOL value, the drive current can be increased by using higher V_{CC}/V_{EE} power supply). The drive current tends to drop off as the output voltage goes up (for turn−on event) or goes down (for turn−off event). As explained in many IGBT application notes, the most critical phase of IGBT switching event is the Miller plateau region where the gate voltage remains constant at a voltage (typically in 9−11 V range depending on IGBT design and the collector current), but the gate drive current is used to charge/discharge the Miller capacitance (C_{GC}). By providing a high drive current in this region, a gate driver can significantly reduce the duration of the phase and help reducing the switching losses. The NCV5700 addresses this requirement by providing and specifying a high drive current in the Miller plateau region. Most other gate driver ICs merely specify peak current at the start of switching – which may be a high number, but not very relevant to the application requirement. It must be remembered that other considerations such as EMI, diode reverse recovery performance, etc., may lead to a system level decision to trade off the faster switching speed against low EMI and reverse recovery. However, the use of NCV5700 does not preclude this trade−off as the user can always tune the drive current by employing external series gate resistor. Important thing to remember is that by providing a high internal drive current capability, the NCV5700 facilitates a wide range of gate resistors. Another value of the high current at the Miller plateau is that the initial switching transition phase is shorter and more controlled. Finally, the high gate driver current (which is facilitated by low impedance internal FETs), ensures that even at high switching frequencies, the power dissipation from the drive circuit is primarily in the external series resistor and more easily manageable. Experimental results have shown that the high current drive results in reduced turn−on energy (E_{ON}) for the IGBT switching.

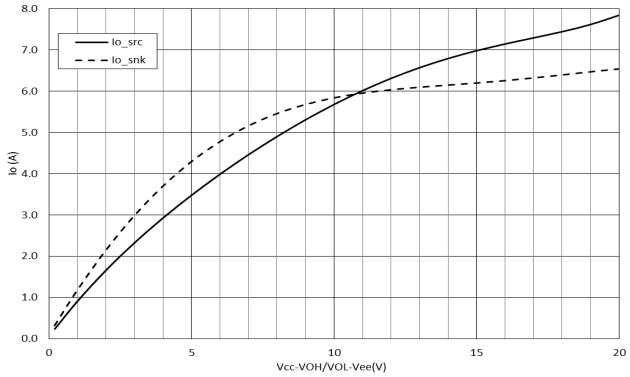

Figure 20. Output Current vs. Output Voltage Drop

When driving larger IGBTs for higher current applications, the drive current requirement is higher, hence lower R_G is used. Larger IGBTs typically have high input capacitance. On the other hand, if the NCV5700 is used to drive smaller IGBT (lower input capacitance), the drive current requirement is lower and a higher R_G is used. Thus, for most typical applications, the driver load RC time constant remains fairly constant. Caution must be exercised when using the NCV5700 with a very low load RC time constant. Such a load may trigger internal protection circuitry within the driver and disable the device. Figure 21 shows the recommended minimum gate resistance as a function of IGBT gate capacitance and gate drive trace inductance.

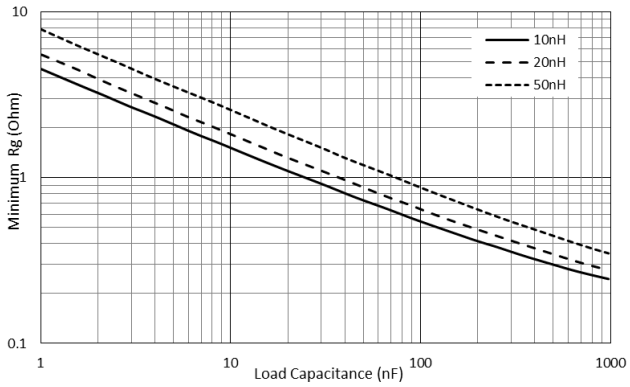

Figure 21. Recommended Minimum Gate Resistance as a Function of IGBT Gate Capacitance

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Gate Voltage Range

The negative drive voltage for gate (with respect to GND, or Emitter of the IGBT) is a robust way to ensure that the gate voltage does not rise above the threshold voltage due to the Miller effect. In systems where the negative power supply is available, the VEE option offered by NCV5700 allows not only a robust operation, but also a higher drive current for turn−off transition. Adequate bypassing between VEE pin and GND pin is essential if this option is used.

The V_{CC} range for the NCV5700 is quite wide and allows the user the flexibility to optimize the performance or use available power supplies for convenience.

Under Voltage Lock Out (UVLO)

This feature ensures reliable switching of the IGBT connected to the driver output. At the start of the driver's operation when V_{CC} is applied to the driver, the output remains turned−off. This is regardless of the signals on V_{IN} until the V_{CC} reaches the UVLO Output Enabled ($V_{UVLO-OUT-ON}$) level. After the V_{CC} rises above the $V_{UVLO-OUT-ON}$ level, the driver is in normal operation. The state of the output is controlled by signal at V_{IN}.

If the V_{CC} falls below the UVLO Output Disabled ($V_{UVLO-OUT-OFF}$) level during the normal operation of the driver, the Fault output is activated and the output is shut−down (after a delay) and remains in this state. The driver output does not start to react to the input signal on V_{IN} until the V_{CC} rises above the $V_{UVLO-OUT-ON}$ again. The waveform showing the UVLO behavior of the driver is in Figure 22.

In an IGBT drive circuit, the drive voltage level is important for drive circuit optimization. If $V_{UVLO-OUT-OFF}$ is too low, it will lead to IGBT being driven with insufficient gate voltage. A quick review of IGBT characteristics can reveal that driving IGBT with low voltage (in 10−12 V range) can lead to a significant increase in conduction loss. So, it is prudent to guarantee $V_{UVLO-OUT-OFF}$ at a reasonable level (above 12 V), so that the IGBT is not forced to operate at a non−optimum gate voltage. On the other hand, having a very high drive voltage ends up increasing switching losses without much corresponding reduction in conduction loss. So, the $V_{UVLO-OUT-ON}$ value should not be too high (generally, well below 15 V). These conditions lead to a tight band for UVLO enable and disable voltages, while guaranteeing a minimum hysteresis between the two values to prevent hiccup mode operation. The NCV5700 meets these tight requirements and ensures smooth IGBT operation. It ensures that a 15 V supply with ±8% tolerance will work without degrading IGBT performance, and guarantees that a fault will be reported and the IGBT will be turned off when the supply voltage drops below 12.2 V.

A UVLO event (V_{CC} voltage going below $V_{UVLO-OUT-OFF}$) also triggers activation of $\overline{FLT}$ output after a delay of t_{d3-FLT}. This indicates to the controller that the driver has encountered an issue and corrective action needs to be taken. However, a nominal delay t_{d1-OUT} = 12 μs is introduced between the initiation of the $\overline{FLT}$ output and actual turning off of the output. This delay provides adequate time for the controller to initiate a more orderly/sequenced shutdown. In case the controller fails to do so, the driver output shutdown ensures IGBT protection after t_{d1-OUT}.

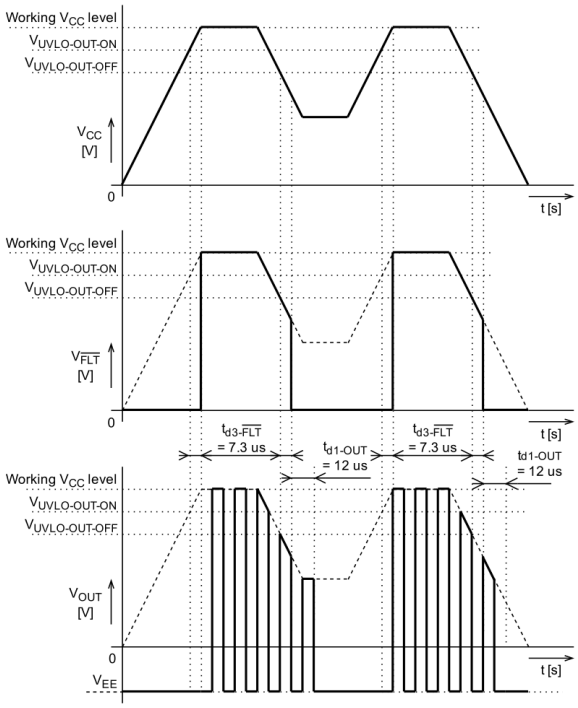

Figure 22. UVLO Function and Limits

Timing Delays and Impact on System Performance

The gate driver is ideally required to transmit the input signal pulse to its output without any delay or distortion. In the context of a high−power system where IGBTs are typically used, relatively low switching frequency (in tens of kHz) means that the delay through the driver itself may not be as significant, but the matching of the delay between different drivers in the same system as well as between different edges has significant importance. With reference to Figure 23(a), two input waveforms are shown. They are typical complementary inputs for high−side (HS) and low−side (LS) of a half−bridge switching configuration. The dead−time between the two inputs ensures safe transition between the two switches. However, once these inputs are through the driver, there is potential for the actual gate voltages for HS and LS to be quite different from the intended input waveforms as shown in Figure 23(a). The end result could be a loss of the intended dead−time and/or pulse−width distortion. The pulse−width distortion can create an imbalance that needs to be corrected, while the loss of dead−time can eventually lead to cross−conduction of the switches and additional power losses or damage to the system.

The NCV5700 driver is designed to address these timing challenges by providing a very low pulse−width distortion and excellent delay matching. As an example, the delay matching is guaranteed to $t_{DISTORT2}$ = ±25 ns while many of competing driver solutions can be >250 ns.

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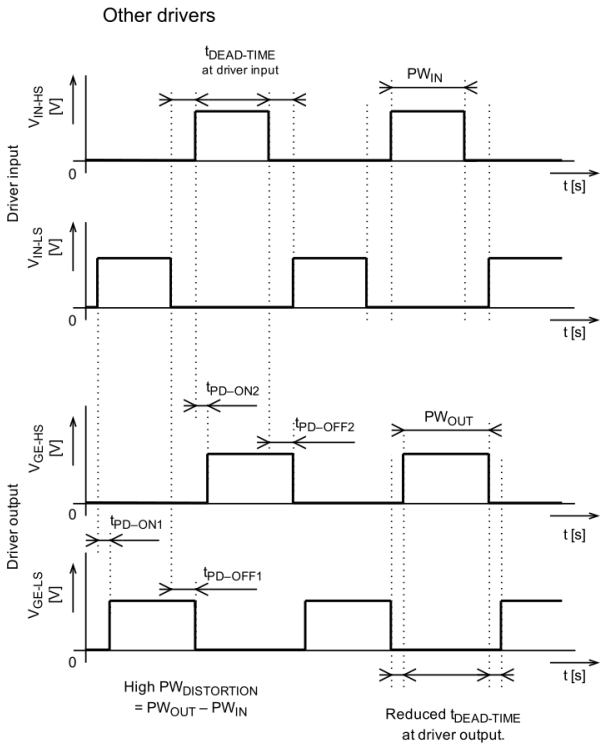

Figure 23(a). Timing Waveforms (Other Drivers)

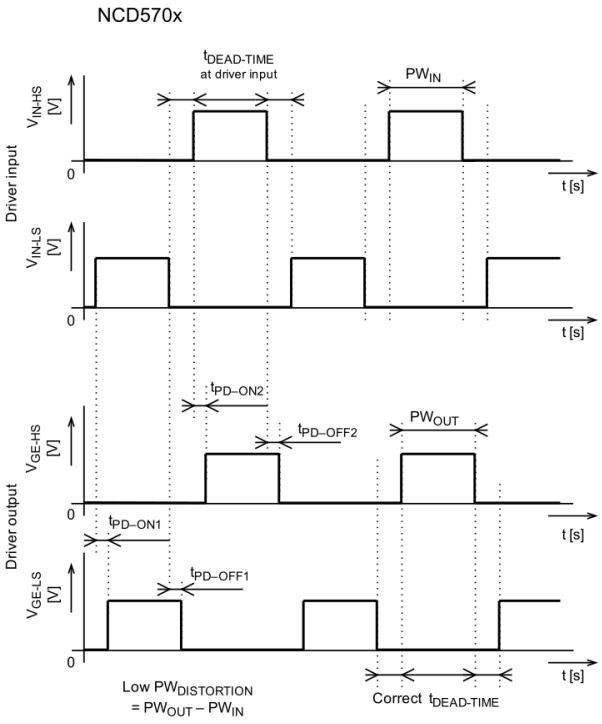

Figure 23(b). NCV5700 Timing Waveforms

Active Miller Clamp Protection

This feature is a cost savvy alternative to a negative gate voltage. The main requirement is to hold the gate of the turned−off (for example low−side) IGBT below the threshold voltage during the turn−on of the opposite−side (in this example high−side) IGBT in the half bridge. The turn−on of the high−side IGBT causes high dv/dt transition on the collector of the turned−off low−side IGBT. This high dv/dt then induces current (Miller current) through the C_{GC} capacitance (Miller capacitance) to the gate capacitance of the low−side IGBT as shown in Figure 24. If the path from gate to GND has critical impedance (caused by R_G) the Miller current could rise the gate voltage above the threshold level. As a consequence the low−side IGBT could be turned on for a few tens or hundreds of nanoseconds. This causes higher switching losses. One way to avoid this situation is to use negative gate voltage, but this requires second DC source for the negative gate voltage.

An alternative way is to provide an additional path from gate to GND with very low impedance. This is exactly what Active Miller Clamp protection does. Additional trace from the gate of the IGBT to the Clamp pin of the gate driver is introduced. After the V_O output has gone below the Active Miler Clamp threshold $V_{MC−THR}$ the Clamp pin is shorted to GND and thus prevents the voltage on the gate of the IGBT to rise above the threshold voltage as shown in Figure 25. The Clamp pin is disconnected from GND as soon as the signal to turn on the IGBT arrives to the gate driver input. The fact that the Clamp pin is engaged only after the gate voltage drops below the $V_{MC−THR}$ threshold ensures that the function of this pin does not interfere with the normal turn−off switching performance that is user controllable by choice of R_G.

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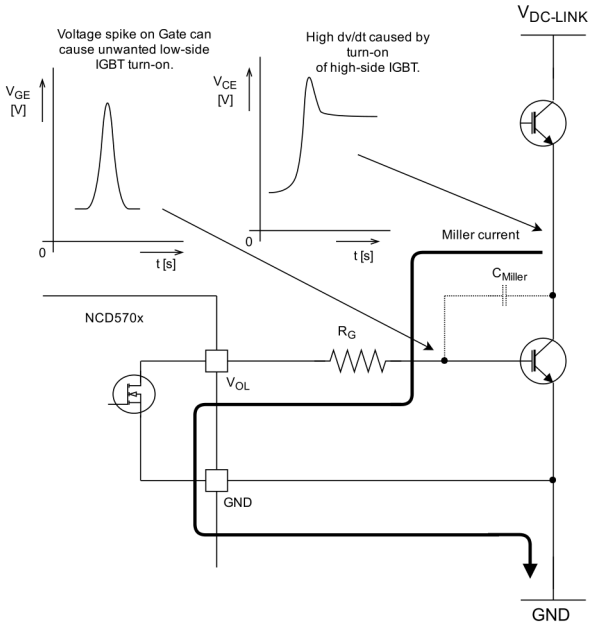

Figure 24. Current Path without Miller Clamp Protection

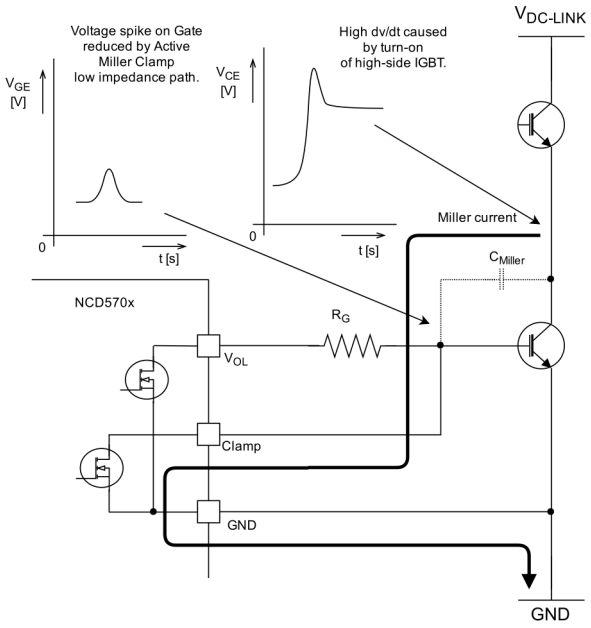

Figure 25. Current Path with Miller Clamp Protection

Desaturation Protection (DESAT)

This feature monitors the collector−emitter voltage of the IGBT in the turned−on state. When the IGBT is fully turned on, it operates in a saturation region. Its collector−emitter voltage (called saturation voltage) is usually low, well below 3 V for most modern IGBTs. It could indicate an overcurrent or similar stress event on the IGBT if the collector−emitter voltage rises above the saturation voltage, after the IGBT is fully turned on. Therefore the DESAT protection circuit compares the collector−emitter voltage with a voltage level $V_{DESAT-THR}$ to check if the IGBT didn't leave the saturation region. It will activate FLT output and shut down driver output (thus turn−off the IGBT), if the saturation voltage rises above the $V_{DESAT-THR}$. This protection works on every turn−on phase of the IGBT switching period.

At the beginning of turning−on of the IGBT, the collector−emitter voltage is much higher than the saturation voltage level which is present after the IGBT is fully turned on. It takes almost 1 μs between the start of the IGBT turn−on and the moment when the collector−emitter voltage falls to the saturation level. Therefore the comparison is delayed by a configurable time period (blanking time) to prevent false triggering of DESAT protection before the IGBT collector−emitter voltage falls below the saturation level. Blanking time is set by the value of the capacitor C_{BLANK}.

The exact principle of operation of DESAT protection is described with reference to Figure 26.

At the turned−off output state of the driver, the DESAT pin is shorted to ground via the discharging transistor (Q_{DIS}). Therefore, the inverting input holds the comparator output at low level.

At the turned−on output state of the driver, the current $I_{DESAT-CHG}$ from current source starts to flow to the blanking capacitor C_{BLANK}, connected to DESAT pin. Appropriate value of this capacitor has to be selected to ensure that the DESAT pin voltage does not rise above the threshold level $V_{DESAT-THR}$ before the IGBT fully turns on. The blanking time is given by following expression. According to this expression, a 47 pF C_{BLANK} will provide a blanking time of (47p *6.5/0.25m =) 1.22 μs.

$$t_{BLANK} = C_{BLANK} \cdot \frac{V_{DESAT-THR}}{I_{DESAT-CHG}}$$

After the IGBT is fully turned−on, the $I_{DESAT-CHG}$ flows through the DESAT pin to the series resistor $R_{S-DESAT}$ and through the high voltage diode and then through the collector and IGBT to the emitter. Care must be taken to select the resistor $R_{S-DESAT}$ value so that the sum of the saturation voltage, drop on the HV diode and drop on the $R_{S-DESAT}$ caused by current $I_{DESAT-CHG}$ flowing from DESAT source current is smaller than the DESAT threshold voltage. Following expression can be used:

$$V_{DESAT-THR} > R_{S-DESAT} \cdot I_{DESAT-CHG} + V_{F_HV\ diode} + V_{CESAT_IGBT}$$

Important part for DESAT protection to work properly is the high voltage diode. It must be rated for at least same voltage as the low side IGBT. The safety margin is application dependent.

The typical waveforms for IGBT overcurrent condition are outlined in Figure 27.

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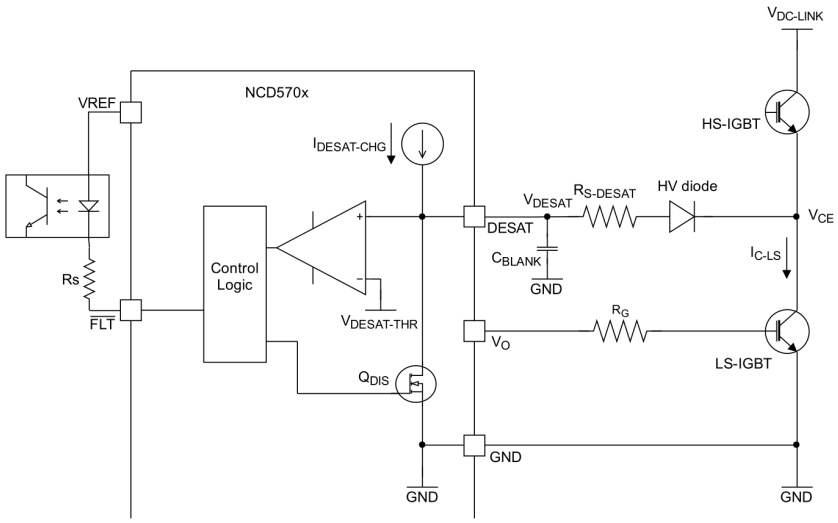

Figure 26. Desaturation Protection Schematic

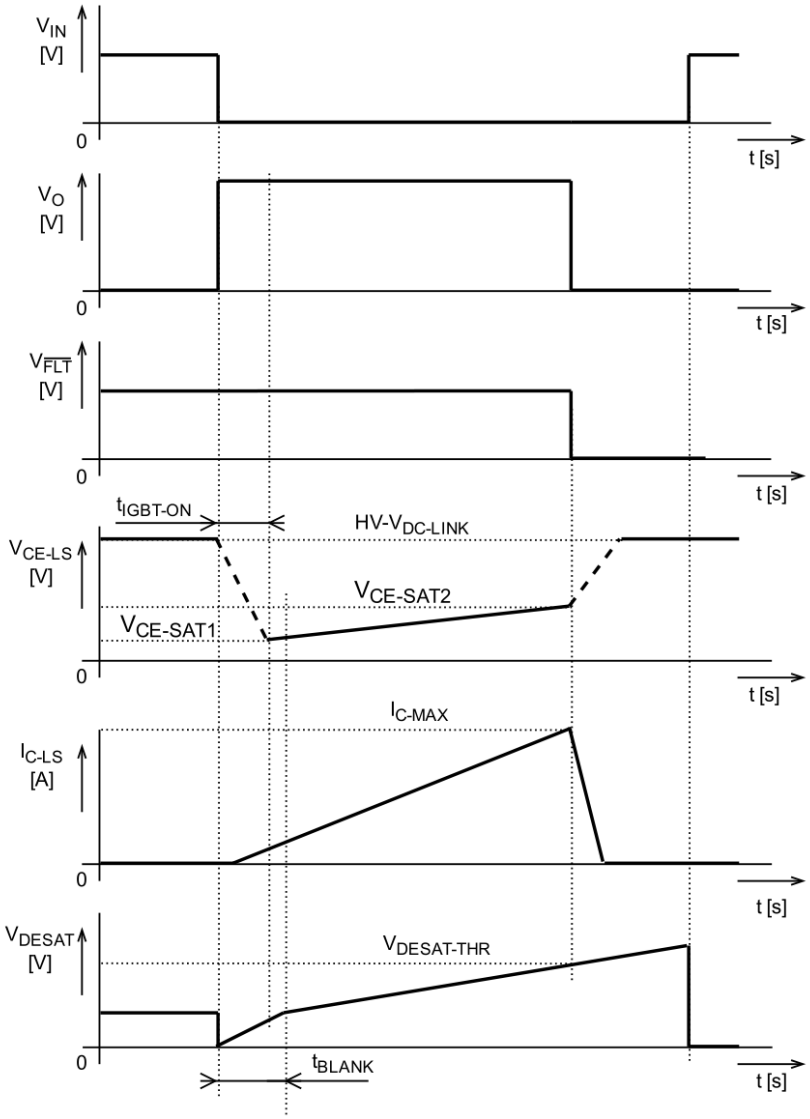

Figure 27. Desaturation Protection Waveforms

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Input Signal

The input signal controls the gate driver output. Figure 28 shows the typical connection diagrams for isolated applications where the input is coming through an opto−coupler or a pulse transformer.

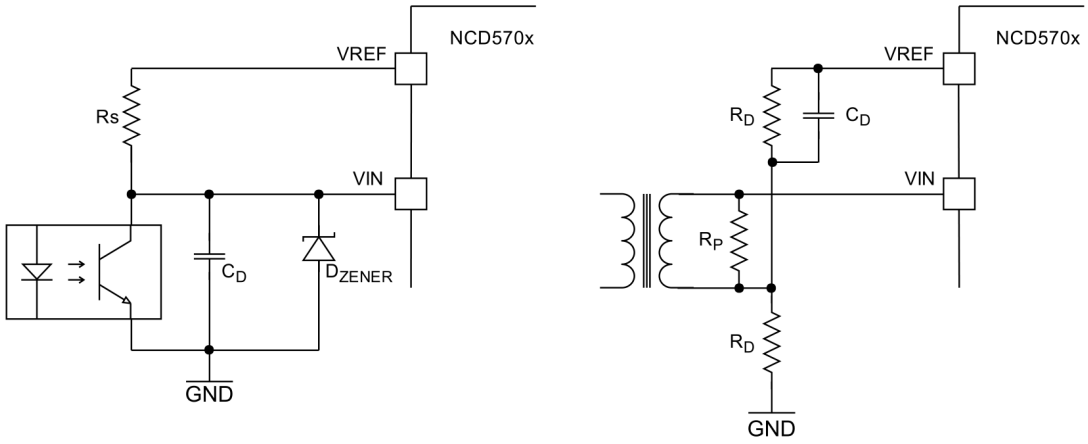

Figure 28. Opto−coupler or Pulse Transformer At Input

The relationship between gate driver input signal from a pulse transformer (Figure 29) or opto−coupler (Figure 30) and the output is defined by many time and voltage values. The time values include output turn−on and turn−off delays (t_{pd-on} and t_{pd-off}), output rise and fall times (t_{rise} and t_{fall}) and minimum input pulse−width (t_{on-min}). Note that the delay times are defined from 50% of input transition to first 10% of the output transition to eliminate the load dependency. The input voltage parameters include input high (V_{IN-H1}) and low (V_{IN-L1}) thresholds as well as the input range for which no output change is initiated (V_{IN-NC}).

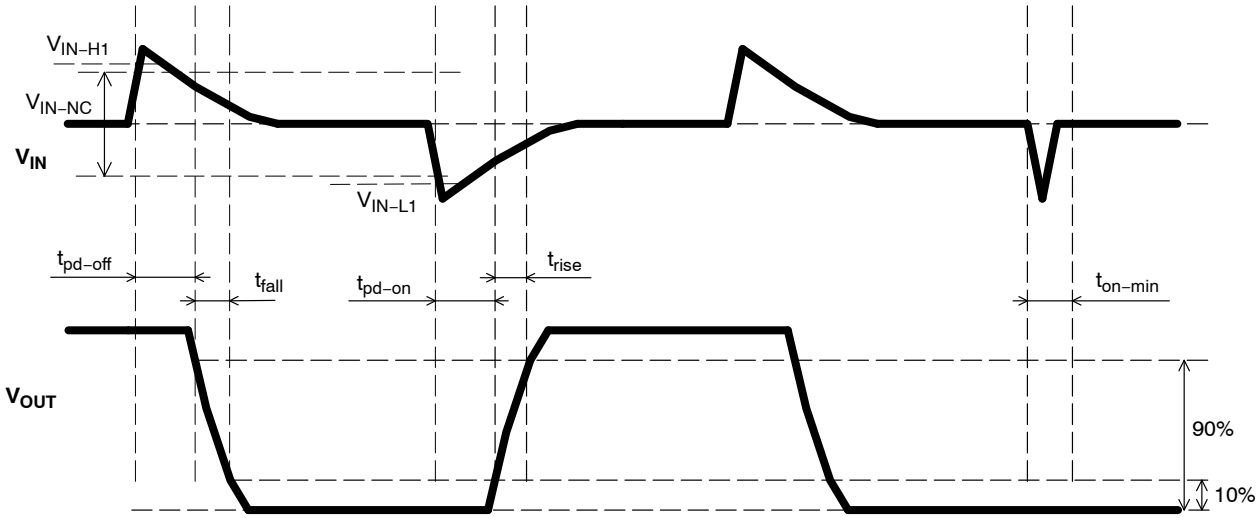

Figure 29. Input and Output Signal Parameters for Pulse Transformer

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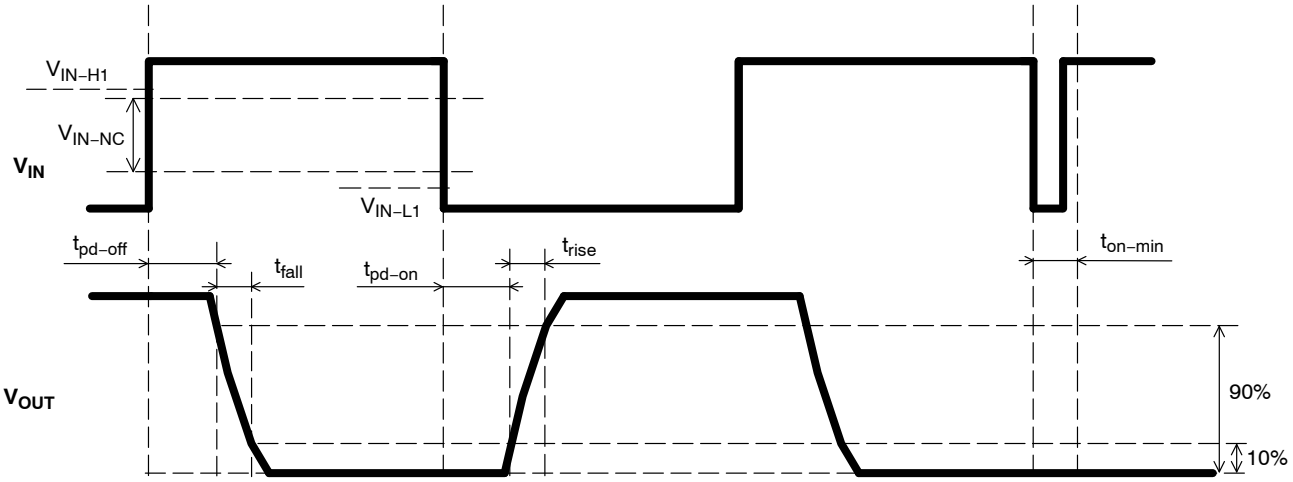

Figure 30. Input and Output Signal Parameters for Opto−coupler

Use of VREF Pin

The NCV5700 provides an additional 5.0 V output (VREF) that can serve multiple functions. This output is capable of sourcing up to 10 mA current for functions such as opto−coupler interface or external comparator interface. The VREF pin should be bypassed with at least a 100 nF capacitor (higher the better) irrespective of whether it is being utilized for external functionality or not. VREF is highly stable over temperature and line/load variations (*see characteristics curves for details*)

Fault Output Pin

This pin provides the feedback to the controller about the driver operation. The situations in which the $\overline{FLT}$ signal becomes active (low value) are summarized in the Table 6.

Table 6. $\overline{FLT}$ LOGIC TRUTH TABLE

VIN	ENABLE	UVLO	DESAT	Internal TSD	VOUT	$\overline{FLT}$	Notes
L	H	Inactive	L	L	H	H	Normal operation – Output High
H	H	Inactive	L	L	L	H	Normal operation – Output Low
X	L	Inactive	X	L	L	H	Disabled – Output Low, $\overline{FLT}$ High
X	X	Active	X	L	L	L	UVLO activated – $\overline{FLT}$ Low ($t_{d3\text{-}\overline{FLT}}$), Output Low ($t_{d3\text{-}\overline{FLT}} + t_{d1-OUT}$)
L	H	Inactive	H	L	L	L	DESAT activated (only when V_{IN} is low) – Output Low (t_{d2_OUT}), $\overline{FLT}$ Low
X	X	Inactive	X	H	L	L	Internal Thermal Shutdown – $\overline{FLT}$ Low ($t_{d3\text{-}\overline{FLT}}$), Output Low ($t_{d3\text{-}\overline{FLT}} + t_{d1-OUT}$)

Thermal Shutdown

The NCV5700 also offers thermal shutdown function that is primarily meant to self−protect the driver in the event that the internal temperature gets excessive. Once the temperature crosses the T_{SD} threshold, the $\overline{FLT}$ output is activated after a delay of $t_{d3\text{-}\overline{FLT}}$. After a delay of t_{d1-OUT} (12 μs), the output is pulled low and many of the internal circuits are turned off. The 12 μs delay is meant to allow the controller to perform an orderly shutdown sequence as appropriate. Once the temperature goes below the second threshold, the part becomes active again.

Additional Use of Enable Pin

For some applications, Enable is a useful feature as it provides the ability to shut down the power stage without involving the controls such as DSP. It can also be used along with the VREF pin and a comparator to provide local shutdown protection at fault conditions such as over temperature or over current, as illustrated in Figure 31.

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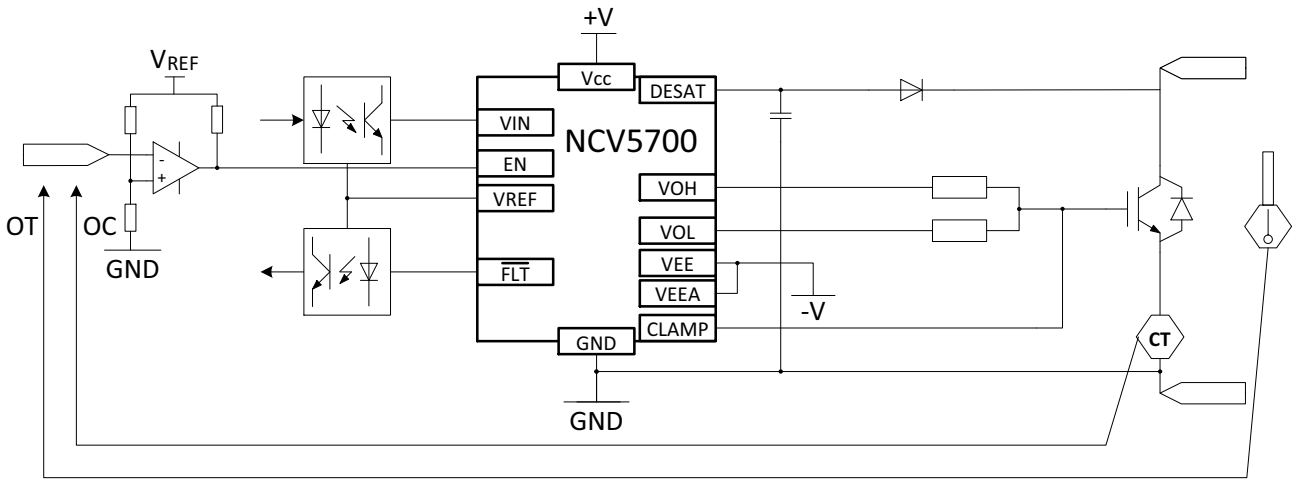

Figure 31. Additional Over Temperature and/or Over Current Shutdown Protection

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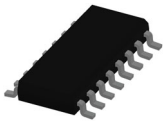

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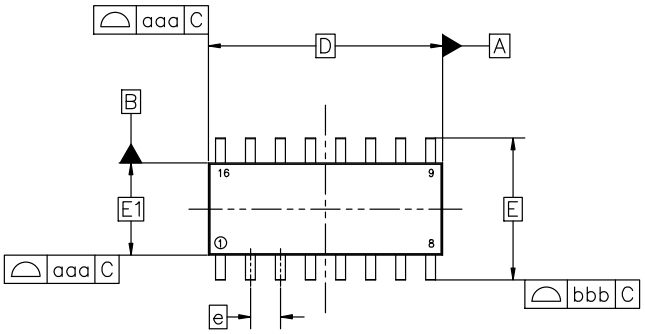
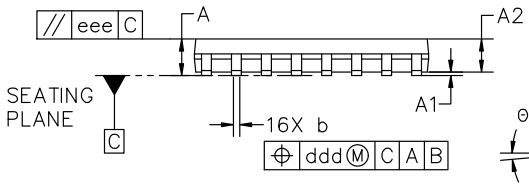
ISSUE M

DATE 18 OCT 2024

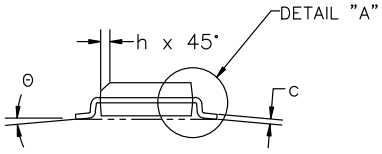
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



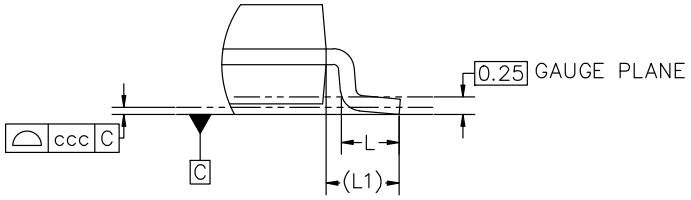
TOP VIEW



SIDE VIEW

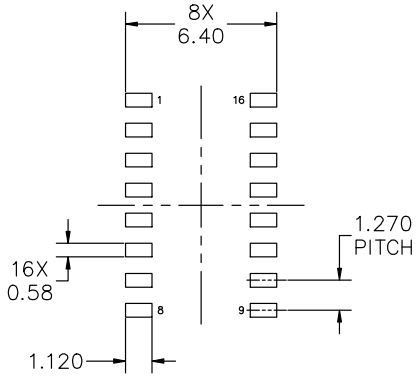


END VIEW



DETAIL "A"
Scale 3:1

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



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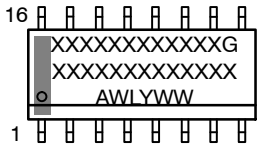
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN	
1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN	
1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN	
1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN	
1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

PIN	
1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

PIN	
1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

PIN	
1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH

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