LDO Regulator – Adjustable, Low Noise, Adjustable Current

3.3 V to 20 V

NCV47551

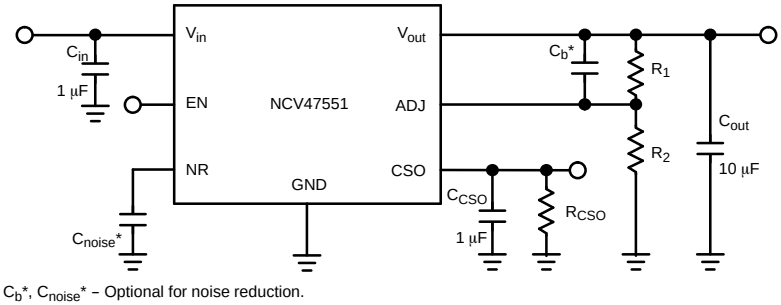
The NCV47551 is a low noise low output current integrated low dropout regulator designed for use in harsh automotive environments. It includes wide operating temperature and input voltage ranges. The device is offered with adjustable voltage versions available in 3% output voltage accuracy. It has a high peak input voltage tolerance and reverse input voltage protection. It also provides overcurrent protection, overtemperature protection and enable for control of the state of the output voltage. The integrated current sense feature provides diagnosis and system protection functionality. The current limit of the device is adjustable by resistor connected to CSO pin. Voltage on CSO pin is proportional to output current.

Features

- Adjustable Voltage Version (from 3.3 V to 20 V) ± 3% Output Voltage
- Enable Input (3.3 V Logic Compatible Thresholds)
- Adjustable Current Limit (from 100 μA to 20 mA) with 10% Accuracy
- Protection Features:
  - Current Limitation
  - Thermal Shutdown
  - Reverse Input Voltage
- This is a Pb–Free Device

Typical Applications

- Microphone Power Supply
- Audio and Infotainment System
- Navigation
- Satellite Radio



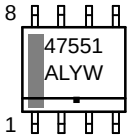
C_b*, C_{noise}* – Optional for noise reduction.

Figure 1. Application Schematic
(See Application Section for more details)

MARKING DIAGRAM



SOIC–8
SUFFIX D
CASE 751



47551	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb–Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

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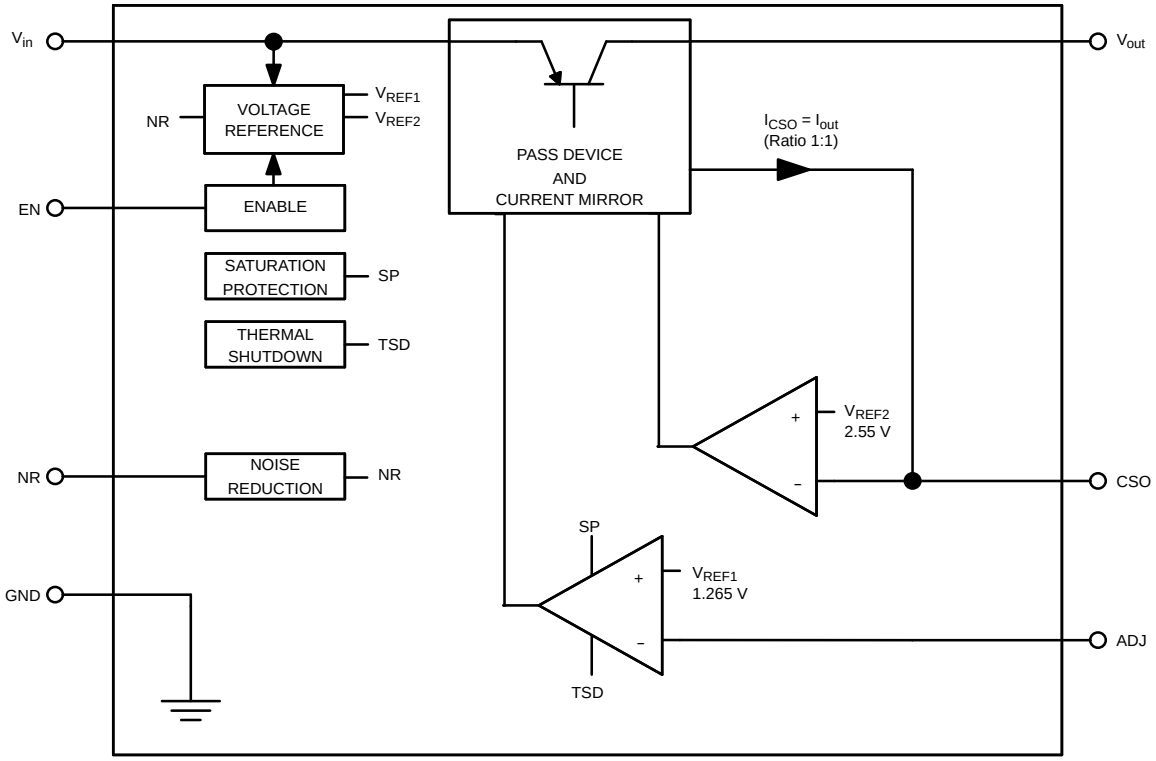

Figure 2. Simplified Block Diagram

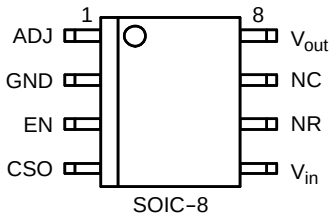

Figure 3. Pin Connections (Top View)

PIN FUNCTION DESCRIPTION

Pin No. SOIC−8	Pin Name	Description
1	ADJ	Adjustable Voltage Setting Input. See Application Section for more details.
2	GND	Power Supply Ground.
3	EN	Enable Input; low level disables the IC.
4	CSO	Current Sense Output, Current Limit setting and Output Current value information. See Application Section for more details.
5	V_{in}	Positive Power Supply Input.
6	NR	Noise Reduction Input. Connect either external capacitor for decreasing noise or must be left unconnected.
7	NC	Not Connected.
8	V_{out}	Regulated Output Voltage.

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ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input Voltage DC	V_{in}	−42	45	V
Enable Input Voltage	V_{EN}	−42	45	V
Adjustable Input Voltage	V_{ADJ}	−0.3	10	V
CSO Voltage	V_{CSO}	−0.3	7	V
Noise Reduction Input Voltage	V_{NR}	−0.3	7	V
Output Voltage	V_{out}	−1	40	V
Junction Temperature	T_J	−40	150	°C
Storage Temperature	T_{STG}	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ESD CAPABILITY (Note 1)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−2	2	kV
ESD Capability, Machine Model	ESD_{MM}	−200	200	V

1. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JS−001−2010)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)

LEAD SOLDERING TEMPERATURE AND MSL (Note 2)

Rating	Symbol	Min	Max	Unit
Moisture Sensitivity Level	MSL	1		−
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions	T_{SLD}	−	265 peak	°C

2. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS (Note 3)

Rating	Symbol	Value	Unit
Thermal Characteristics Thermal Resistance, Junction−to−Air (Note 4) Thermal Reference, Junction−to−Lead (Note 4)	 $R_{\theta JA}$ $R_{\psi JL}$	 133 76	°C/W

3. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
4. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 5)	V_{in}	4.4	40	V
Nominal Output Voltage	V_{out_nom}	3.3	20	V
Output Current Limit (Note 6)	I_{LIM}	0.1	20	mA
Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Minimum V_{in} = 4.4 V or (V_{out_nom} + 1 V), whichever is higher.
6. Corresponding R_{CSO} is in range from 25.5 kΩ down to 127.5 Ω.

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ELECTRICAL CHARACTERISTICS V_{in} = 13.5 V, V_{EN} = 3.3 V, R_{CSO} = 0 Ω, C_{CSO} = 1 μF, C_{in} = 1 μF, C_{out} = 10 μF, ESR = 1.5 Ω, Min and Max values are valid for temperature range −40°C ≤ T_J ≤ +150°C unless noted otherwise and are guaranteed by test, design or statistical correlation. Typical values are referenced to T_J = 25°C. Output Current I_{out} is the current out of pin including current through the resistor divider R_1 and R_2. (Note 7)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT						
Output Voltage (Accuracy %) (Note 8)	V_{in} = V_{in_min} to 40 V I_{out} = 0.1 mA to 20 mA	V_{out}	−3	–	+3	%
Line Regulation (Note 8)	V_{in} = V_{in_min} to (V_{out_nom} + 20 V) I_{out} = 0.1 mA	Reg_{line}	–	0.1	1.0	%
Load Regulation	I_{out} = 0.1 mA to 20 mA V_{in} = (V_{out_nom} + 8.5 V)	Reg_{load}	–	0.2	1.4	%
Dropout Voltage (Note 9)	I_{out} = 10 mA, V_{out_nom} = 5 V V_{DO} = V_{in} − V_{out}	V_{DO}	–	210	500	mV
DISABLE AND QUIESCENT CURRENTS						
Disable Current	V_{EN} = 0 V	I_{DIS}	–	0.075	10	μA
Quiescent Current, I_q = I_{in} − I_{out}	I_{out} = 0.1 mA, V_{in} = (V_{out_nom} + 8.5 V)	I_q	–	265	380	μA
Quiescent Current, I_q = I_{in} − I_{out}	I_{out} = 1 mA, V_{in} = (V_{out_nom} + 8.5 V)	I_q	–	1.45	3	mA
CURRENT LIMIT PROTECTION						
Current Limit	V_{out} = 0.9 x V_{out_nom}, V_{in} = (V_{out_nom} + 8.5 V)	I_{LIM}	20	–	50	mA
PSRR AND NOISE						
Power Supply Ripple Rejection (Note 10)	I_{out} = 1 mA, R_1 = 82 kΩ, R_2 = 27 kΩ C_{in} = none, C_b = 10 nF, C_{noise} = 10 nF f = 100 Hz, 0.5 V_{p-p} f = 1 kHz, 0.5 V_{p-p}	PSRR	 – –	 85 90	 – 	dB
Output Noise Voltage (Note 10)	I_{out} = 1 mA, R_1 = 82 kΩ, R_2 = 27 kΩ, C_b = 10 nF f = 10 Hz to 100 kHz, C_{noise} = none f = 10 Hz to 100 kHz, C_{noise} = 10 nF f = 20 Hz to 20 kHz, C_{noise} = 10 nF	V_n	 – – –	 60 23 20	 – – –	μV_{rms}
ENABLE						
Enable Input Threshold Voltage Logic Low (OFF) Logic High (ON)	 V_{out} ≤ 0.1 V V_{out} ≥ 0.9 x V_{out_nom}	$V_{th(EN)}$	 0.99 –	 1.8 1.9	 – 2.31	V
Enable Input Current	V_{EN} = 3.3 V	I_{EN}	2	8	20	μA
Turn On Time from ENABLE ON to 90% of V_{out_nom}	I_{out} = 1 mA R_1 = 82 kΩ, R_2 = 27 kΩ C_b = 10 nF, C_{noise} = 10 nF	t_{on}	–	2.8	–	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
8. V_{in_min} = 4.4 V or (V_{out_nom} + 1 V), whichever is higher.
9. Measured when the output voltage V_{out} has dropped – 2% from the nominal value obtained at V_{in} = V_{out_nom} + 8.5 V.
10. Values based on design and/or characterization.
11. Not guaranteed in dropout.
12. I_{CSO} current at no load includes also mirrored current of resistor divider (I_{div} = V_{out} / (R_1 + R_2)).

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ELECTRICAL CHARACTERISTICS V_{in} = 13.5 V, V_{EN} = 3.3 V, R_{CSO} = 0 Ω, C_{CSO} = 1 μF, C_{in} = 1 μF, C_{out} = 10 μF, ESR = 1.5 Ω, Min and Max values are valid for temperature range −40°C ≤ T_J ≤ +150°C unless noted otherwise and are guaranteed by test, design or statistical correlation. Typical values are referenced to T_J = 25°C. Output Current I_{out} is the current out of pin including current through the resistor divider R_1 and R_2. (Note 7)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
OUTPUT CURRENT SENSE						
CSO Voltage Level at Current Limit	V_{out} = 0.9 x V_{out_nom}, (V_{out_nom} = 5 V) R_{CSO} = 220 Ω	V_{CSO_Ilim}	2.346 (−8 %)	2.55	2.754 (+8 %)	V
CSO Transient Voltage Level	C_{CSO} = 4.7 μF, R_{CSO} = 220 Ω I_{out} pulse from 0.1 mA to 20 mA, tr = 1 μs	V_{CSO}	–	–	3.3	V
Output Current to CSO Current Ratio (Note 11)	V_{CSO} = 2 V I_{out} = 0.1 mA to 20 mA, (V_{out_nom} = 5 V)	I_{out}/I_{CSO}	– (−10%)	(1/1)	– (+10%)	–
CSO Current at no Load Current (Note 12)	V_{CSO} = 0 V R_1 = 82 kΩ, R_2 = 27 kΩ, C_b = 10 nF	I_{CSO_off}	–	47	60	μA
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 10)	I_{out} = 1 mA	T_{SD}	150	–	195	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
8. V_{in_min} = 4.4 V or (V_{out_nom} + 1 V), whichever is higher.
9. Measured when the output voltage V_{out} has dropped – 2% from the nominal value obtained at V_{in} = V_{out_nom} + 8.5 V.
10. Values based on design and/or characterization.
11. Not guaranteed in dropout.
12. I_{CSO} current at no load includes also mirrored current of resistor divider (I_{div} = V_{out} / (R_1 + R_2)).

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TYPICAL CHARACTERISTICS

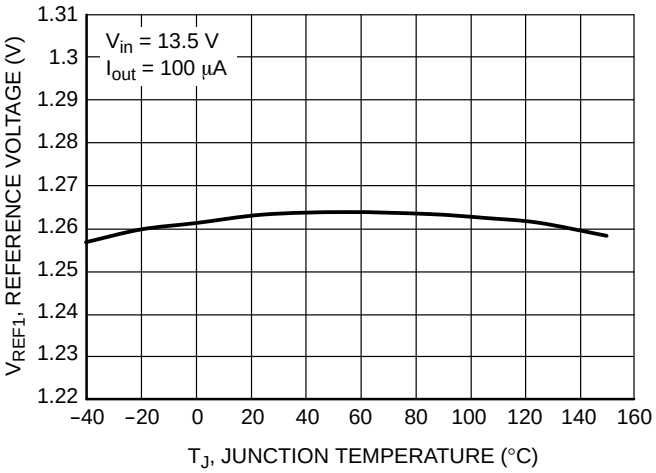

Figure 4. Reference Voltage vs. Temperature

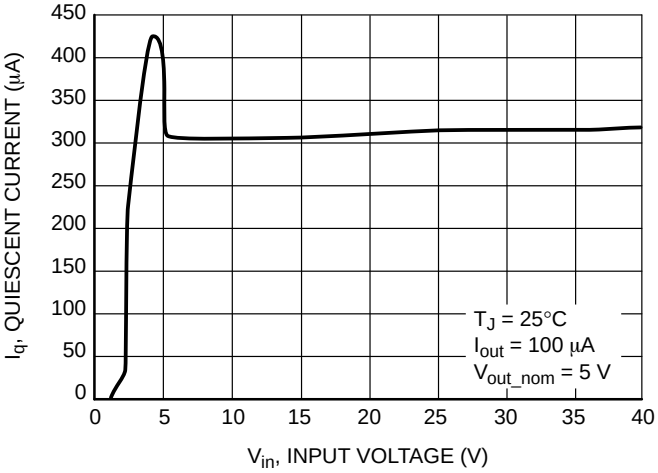

Figure 5. Quiescent Current vs. Input Voltage

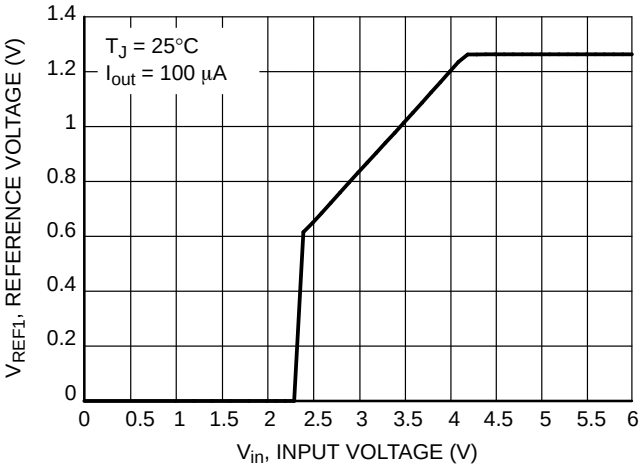

Figure 6. Reference Voltage vs. Input Voltage

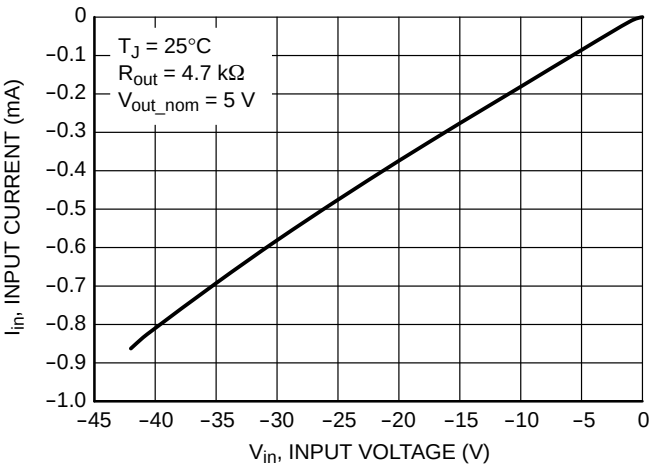

Figure 7. Input Current vs. Input Voltage (Reverse Input Voltage)

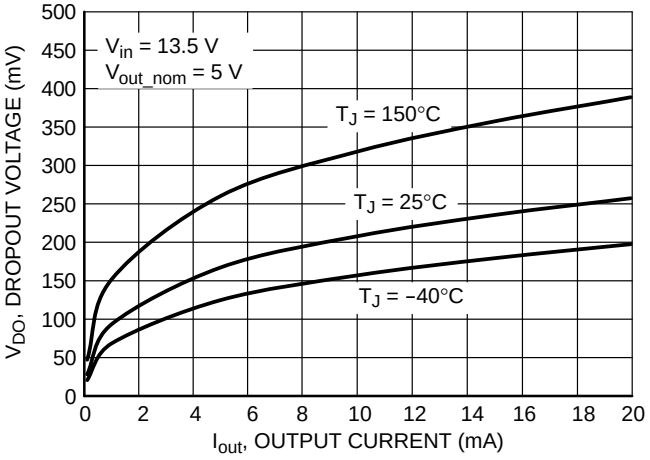

Figure 8. Dropout vs. Output Current

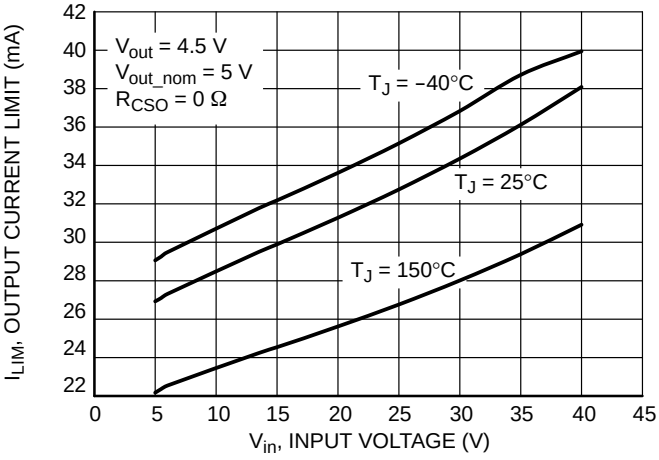

Figure 9. Output Current Limit vs. Input Voltage

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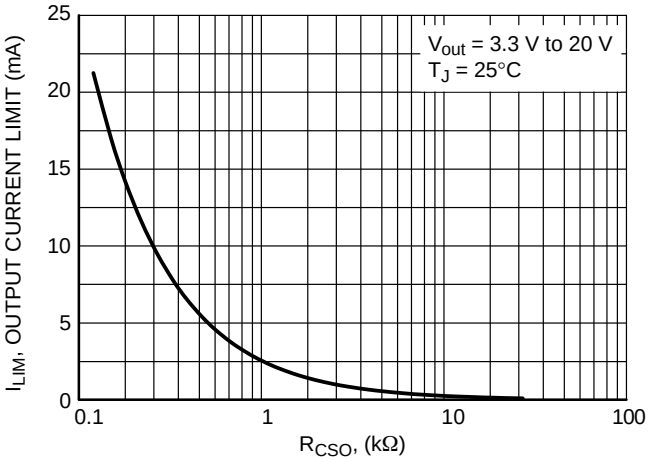

Figure 10. Output Current Limit vs. R_{CSO}

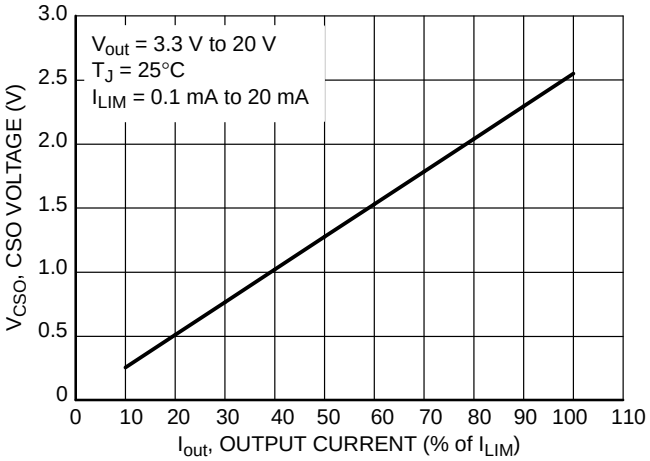

Figure 11. Output Current (% of I_{LIM}) vs. CSO Voltage

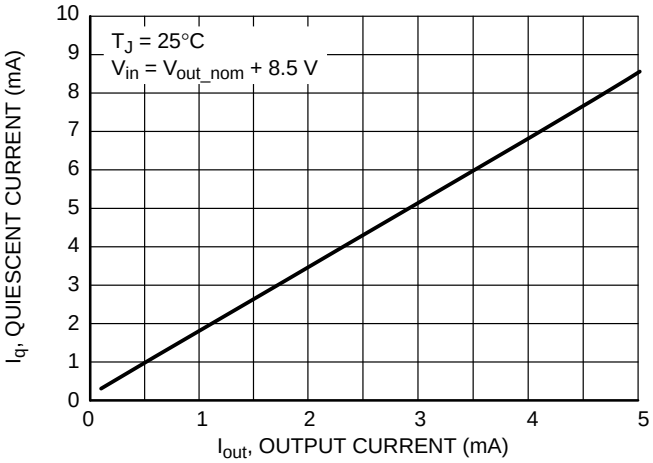

Figure 12. Quiescent Current vs. Output Current (Low Load)

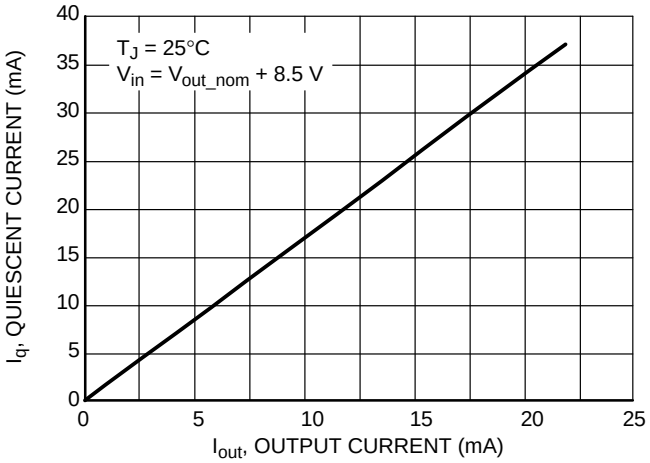

Figure 13. Quiescent Current vs. Output Current (High Load)

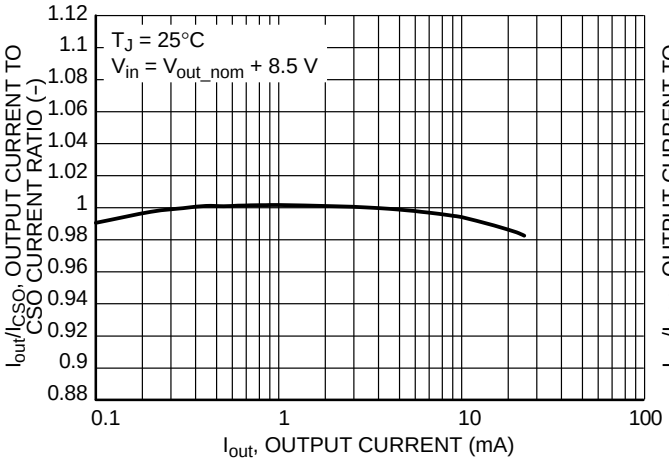

Figure 14. Output Current to CSO Current Ratio vs. Output Current

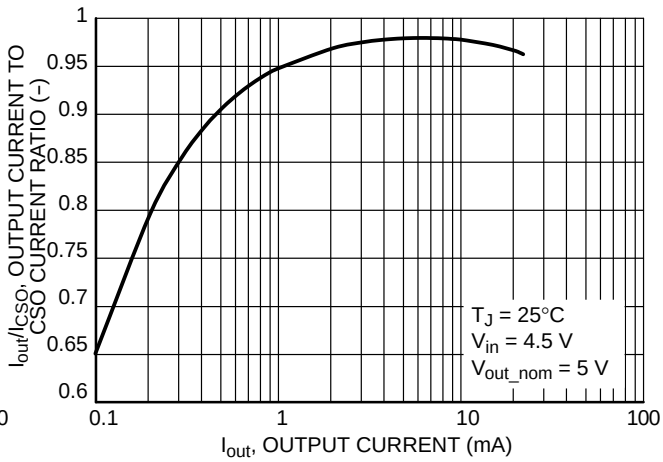

Figure 15. Output Current to CSO Current Ratio vs. Output Current (In Dropout)

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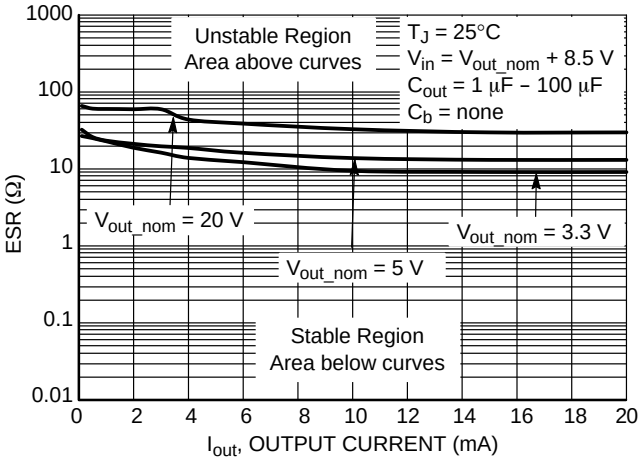

Figure 16. Output Capacitor Stability Region vs. Output Current

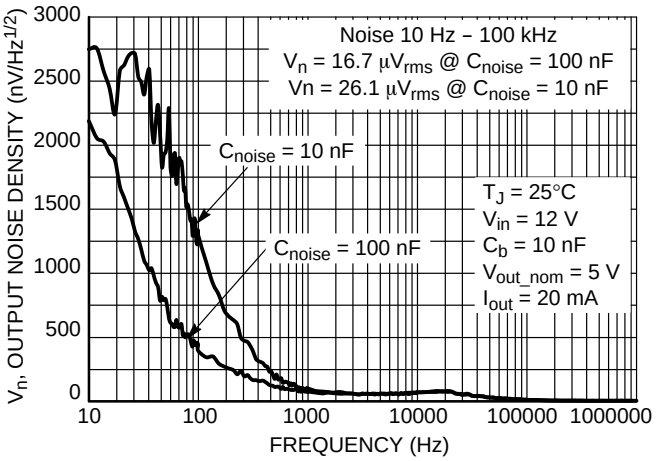

Figure 17. Noise vs. Frequency

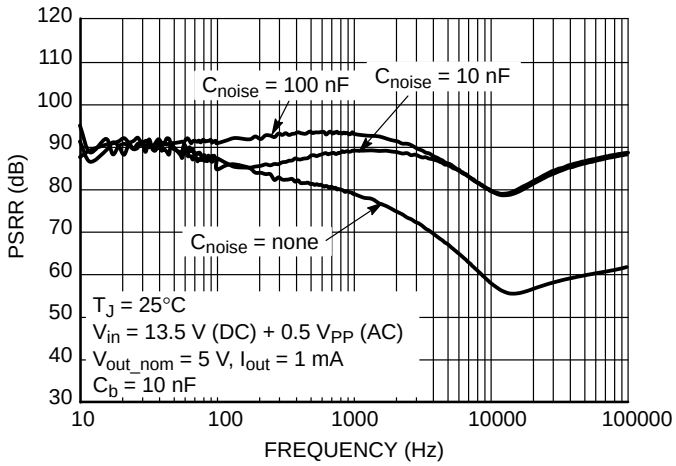

Figure 18. PSRR vs. Frequency

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DEFINITIONS

General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Output voltage

The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

Line Regulation

The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

Load Regulation

The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

Dropout Voltage

The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output voltage V_{out} has dropped −2% from the nominal value obtained at $V_{in} = V_{out_nom} + 8.5$ V. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Quiescent and Disable Currents

Quiescent Current (I_q) is the difference between the input current (measured through the LDO input pin) and the output load current. If Enable pin is set to LOW the regulator reduces its internal bias and shuts off the output, this term is called the disable current (I_{DIS}).

Current Limit

Current Limit is value of output current by which output voltage drops below 90% of its nominal value.

PSRR

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

Line Transient Response

Typical output voltage overshoot and undershoot response when the input voltage is excited with a given slope.

Load Transient Response

Typical output voltage overshoot and undershoot response when the output current is excited with a given slope between low-load and high-load conditions.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

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APPLICATIONS INFORMATION

Circuit Description

The NCV47551 is an integrated low dropout regulator that provides a regulated voltage at 20 mA to the output. It is enabled with an input to the enable pin. The regulator voltage is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference, which gives it the lowest possible dropout voltage. The output current capability is 20 mA, and the base drive quiescent current is controlled to prevent oversaturation when the input voltage is low or when the output is overloaded. The integrated current sense feature provides diagnosis and system protection functionality. The current limit of the device is adjustable by resistor connected to CSO pin. Voltage on CSO pin is proportional to output current. The regulator is protected by both current limit and thermal shutdown. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_{out}) and drives the base of a PNP series pass transistor via a buffer. The reference is a bandgap design to give it a temperature−stable output. Saturation control of the PNP is a function of the load current and input voltage. Oversaturation of the output power device is prevented, and quiescent current in the ground pin is minimized.

Regulator Stability Considerations

The input capacitor (C_{in}) is necessary to stabilize the input impedance to avoid voltage line influences. The output capacitor (C_{out}) helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information. The value for the output capacitor C_{out}, shown in Figure 1 should work for most applications; see also Figure 14 for output stability at various load and Output Capacitor ESR conditions. Stable region of ESR in Figure 14 shows ESR values at which the LDO output voltage does not have any permanent oscillations at any dynamic changes of output load current. Marginal ESR is the value at which the output voltage waving is fully damped during four periods after the load change and no oscillation is further observable.

ESR characteristics were measured with ceramic capacitors and additional series resistors to emulate ESR. Low duty cycle pulse load current technique has been used to maintain junction temperature close to ambient temperature.

Enable Input

The enable pin is used to turn the regulator on or off. By holding the pin down to a voltage less than 0.99 V, the output of the regulator will be turned off. When the voltage on the enable pin is greater than 2.31 V, the output of the regulator will be enabled to power its output to the regulated output voltage. The enable pin may be connected directly to the input pin to give constant enable to the output regulator.

Setting the Output Voltage

The output voltage range can be set between 3.3 V and 20 V. This is accomplished with an external resistor divider feeding back the voltage to the IC back to the error amplifier by the voltage adjust pin ADJ. The internal reference voltage is set to a temperature stable reference (V_{REF1}) of 1.265 V. The output voltage is calculated from the following formula. Ignoring the bias current into the ADJ pin:

$$V_{out_nom} = V_{REF1}\left(1 + \frac{R_1}{R_2}\right) \quad \text{(eq. 1)}$$

Use $R_2 < 50\ k\Omega$ to avoid significant voltage output errors due to ADJ bias current.

Designers should consider the tolerance of R_1 and R_2 during the design phase.

Setting the Output Current Limit

The output current limit can be set between 0.1 mA and 20 mA by external resistor R_{CSO} (see Figure 1). Capacitor C_{CSO} from range 1 μF to 4.7 μF in parallel with R_{CSO} is required for stability of current limit control circuitry (see Figure 1).

$$V_{CSO} = I_{out} \times R_{CSO} \quad \text{(eq. 2)}$$

$$I_{LIM} = \frac{2.55}{R_{CSO}} \quad \text{(eq. 3)}$$

$$R_{CSO} = \frac{2.55}{I_{LIM}} \quad \text{(eq. 4)}$$

Where

R_{CSO} – current limit setting resistor
V_{CSO} - voltage at CSO pin proportional to I_{out}
I_{LIM} – current limit value
I_{out} – output current actual value

CSO pin provides information about output current actual value. The CSO voltage is proportional to output current according to Equation 2.

Once output current reaches its limit value (I_{LIM}) set by external resistor R_{CSO} than voltage at CSO pin is typically 2.55 V. Calculations of I_{LIM} or R_{CSO} values can be done using equations Equations 3 and 4, respectively.

Designers should consider the tolerance of R_{CSO} during the design phase.

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Thermal Considerations

As power in the NCV47551 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV47551 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV47551 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \qquad \text{(eq. 5)}$$

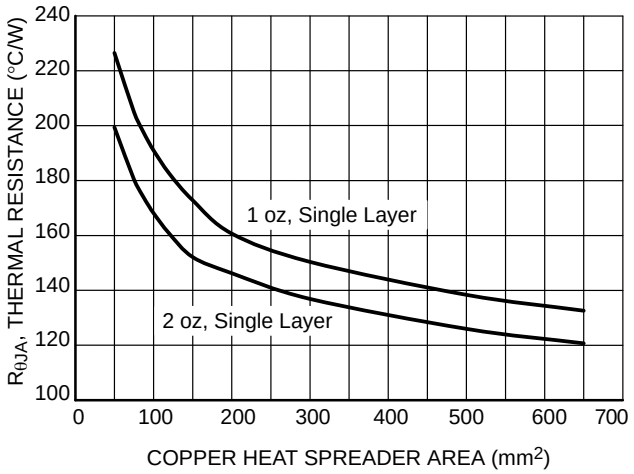

Figure 19. Thermal Resistance vs. PCB Copper Area

Since T_J is not recommended to exceed 150°C, then the NCV47551 in SO-8 soldered on 645 mm^2, 1 oz copper area, FR4 can dissipate up to 0.94 W when the ambient temperature (T_A) is 25°C. See Figure 19 for R_{thJA} versus PCB area. The power dissipated by the NCV47551 can be calculated from the following equations:

$$P_D \approx V_{in}\left(I_q @ I_{out}\right) + I_{out}\left(V_{in} - V_{out}\right) \qquad \text{(eq. 6)}$$

or

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{out} \times I_{out}\right)}{I_{out} + I_q} \qquad \text{(eq. 7)}$$

Hints

V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV47551 and make traces as short as possible.

ORDERING INFORMATION

Device	Output Voltage	Marking	Package	Shipping†
NCV47551DAJR2G	Adjustable	47551	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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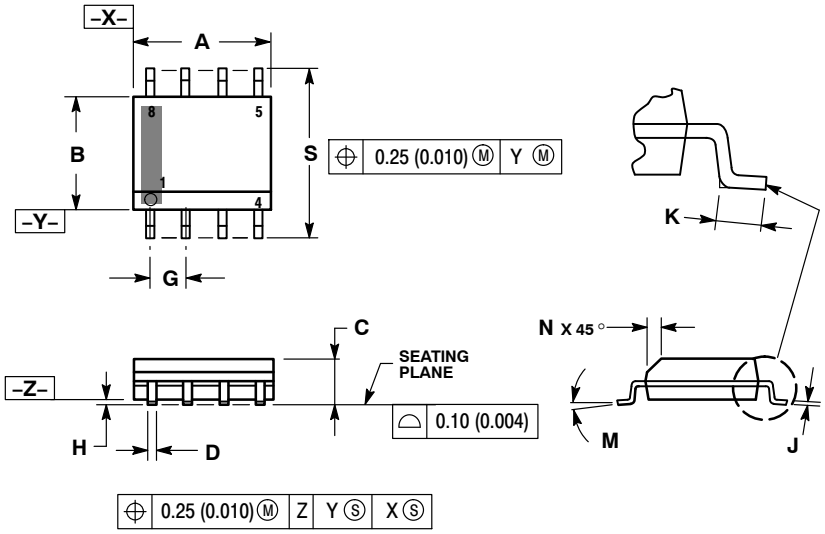
SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

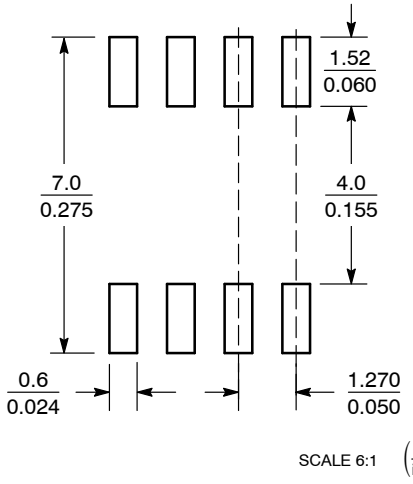
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

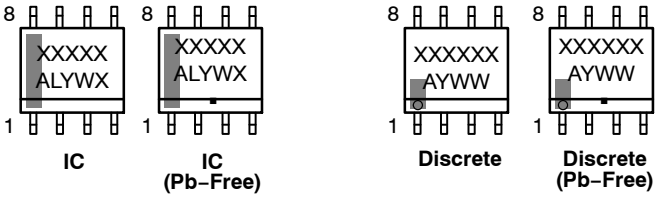
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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