

Operational Amplifier, 36 V, 3 MHz, 0.95 mV Input Offset Voltage, Rail-to-Rail

NCS20231, NCV20231

The NCS2023x series of op amps feature a wide supply range of 2.7 V to 36 V with an input offset voltage as low as ± 0.95 mV max. These op amps are available in single, dual, and quad channel configurations. Automotive qualified options are available under the NCV prefix with an optional extended operating temperature range from -40 °C to 150 °C. All other versions are specified over the operating temperature range from -40 °C to 125 °C.

Features

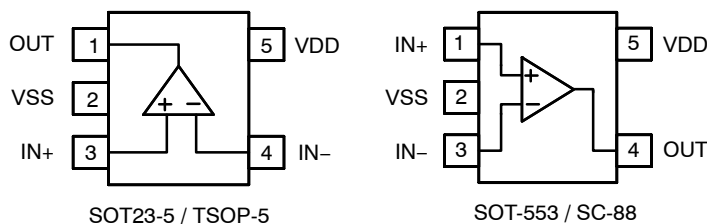
- Supply Voltage Range: 2.7 V to 36 V
- Temperature Range: -40 °C to 150 °C
- Unity Gain Bandwidth: 3 MHz
- Input Offset Voltage: ± 1.2 mV max, $T_A = -40$ to 150 °C
- Input Offset Voltage Drift: ± 2 μ V/°C max
- Common-Mode Input Voltage Range
 - ♦ Optimal: $V_{SS} - 0.1$ to $V_{DD} - 2$ V
 - ♦ Functional: $V_{SS} - 0.1$ to $V_{DD} + 0.1$ V
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Telecom Equipment
- Power Supply Designs
- Diesel Injection Control
- Automotive
- Motor Control

PIN CONNECTIONS

Single Channel

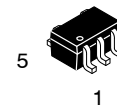
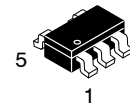


SOT23-5 / TSOP-5

SOT-553 / SC-88

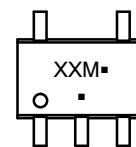
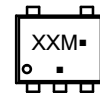
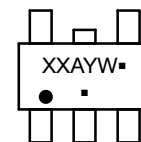
Dual Channel

Quad Channel


SC-88A / SC70-5
CASE 419A-02

TSOP-5
CASE 483

SOT-553, 5 LEAD
CASE 463B

DEVICE MARKING INFORMATION


SC-88A / SC70-5
CASE 419A-02

SO-553, 5 LEAD
CASE 463B

TSOP-5
CASE 483

XX = Specific Device Code
 A = Assembly Location
 Y = Year
 W = Work Week
 M = Date Code
 G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Supply Voltage Range ($V_{DD} - V_{SS}$)	V_S	-0.3 to 40	V
Input Common-Mode Voltage	V_{CM}	$V_{SS} - 0.2$ to $V_{DD} + 0.2$	V
Differential Input Voltage	V_{ID}	$\pm V_S$	V
Maximum Input Current	I_I	± 10	mA
Maximum Output Current	I_O	± 100	mA
Continuous Total Power Dissipation	P_D	200	mW
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	T_{STG}	-65 to 150	°C
ESD Capability, Human Body Model (Note 2)	HBM	± 2000	V
ESD Capability, Charge Device Model (Note 2)	CDM	± 1000	V
Moisture Sensitivity Level	MSL	Level 1	
Lead Temperature Soldering Reflow (SMD Styles Only), Pb-Free Versions (Note 3)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area
2. This device series incorporates ESD protection and is tested by the following methods:
ESD Human Body Model tested per JEDEC standard JS-001-2017 (AEC-Q100-002)
ESD Charged Device Model tested per JEDEC standard JS-002-2014 (AEC-Q100-011)
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERM/D

THERMAL CHARACTERISTICS (Note 4)

Package	θ_{JA} Junction-to-Ambient Thermal Resistance	Ψ_{JT} Junction-to-Case Top Thermal Characteristic	Ψ_{JB} Junction-to-Board Thermal Characteristic	Unit
TSOP-5 / SOT23-5	254	78	150	°C/W
SC-88A / SC-70-5 / SOT-353	902	70	810	°C/W
SOT-553	238	14	134	°C/W

4. Thermal parameters are based on a 2s2p board following JESD51-7 (JEDEC)

RECOMMENDED OPERATING RANGES (Note 5)

Parameter	Symbol	Min	Max	Unit
Supply Voltage ($V_{DD} - V_{SS}$)	V_S	2.7	36	V
Differential Input Voltage ($V_{IN+} - V_{IN-}$)	V_{ID}	-	± 5 (Note 6)	V
Input Common-Mode Range (Note 7)	V_{CM}	$V_{SS} - 0.1$	$V_{DD} - 2$ V	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area
6. The differential voltage may not exceed the supply voltage, $\pm V_S$. For supplies greater than $V_S = 5$ V, differential voltages up to $\pm V_S$ will consume more input current. See APPLICATION INFORMATION.
7. The specified input common mode range yields the best performance. However, the input common mode range is functional up to $V_{DD} + 0.1$ V. See APPLICATION INFORMATION.

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ELECTRICAL CHARACTERISTICS ($V_S = 2.7\text{ V to }36\text{ V}$)

At $T_A = +25\text{ }^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

Boldface limits apply over the specified temperature range, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Supply Voltage (V)	Temp ($^\circ\text{C}$)	Min	Typ	Max	Unit
INPUT CHARACTERISTICS								
Offset Voltage	V_{OS}	$V_{CM} = \text{mid-supply}$	2.7, 5, 10, 36	25	–	± 0.3	± 0.95	mV
				–40 to 125	–	–	± 1.2	
				–40 to 150	–	–	± 1.2	
Offset Voltage Drift over Temperature	dV_{OS}/dT	$V_{CM} = \text{mid-supply}$	2.7, 5, 10, 36	–40 to 125	–	± 0.5	± 2	$\mu\text{V}/^\circ\text{C}$
				–40 to 150	–	± 0.5	± 5	
Input Bias Current (Note 8)	I_{IB}		2.7, 5, 10, 36	25	–	± 5	± 60	pA
				–40 to 125	–	–	± 3000	
				150	–	± 10000	–	
Input Offset Current (Note 8)	I_{OS}		2.7	25	–	± 0.5	± 60	pA
				–40 to 125	–	–	± 500	
				–40 to 150	–	–	± 2000	
			5, 10	25	–	± 0.5	± 60	
				–40 to 125	–	–	± 800	
				–40 to 150	–	–	± 2500	
			36	25	–	± 0.5	± 60	pA
				–40 to 125	–	–	± 2000	
				–40 to 150	–	–	± 2500	
Input Capacitance	C_{IN}	IN+	2.7, 36	25	–	1	–	pF
		IN–	2.7, 36	25	–	6	–	
Common Mode Rejection Ratio	CMRR	$V_{CM} = V_{SS} - 0.1\text{ V}$ to $V_{DD} - 2\text{ V}$	2.7	25	80	98	–	dB
				–40 to 125	75	–	–	
				–40 to 150	69	–	–	
			5 (Note 8)	25	90	105	–	
				–40 to 125	85	–	–	
				–40 to 150	80	–	–	
			10 (Note 8)	25	100	117	–	
				–40 to 125	100	–	–	
				–40 to 150	94	–	–	
			36	25	110	122	–	
				–40 to 125	110	–	–	
				–40 to 150	107	–	–	
		$V_{CM} = V_{SS} + 1.8\text{ V}$ to $V_{DD} - 2.4\text{ V}$	36	25	117 (Note 8)	125	–	dB
EMI Rejection Ratio	EMIRR		2.7, 36	25	–	See Figure 29	–	dB

8. Guaranteed by design and/or characterization.

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ELECTRICAL CHARACTERISTICS ($V_S = 2.7\text{ V to }36\text{ V}$) (continued)

At $T_A = +25\text{ }^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

Boldface limits apply over the specified temperature range, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Supply Voltage (V)	Temp ($^\circ\text{C}$)	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS								
Open Loop Voltage Gain	A_{VOL}	$V_{CM} = \text{mid-supply}$	2.7	25	100	115	–	dB
				–40 to 125	90	–	–	
				–40 to 150	90	–	–	
			5 (Note 9)	25	120	135	–	
				–40 to 125	115	–	–	
				–40 to 150	115	–	–	
			10 (Note 9)	25	130	145	–	
				–40 to 125	120	–	–	
				–40 to 150	120	–	–	
			36	25	135	154	–	
				–40 to 125	130	–	–	
				–40 to 150	130	–	–	
Open Loop Output Impedance	Z_{OUT}			–	–	See Figure 28	–	Ω
High Level Output Voltage Swing from V_{DD}	$V_{DD}-V_{OH}$	$R_L = 10\text{ k}\Omega$	2.7, 5, 10, 36	25	–	60	80	mV
				–40 to 125	–	–	120	
				–40 to 150	–	–	150	
		$I_{OUT} = 1\text{ mA}$	2.7, 5, 10, 36	25	–	40	60	
				–40 to 125	–	–	80	
				–40 to 150	–	–	100	
		$I_{OUT} = 5\text{ mA}$	10	25	–	165	200	
				–40 to 125	–	–	350	
				–40 to 150	–	–	400	
Low Level Output Voltage Swing from V_{SS}	$V_{OL}-V_{SS}$	$R_L = 10\text{ k}\Omega$	2.7, 5, 10	25	–	16	30	mV
				–40 to 125	–	–	50	
				–40 to 150	–	–	50	
			36	25	–	55	80	
				–40 to 125	–	–	250	
				–40 to 150	–	–	120	
		$I_{OUT} = 1\text{ mA}$	2.7, 5, 10, 36	25	–	35	50	
				–40 to 125	–	–	80	
				–40 to 150	–	–	80	
		$I_{OUT} = 5\text{ mA}$	10	25	–	150	170	
				–40 to 125	–	–	300	
				–40 to 150	–	–	300	
Output Current Capability	I_{OUT}	Output to V_{DD} rail, sinking current	2.7, 5, 10, 36	25	–	28	–	mA
		Output to V_{SS} rail, sourcing current	2.7, 5, 10, 36	25	–	28	–	
Capacitive Load Drive	C_L	Phase margin = 35°	2.7 to 36	25	–	140	–	pF

9. Guaranteed by design and/or characterization.

NCS20231, NCV20231

ELECTRICAL CHARACTERISTICS ($V_S = 2.7\text{ V to }36\text{ V}$) (continued)

At $T_A = +25\text{ }^{\circ}\text{C}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

Boldface limits apply over the specified temperature range, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Supply Voltage (V)	Temp ($^{\circ}\text{C}$)	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE								
Gain Bandwidth Product	GWBP	$C_L = 25\text{ pF}$	2.7, 5, 10, 36	25	–	3	–	MHz
Gain Margin	A_m	$C_L = 25\text{ pF}$	2.7, 5, 10, 36	25	–	16	–	dB
Phase Margin	Φ_m	$C_L = 25\text{ pF}$	2.7, 5, 10, 36	25	–	60	–	$^{\circ}$
Slew Rate	SR	Unity gain, $R_L = 2\text{ k}\Omega$	2.7, 5, 10, 36	25	–	4	–	V/ μs
Settling Time to 0.1 %	t_s	$V_{IN} = 1\text{ V step}$	2.7	25	–	7	–	μs
		$V_{IN} = 3\text{ V step}$	5	25	–	7	–	
		$V_{IN} = 8\text{ V step}$	10	25	–	7	–	
		$V_{IN} = 10\text{ V step}$	36	25	–	6	–	
Settling Time to 0.01 %	t_s	$V_{IN} = 1\text{ V step}$	2.7	25	–	20	–	μs
		$V_{IN} = 3\text{ V step}$	5	25	–	10	–	
		$V_{IN} = 8\text{ V step}$	10	25	–	9	–	
		$V_{IN} = 10\text{ V step}$	36	25	–	9	–	

NOISE PERFORMANCE

Total Harmonic Distortion + Noise	THD+ N	$V_{IN} = 0.5\text{ V}_{pp}$, $f = 1\text{ kHz}$, $A_V = 1$	2.7	25	–	0.009	–	%
		$V_{IN} = 2.5\text{ V}_{pp}$, $f = 1\text{ kHz}$, $A_V = 1$	5	25	–	0.0004	–	
		$V_{IN} = 7.5\text{ V}_{pp}$, $f = 1\text{ kHz}$, $A_V = 1$	10	25	–	0.0002	–	
		$V_{IN} = 28.5\text{ V}_{pp}$, $f = 1\text{ kHz}$, $A_V = 1$	36	25	–	0.0002	–	
Voltage Noise Density	e_n	$f = 1\text{ kHz}$	2.7, 5, 10, 36	25	–	20	–	nV/ $\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$			–	20	–	
Current Noise Density	i_n	$f = 1\text{ kHz}$	2.7, 5, 10, 36	25	–	30	–	fA/ $\sqrt{\text{Hz}}$
Voltage Noise, Peak to Peak	e_{pp}	$f_{IN} = 0.1\text{ Hz to }10\text{ Hz}$	2.7, 5, 10, 36	25	–	700	–	nV $_{pp}$

POWER SUPPLY

Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to }36\text{ V}$	2.7, 36	25	125	138	–	dB
				–40 to 125	120	–	–	
				–40 to 150	120	–	–	
Quiescent Current	I_Q	No load	2.7, 5	25	–	0.37	0.595	mA
				–40 to 125	–	–	0.650	
				–40 to 150	–	–	0.7	
			10	25	–	0.375	0.595	
				–40 to 125	–	–	0.650	
				–40 to 150	–	–	0.75	
			36	25	–	0.41	0.595	
				–40 to 125	–	–	0.650	
				–40 to 150	–	–	0.8	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

TYPICAL PERFORMANCE AT $T_A = 25^\circ\text{C}$, $V_{CM} = \text{MID-SUPPLY}$, $C_L = 20\text{ PF}$, $R_L = 10\text{ K}\Omega$ TO MID-SUPPLY, UNLESS OTHERWISE NOTED

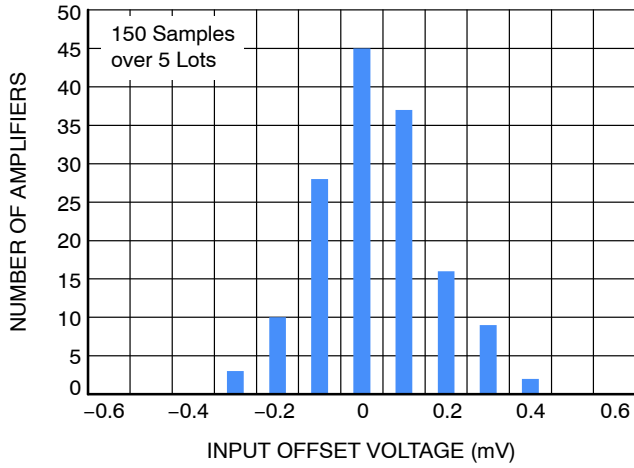


Figure 1. Input Offset Voltage Distribution

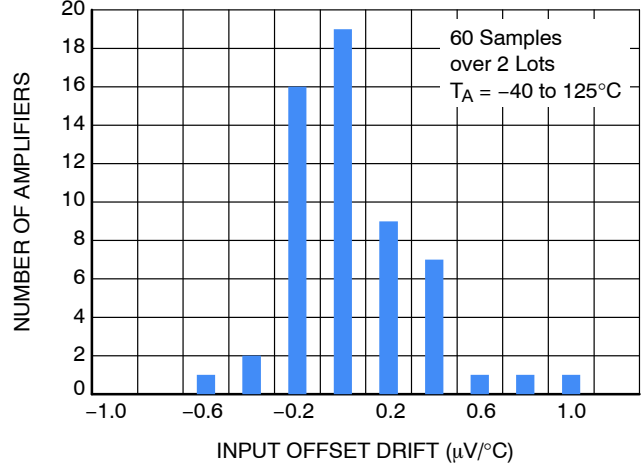


Figure 2. Input Offset Voltage Drift Distribution

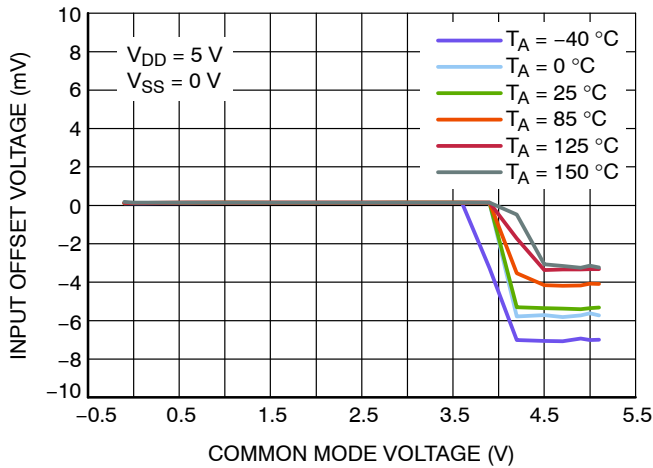


Figure 3. Input Offset Voltage vs. Common Mode Voltage

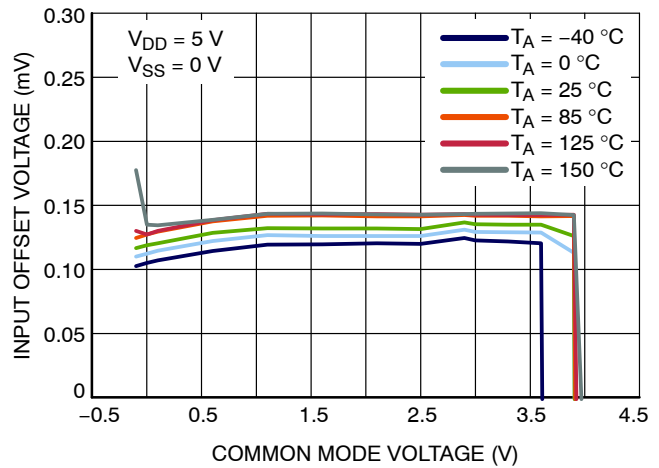


Figure 4. Input Offset Voltage vs. Common Mode Voltage, Performance Region

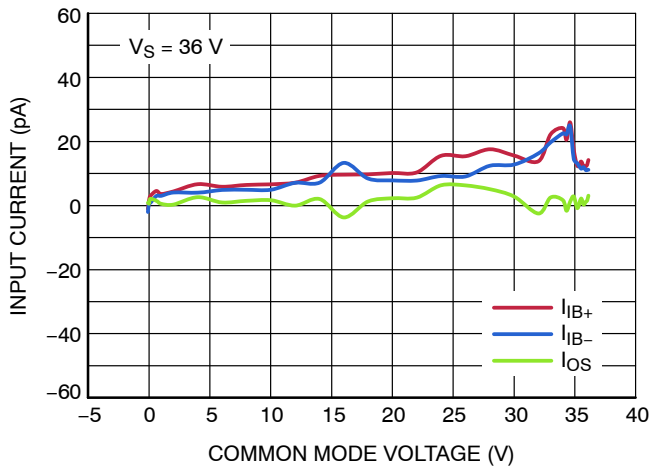


Figure 5. Input Current vs. Common Mode Voltage

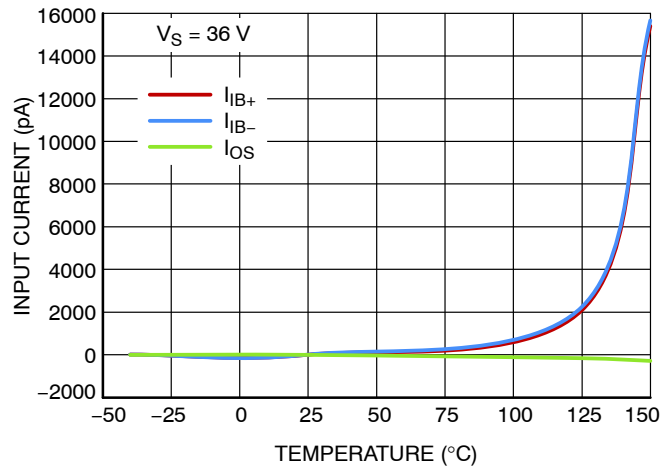


Figure 6. Input Current vs. Temperature

TYPICAL CHARACTERISTICS

TYPICAL PERFORMANCE AT $T_A = 25^\circ\text{C}$, $V_{CM} = \text{MID-SUPPLY}$, $C_L = 20\text{ pF}$, $R_L = 10\text{ k}\Omega$ TO MID-SUPPLY, UNLESS OTHERWISE NOTED

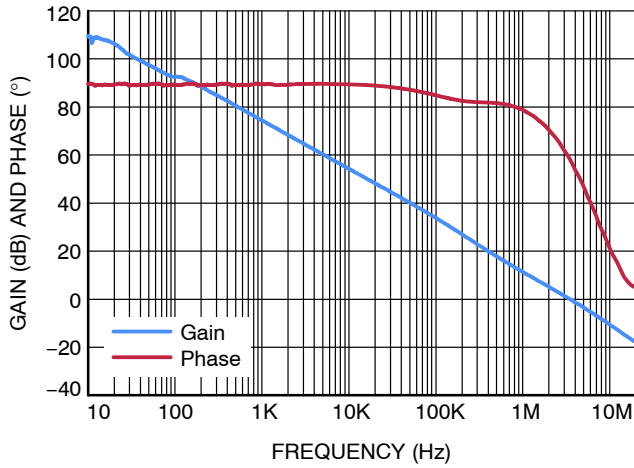


Figure 7. Open Loop Gain and Phase vs. Frequency

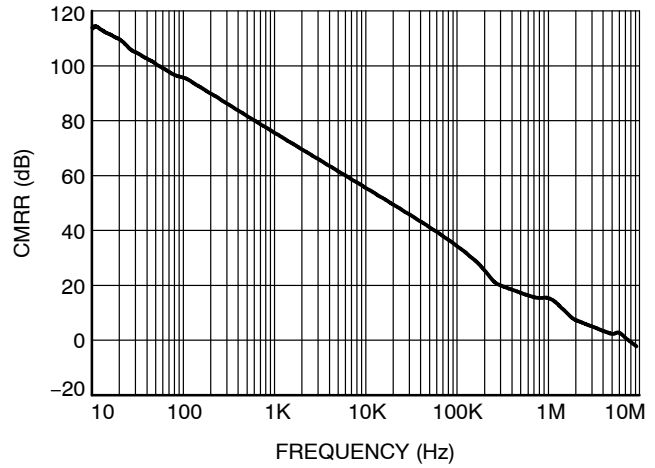


Figure 8. CMRR vs. Frequency

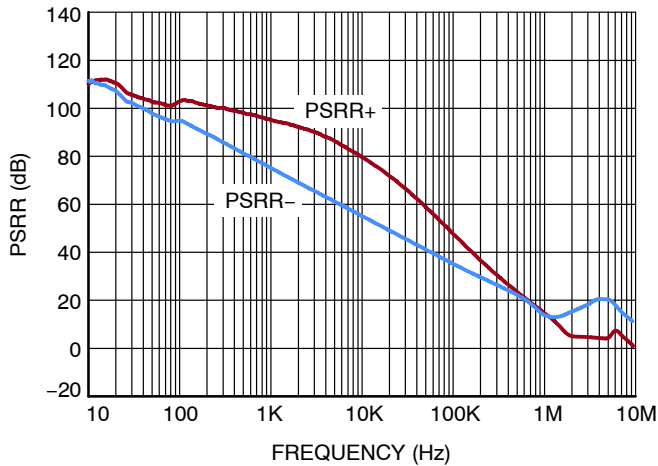


Figure 9. PSRR vs. Frequency

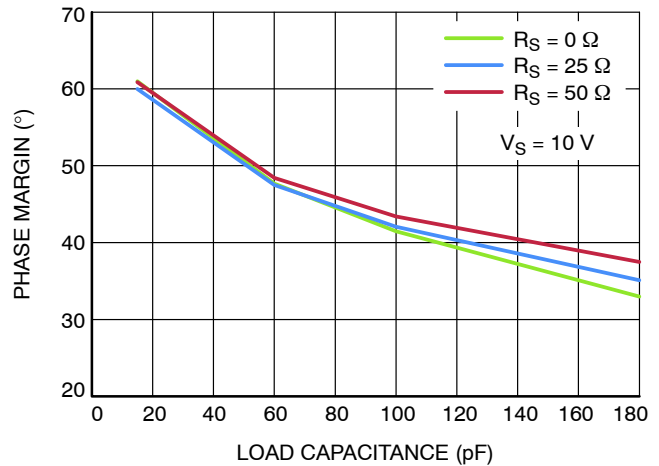


Figure 10. Phase Margin vs. Capacitive Load

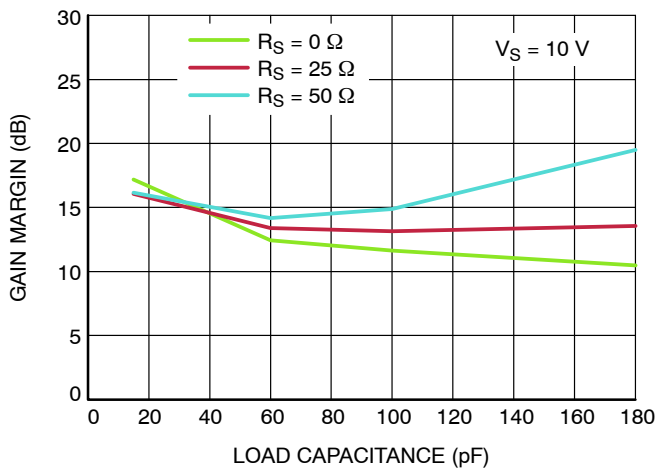


Figure 11. Gain Margin vs. Capacitive Load

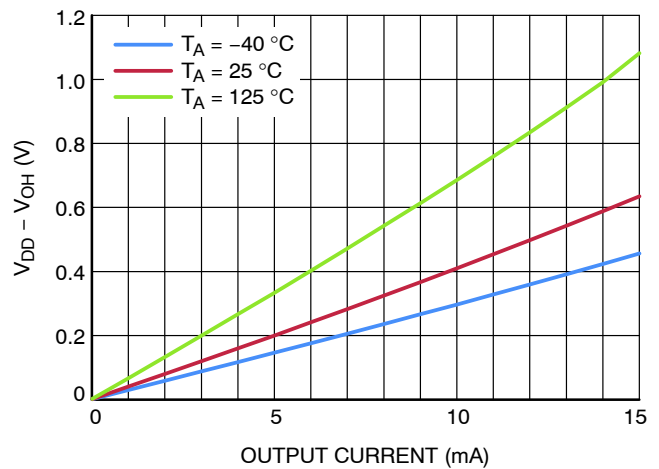


Figure 12. Output Voltage Swing High vs. Output Current at $V_S = 2.7\text{ V}$

TYPICAL CHARACTERISTICS

TYPICAL PERFORMANCE AT $T_A = 25^\circ\text{C}$, $V_{CM} = \text{MID-SUPPLY}$, $C_L = 20 \text{ PF}$, $R_L = 10 \text{ K}\Omega$ TO MID-SUPPLY, UNLESS OTHERWISE NOTED

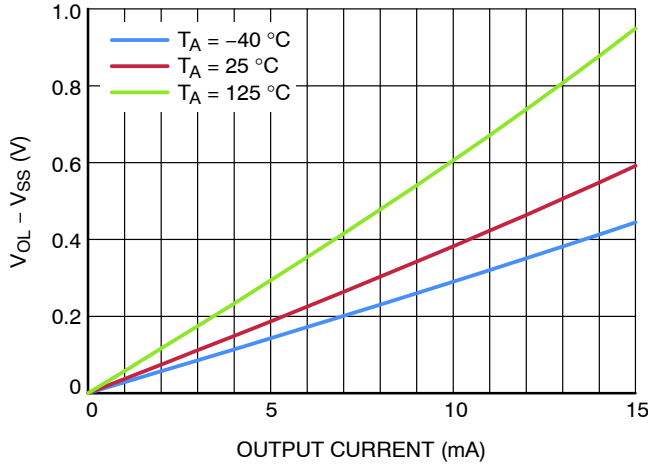


Figure 13. Output Voltage Swing vs. Output Current at $V_S = 2.7 \text{ V}$

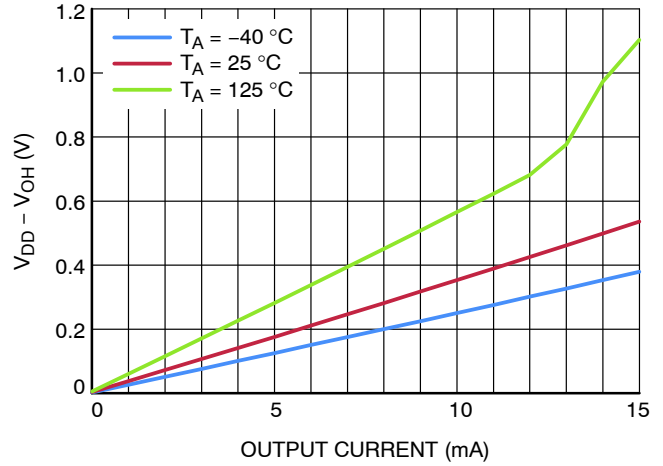


Figure 14. Output Voltage Swing vs. Output Current at $V_S = 36 \text{ V}$

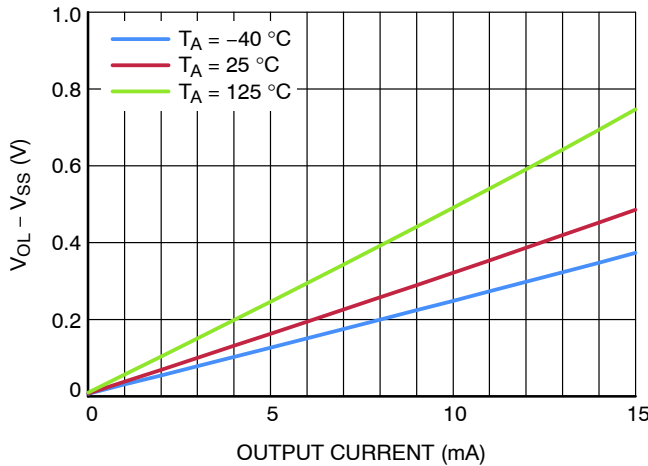


Figure 15. Output Voltage Swing vs. Output Current at $V_S = 36 \text{ V}$

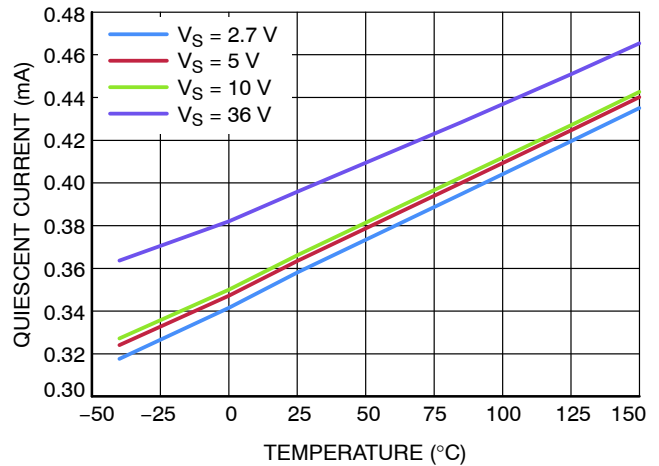


Figure 16. Quiescent Current vs. Temperature

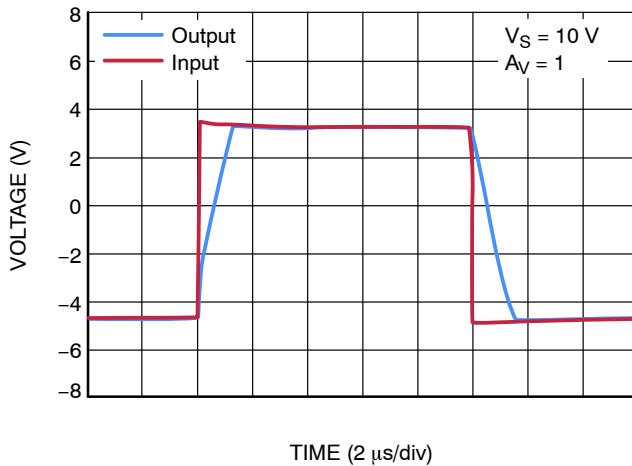


Figure 17. Large Signal Step Response

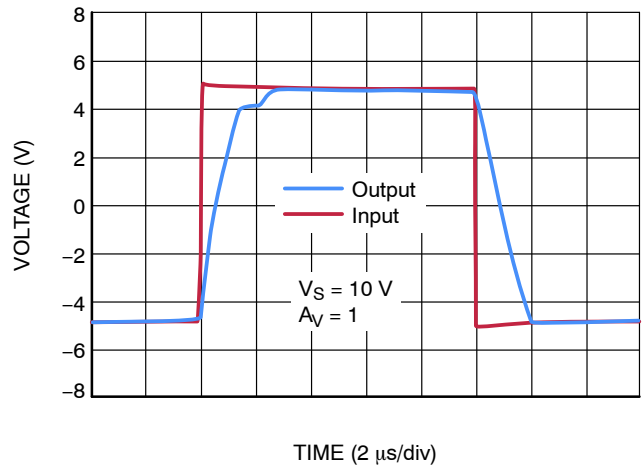


Figure 18. Large Signal Step Response

TYPICAL CHARACTERISTICS

TYPICAL PERFORMANCE AT $T_A = 25^\circ\text{C}$, $V_{CM} = \text{MID-SUPPLY}$, $C_L = 20\text{ pF}$, $R_L = 10\text{ k}\Omega$ TO MID-SUPPLY, UNLESS OTHERWISE NOTED

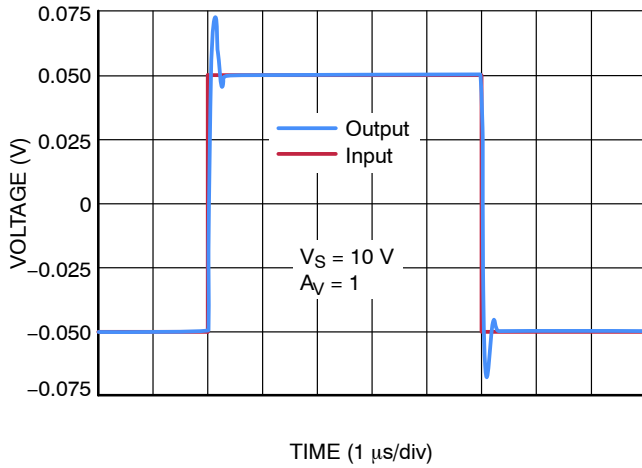


Figure 19. Small Signal Step Response

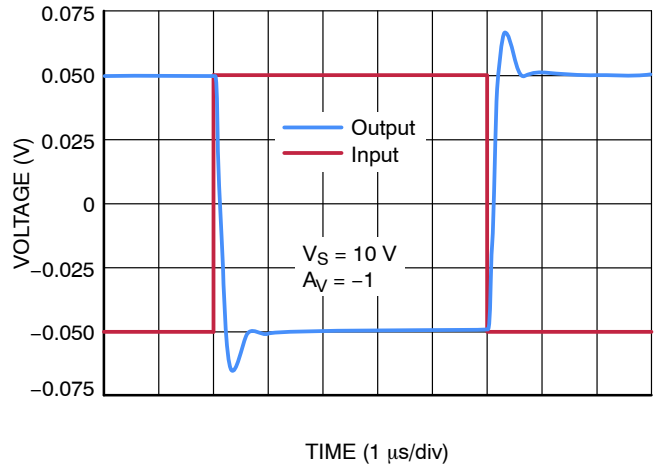


Figure 20. Small Signal Step Response

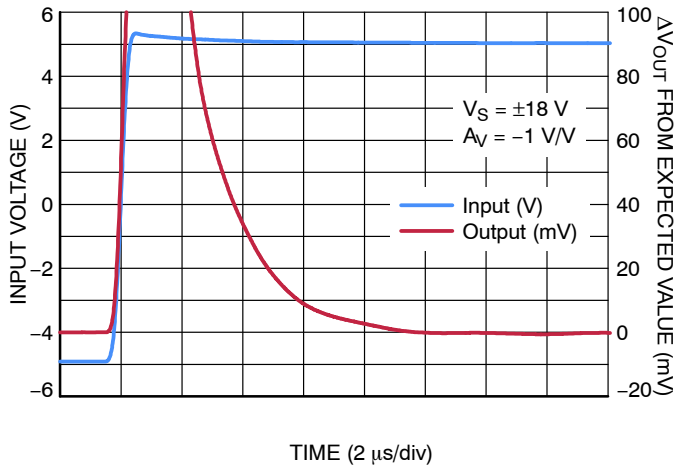


Figure 21. Settling Time

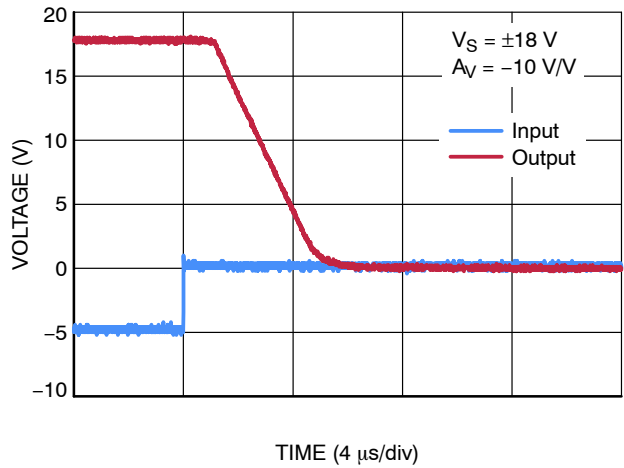


Figure 22. Output Overload Recovery Response

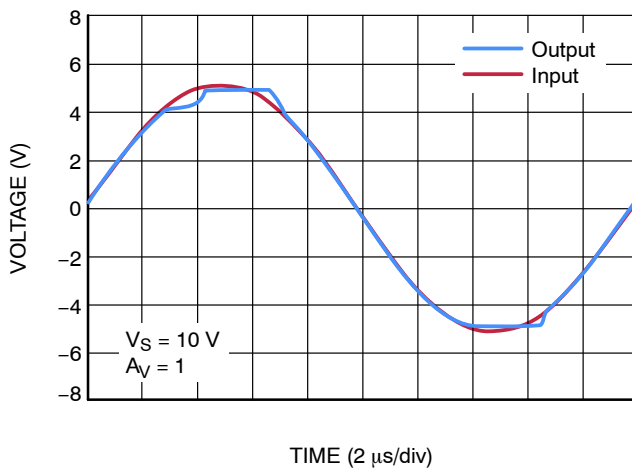


Figure 23. No Phase Reversal

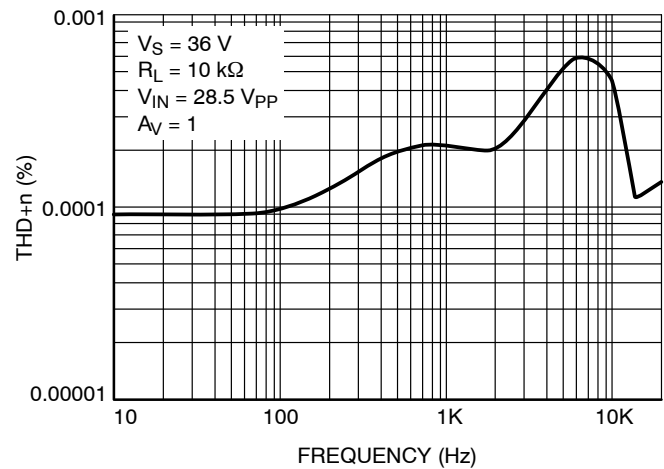


Figure 24. THD+n vs. Frequency

TYPICAL CHARACTERISTICS

TYPICAL PERFORMANCE AT $T_A = 25^\circ\text{C}$, $V_{CM} = \text{MID-SUPPLY}$, $C_L = 20\text{ pF}$, $R_L = 10\text{ k}\Omega$ TO MID-SUPPLY, UNLESS OTHERWISE NOTED

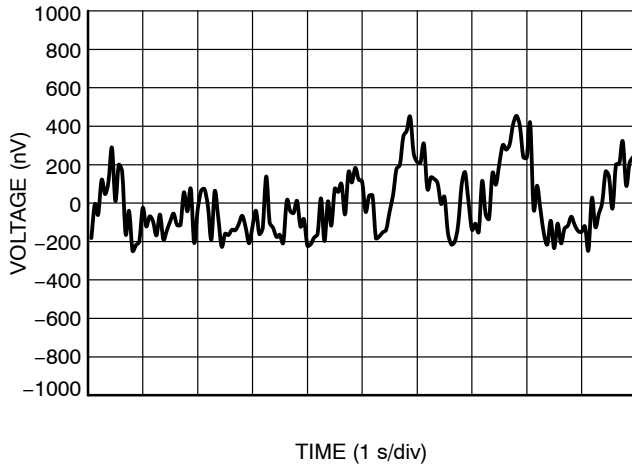


Figure 25. 0.1 Hz to 10 Hz Noise

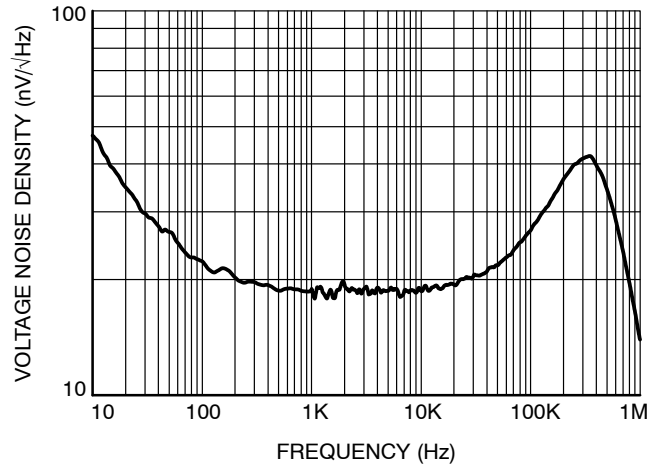


Figure 26. Voltage Noise Density vs. Frequency

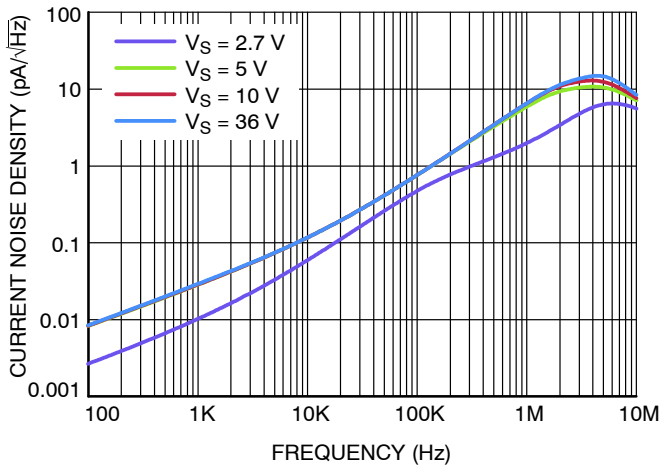


Figure 27. Current Noise Density vs. Frequency

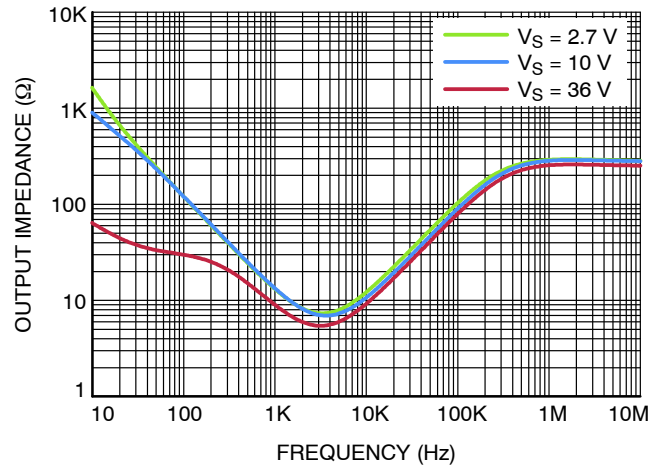


Figure 28. Open Loop Output Impedance vs. Frequency

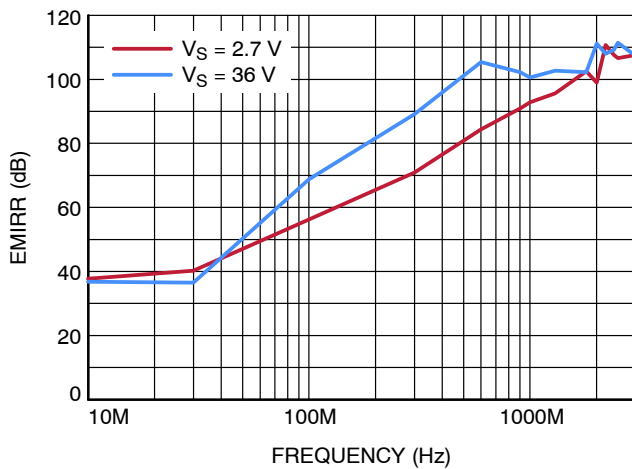


Figure 29. EMIRR vs. Frequency

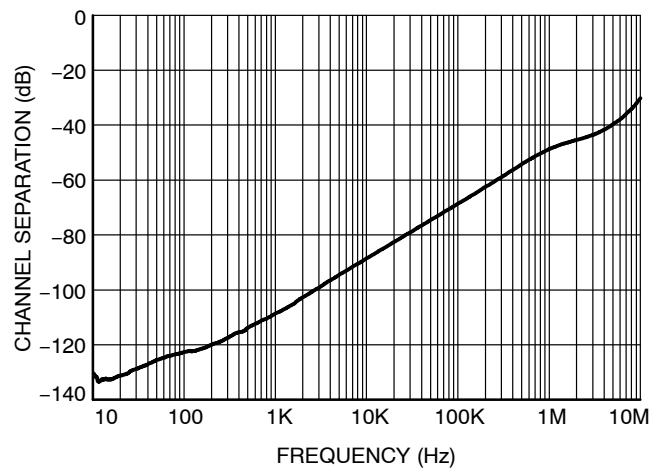


Figure 30. Channel Separation vs. Frequency

APPLICATION INFORMATION

Input and ESD Structure

The NCS20231 amplifier has back-to-back Zener diodes, which allow for normal operation with the differential voltage up to ± 5 V. Differential voltages beyond this are

permitted, up to $\pm V_S$, but increased input leakage current should be expected. Internal current limiting resistors in series with the input pins limit the current to ± 10 mA in scenarios where the differential voltage is as high as ± 36 V.

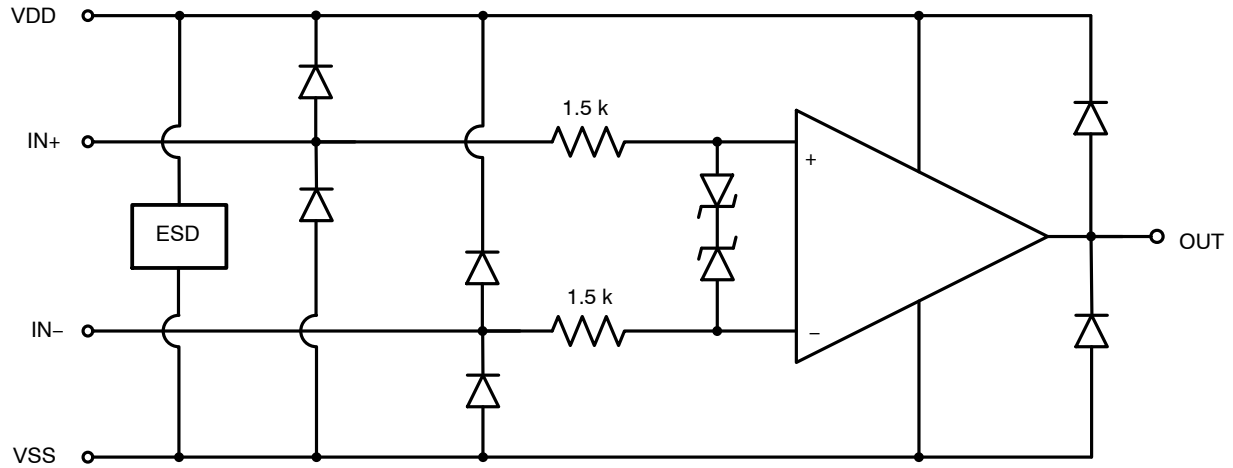


Figure 31. Representative Schematic of the Op Amp

Each input pin is diode clamped to the rails. In case of an input overvoltage, input currents must be limited to within ± 10 mA to prevent excessive current from damaging the part.

Rail-to-Rail Performance

The functional common mode input voltage spans 100 mV beyond the rails. High precision performance, as

shown throughout the ELECTRICAL CHARACTERISTICS table, is achieved in the $V_{SS} - 0.1$ V to $V_{DD} - 2$ V common mode voltage range. The input common mode extends further up to $V_{DD} + 0.1$ V to ensure functionality near the upper rail, though without precision performance in that region. The typical performance within the $V_{DD} - 2$ V to $V_{DD} + 0.1$ V range is shown in the table below.

Parameter	Symbol	Conditions	Typ	Units
Input Offset Voltage	V_{OS}	$V_{CM} = V_{DD} - 0.5$ V	± 9	mV
Input Offset Voltage over Temperature	dV_{OS}/dT		± 24	$\mu V/^{\circ}C$
Common Mode Rejection Ratio	CMRR	$V_{CM} = V_{DD} - 0.5$ V to $V_{DD} + 0.1$ V	75	dB
Open Loop Voltage Gain	A_{VOL}	$V_{CM} = V_{DD} - 0.5$ V	90	dB
Gain Bandwidth Product	GBWP	$V_{CM} = V_{DD} - 0.5$ V, $C_L = 25$ pF	2.5	MHz
Slew Rate	SR	Unity gain, $V_{CM} = V_{DD} - 1$ V to $V_{DD} - 0.2$ V	1.2	V/ μs
Voltage Noise Density	e_n	$f = 1$ kHz	1000	nV/ $\sqrt{Hz}$

The NCS20231 does not exhibit output phase reversal. Phase reversal occurs in some amplifiers when the input voltage exceeds the recommended input common mode voltage range, causing the output to flip to the opposite rail.

Instead, when the input common mode voltage range is exceeded on the NCS20231, the output becomes clipped at the output, limited by the output voltage swing.

NCS20231, NCV20231

ORDERING INFORMATION

Temperature	Channels	Package	Device Part Number	Marking	Shipping [†]
-------------	----------	---------	--------------------	---------	-----------------------

Industrial and Commercial

-40 °C to 125 °C	Single	TSOP-5	NCS20231SN2T1G	AAC	3000 / Tape & Reel
		SC-88	NCS20231SQ3T2G	AAG	3000 / Tape & Reel
		SOT-553	NCS20231XV53T2G	AC	4000 / Tape & Reel

Automotive Qualified, Grade 1

-40°C to 150 °C	Single	TSOP-5	NCV20231SN2T1G	AAC	3000 / Tape & Reel
		SC-88	NCV20231SQ3T2G	AAG	3000 / Tape & Reel
		SOT-553	NCV20231XV53T2G	AC	4000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

* In Development. Contact local sales office for more information.

NCS20231, NCV20231

REVISION HISTORY

Revision	Description of Changes	Date
5	Revision to delete dual and quad package options.	7/3/2025

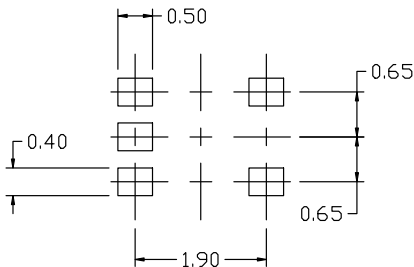
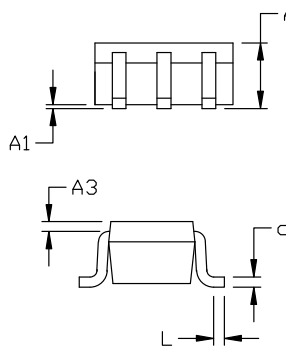
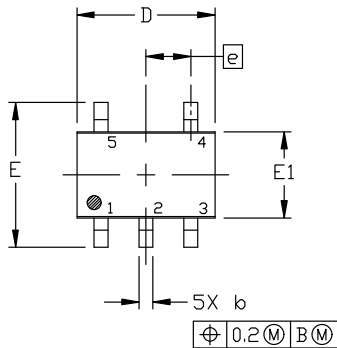
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



SCALE 2:1

SC-88A (SC-70-5/SOT-353)
CASE 419A-02
ISSUE M

DATE 11 APR 2023



RECOMMENDED
MOUNTING FOOTPRINT

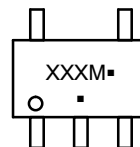
* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30

GENERIC MARKING
DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

STYLE 1:

- PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:

- PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:

- PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:

- PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:

- PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:

- PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:

- PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:

- PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

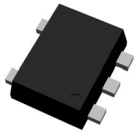
STYLE 9:

- PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

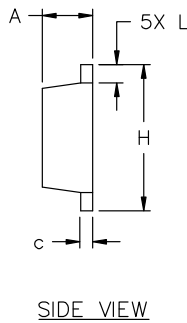
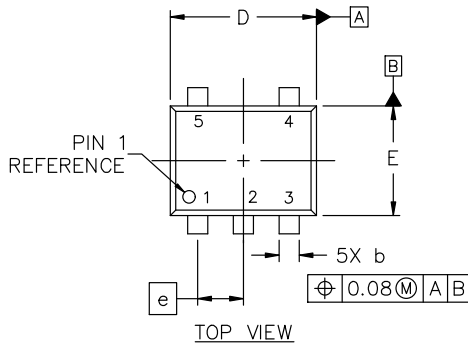
Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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DESCRIPTION:	SC-88A (SC-70-5/SOT-353)	PAGE 1 OF 1

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SOT-553-5 1.60x1.20x0.55, 0.50P
CASE 463B
ISSUE D

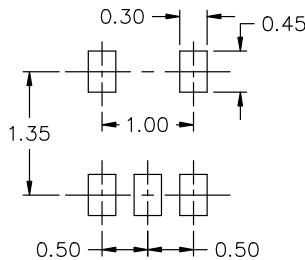
DATE 21 FEB 2024



NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
b	0.17	0.22	0.27
c	0.08	0.13	0.18
D	1.55	1.60	1.65
E	1.15	1.20	1.25
e	0.50 BSC		
H	1.55	1.60	1.65
L	0.10	0.20	0.30



RECOMMENDED MOUNTING FOOTPRINT*

- * FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

GENERIC MARKING DIAGRAM*


XX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR 1
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

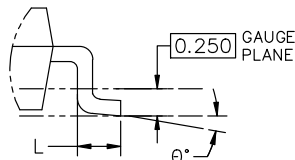
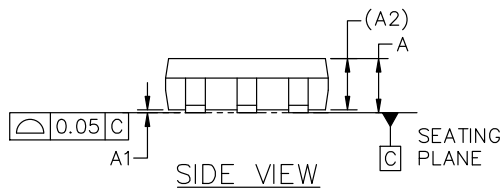
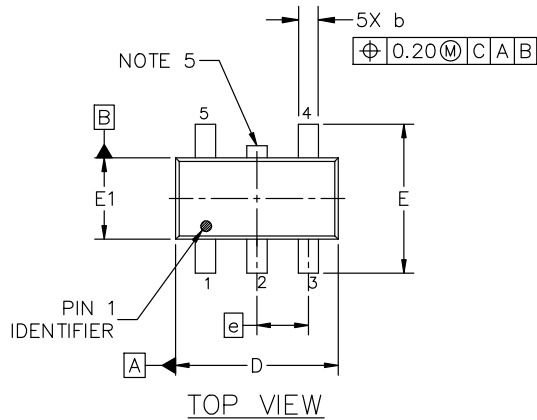
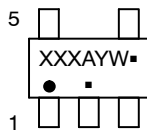
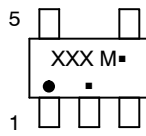
STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

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TSOP-5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

DATE 01 APR 2024


GENERIC
MARKING DIAGRAM*

Analog

Discrete/Logic

XXX = Specific Device Code XXX = Specific Device Code
A = Assembly Location M = Date Code
Y = Year ■ = Pb-Free Package
W = Work Week
■ = Pb-Free Package

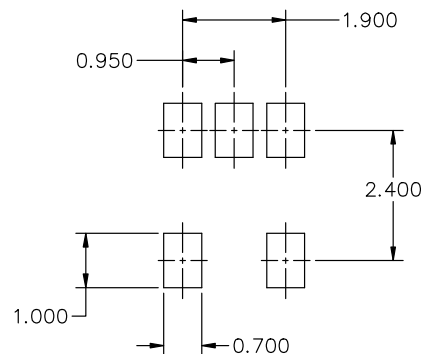
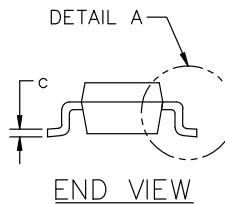
(Note: Microdot may be in either location)

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3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2	0.950 REF.		
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e	0.950 BSC		
L	0.200	0.400	0.600
θ	0°	5°	10°


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