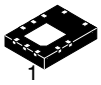
# PWM Controller, Input Current Mode, Ultra Wide

# NCP12700



WQFN10
MT SUFFIX
CASE 511DV

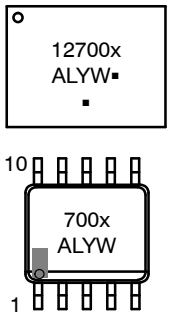


MSOP
DN SUFFIX
CASE 846AE

The NCP12700 is a fixed frequency, peak current mode, PWM controller containing all of the features necessary for implementing single−ended power converter topologies. The device features a high voltage startup capable of operating over a wide input range and supplying at least 15 mA to provide temporary bias to $V_{CC}$ during system startup. The device contains a programmable oscillator capable of operating from 100 kHz to 1 MHz and integrates slope compensation to prevent subharmonic oscillations. The controller offers an adjustable soft−start, input voltage UVLO protection, and an adjustable Over−Power Protection circuit which limits the total power capability of the circuit as the input voltage increases, easing the system thermal design. The UVLO pin also features a shutdown comparator which allows for an external signal to disable switching and bring the controller into a low quiescent state.

The NCP12700 contains a suite of protection features including cycle−by−cycle peak current limiting, timer−based overload protection, and a FLT pin which can be interfaced with an NTC and an auxiliary winding to provide system thermal protection and output over−voltage protection. All protection features place the device into a low quiescent fault mode and recovery from fault mode is dependent on the device option.

## MARKING DIAGRAMS




12700 or 700 = Specific Device Code
x = A, B or C
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

## ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

### Common General Features

- Wide Input Range (9 – 120/200 V; MSOP10/WQFN10)
- Startup Regulator Circuit with 15 mA Capability
- Current Mode Control with Integrated Slope Compensation
- Suitable for Flyback or Forward Converters
- Single Resistor Programmable Oscillator
- 1 A / 2.8 A Source / Sink Gate Driver
- User Adjustable Soft−Start Ramp
- Input Voltage UVLO with Hysteresis
- Shutdown Threshold for External Disable
- Skip Cycle Mode for Low Standby Power
- This is a Pb−Free Device

### Fault Protection Features

- User Adjustable Over−Power Protection
- Overload Protection with 30 ms Overload Timer
- NTC−Compatible Fault Interface for Thermal Protection
- Output OVP Fault Interface
- Fault Auto−recovery Mode with 1 s Auto−recovery Period

### Typical Applications

- Single−ended Power Converters including CCM/DCM Flyback and Forward Converters
- Telecommunications Power Converters
- Industrial Power Converter Modules
- Transportation & Railway Power Modules
- Power over Ethernet Powered Devices (PoE PD)

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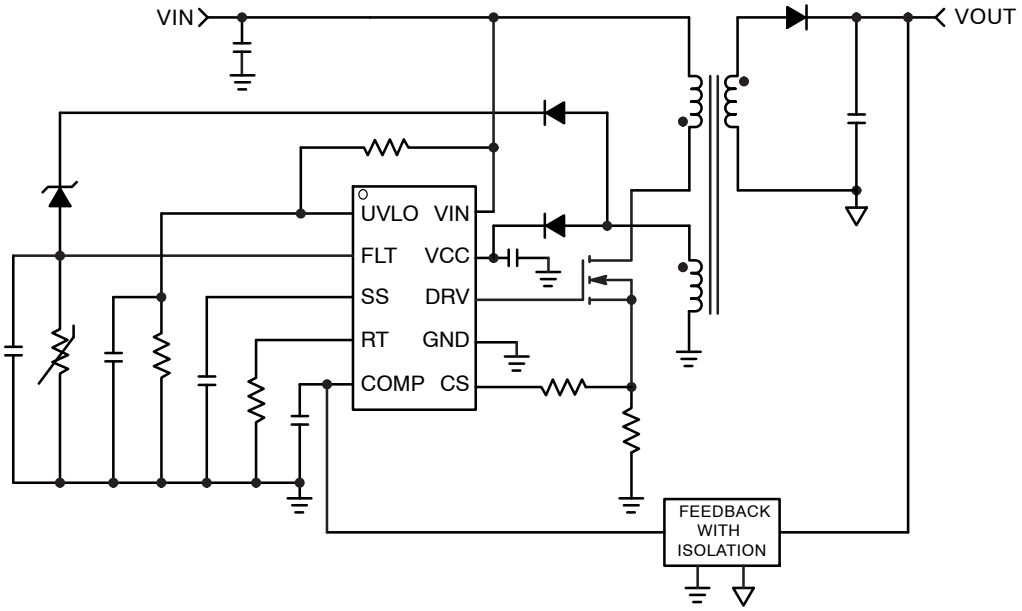



**Figure 1. Typical Application Circuit for Vin = 12 – 160 V**

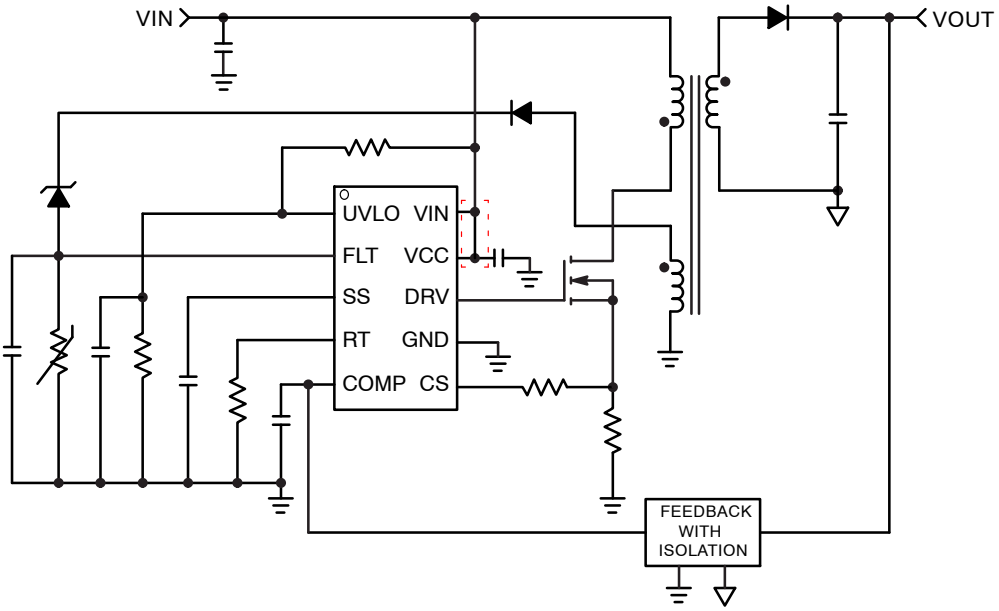



**Figure 2. Typical Application Circuit for Vin = 9 – 18 V**



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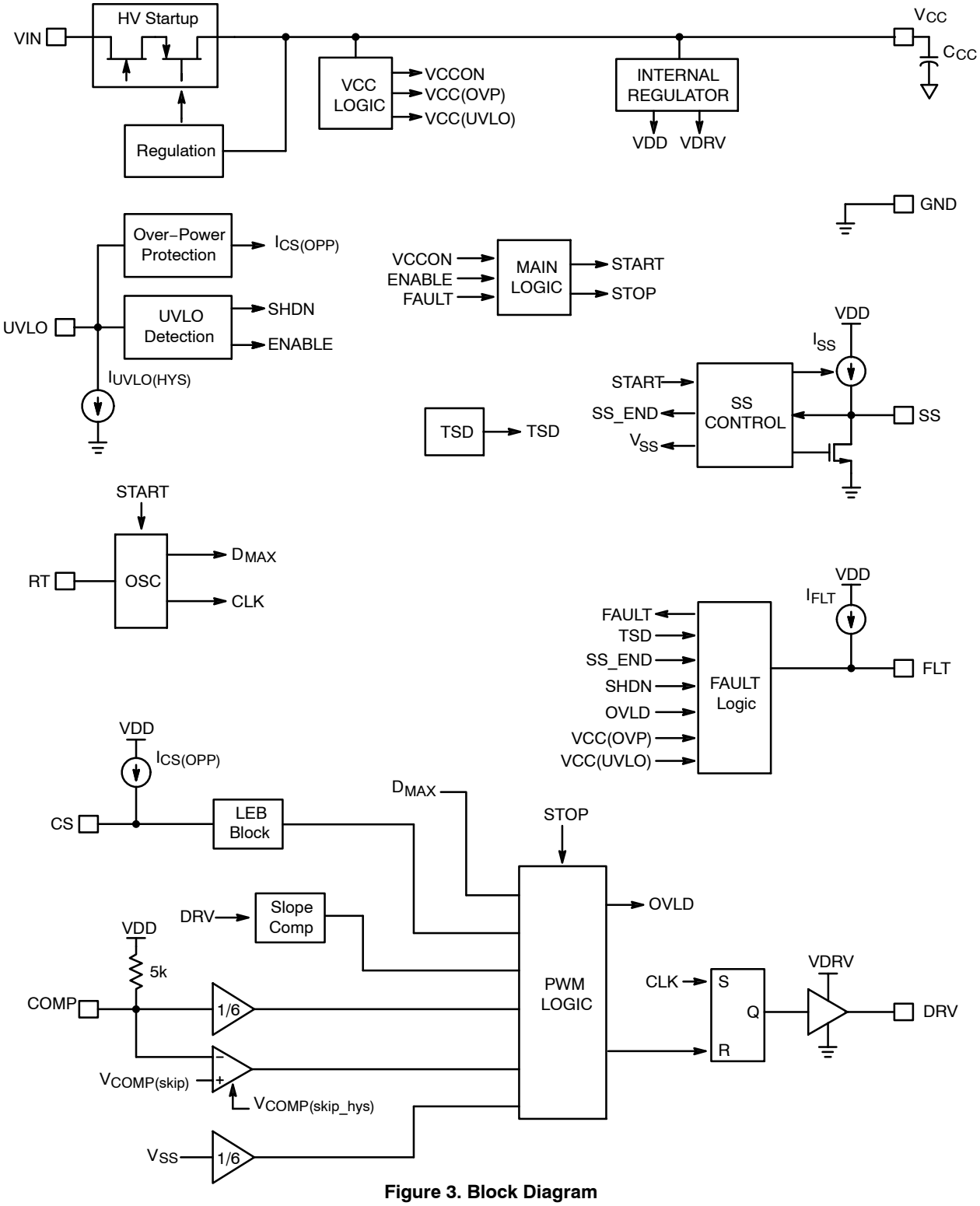
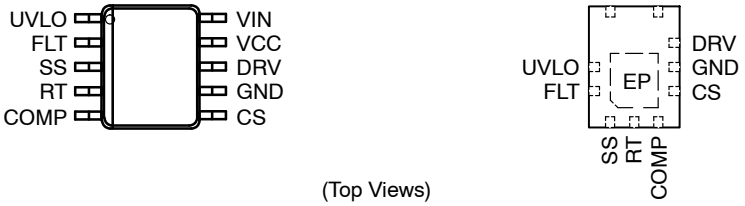



**Figure 3. Block Diagram**



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## PINOUTS




(Top Views)

**Table 1. PIN FUNCTION DESCRIPTION**

| MSOP10 | WQFN10 | Pin Name | Pin Description |
|---|---|---|---|
| 1 | 9 | UVLO | The UVLO pin is the input to the Standby and UVLO comparators. A resistor divider between the power supply input voltage and ground is connected to the UVLO pin to set the input voltage level at which the controller will be enabled. UVLO Hysteresis is set by a 5 μA pull−down current source. An externally supplied pull−down signal can also be used to disable the controller. The UVLO pin is also used to determine the Over−Power Protection current supplied to the CS pin. |
| 2 | 10 | FLT | The FLT pin is the input to a window comparator which provides an upper and lower fault threshold. When either threshold is tripped, the controller enters the fault mode which can be a permanent latch off or a minimum 1 s auto−recovery period. A precision current source is output from the FLT pin allowing an NTC to ground to be placed at the pin for system Over−temperature protection. The upper threshold can be used for output over−voltage protection sensed through the auxiliary winding or as a general purpose fault. |
| 3 | 1 | SS | The SS pin sets the soft−start ramp of the peak current limit when the controller is enabled. An internal 15 μA current source and an external capacitor to ground are used to control the ramp rate. Typical soft start capacitor values will be in the range of 10 nF to 100 nF. |
| 4 | 2 | RT | The RT pin sets the oscillator frequency in the controller. This pin requires a resistor to ground located close to the IC. Typical RT values are in the range of 10 kΩ − 100 kΩ. |
| 5 | 3 | COMP | The COMP pin provides the compensated error voltage for the PWM and Skip comparators. An internal 5 kΩ pull−up resistor is connected to the COMP pin and can be used to bias the transistor of an opto−coupler. |
| 6 | 4 | CS | The CS pin is the current sense input for the PWM and Current Limit comparators. The comparator input is held low for 60 ns after the DRV goes high to prevent leading edge current spikes from tripping the comparators. An external low pass filter is recommended for improved noise immunity. The external filter resistor is also used to determine the amount of Over−Power Protection applied to the current sense. |
| 7 | 5 | GND | This pin is the controller ground. For the WQFN package the exposed pad (EP) should be connected to GND. |
| 8 | 6 | DRV | The DRV pin is a high current output used to drive the external MOSFET gate. DRV has source and sink capability of 1 A and 2.8 A, respectively. |
| 9 | 7 | VCC | The VCC pin provides bias to the controller. An external decoupling capacitor to ground in the range of 1 − 10 μF is recommended. |
| 10 | 8 | VIN | The VIN pin is the input to the high voltage startup regulator. The regulator is capable of sourcing > 15 mA to temporarily bias VCC while the application is starting up. |

## ORDERING INFORMATION

| Device | Package | $V_{CS(LIM)}$ | OTP Fault | OVP Fault | Shipping† |
|---|---|---|---|---|---|
| NCP12700ADNR2G | MSOP10 | 495 mV | Latch | Latch | 4000 / Tape & Reel |
| NCP12700BDNR2G | MSOP10 | 495 mV | Autorecovery | Autorecovery | 4000 / Tape & Reel |
| NCP12700CDNR2G (In Development) | MSOP10 | 250 mV | Autorecovery | Autorecovery | 4000 / Tape & Reel |
| NCP12700BMTTXG | WQFN10 | 495 mV | Autorecovery | Autorecovery | 3000 / Tape & Reel |
| NCP12700CMTTXG (In Development) | WQFN10 | 250 mV | Autorecovery | Autorecovery | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.



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**Table 2. MAXIMUM RATINGS**

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| High Voltage Startup Voltage | (MSOP10)<br>(WQFN10) | $V_{IN(MAX)}$ | 120<br>200 | V |
| High Voltage Startup Current | | $I_{IN(MAX)}$ | 50 | mA |
| Supply Voltage | | $V_{CC(MAX)}$ | −0.3 to 30 | V |
| Supply Current | | $I_{CC(MAX)}$ | 50 | mA |
| DRV Voltage (Note 1) | | $V_{DRV(MAX)}$ | −0.3 V to $V_{DRV(high)}$ | V |
| DRV Current (Peak) | | $I_{DRV(MAX)}$ | 3.25 | A |
| FLT Voltage | | $V_{FLT(MAX)}$ | $V_{CC}$ + 1.25 | V |
| FLT Current | | $I_{FLT(MAX)}$ | 10 | mA |
| Max Voltage on Signal Pins | | $V_{SIG(MAX)}$ | −0.3 to 5.5 | V |
| Max Current on Signal Pins | | $I_{SIG(MAX)}$ | 10 | mA |
| Thermal Resistance Junction−to−Air (Note 2) | (MSOP10)<br>(WQFN10) | $R_{\theta J-A}$ | 165<br>51 | °C/W |
| Junction−to−Top Thermal Characterization Parameter | (MSOP10)<br>(WQFN10) | $\Psi_{J-C}$ | 10<br>12 | °C/W |
| Maximum Junction Temperature | | $T_{JMAX}$ | 150 | °C |
| Maximum Power Dissipation | (MSOP10)<br>(WQFN10) | $P_D$ | Internally Limited | W |
| Storage Temperature Range | | $T_{STG}$ | −55 to 150 | °C |
| Operating Temperature Range | | $T_J$ | −40 to 125 | °C |
| ESD Capability (Note 3)<br>Human Body Model per JEDEC Standard JESD22−A114E<br>Charge Device Model per JEDEC Standard JESD22−C101E | | | <br>2000<br>1000 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum driver voltage is limited by the driver clamp voltage, $V_{DRV(high)}$, when $V_{CC}$ exceeds the driver clamp voltage. Otherwise, the maximum driver voltage is $V_{CC}$.
2. Per JEDEC specification JESD51.7 using two 1 oz copper planes with board size = 80x80x1.6 mm
3. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per JEDEC Standard JESD22−A114E
   Charge Device Model TBD per JEDEC Standard JESD22−C101E
4. This device contains latch−up protection and has been tested per JEDEC JESD78D, Class I and exceeds +/−100 mA (TBD).

**Table 3. RECOMMENDED OPERATING CONDITIONS**

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| VIN Voltage | (MSOP10)<br>(WQFN10) | $V_{IN}$ | 9 – 100<br>12 – 160 | V |
| Supply Voltage − All | | $V_{CC}$ | 9 – 20 V | V |
| Operating Temperature Range | | $T_J$ | −40 to 125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.



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**Table 4. ELECTRICAL CHARACTERISTICS** ($V_{IN}$ = 12 V, $V_{CC}$ = 12 V, $V_{COMP}$ = Open, $V_{FLT}$ = Open, $C_{DRV}$ = 1 nF, $R_T$ = 49.9k, $V_{CS}$ = 0 V, $V_{SS}$ = Open, $V_{UVLO}$ = 1.2, for typical values $T_J$ = 25°C, for min/max values, $T_J$ is – **40**°C to **125**°C, unless otherwise noted)

| Characteristics | Test Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **HIGH VOLTAGE STARTUP REGULATOR** | | | | | | |
| Regulated Voltage | $V_{CC}$ = Open, $I_{CC}$ = 5 mA | $V_{CC(REG)}$ | 7.6 | 8 | 8.4 | V |
| Current Source Capability | $V_{IN}$ = 9 V, $V_{CC}$ = 7 V | $I_{VIN(SRC)}$ | 15 | | | mA |
| Current Source Limit | $V_{CC}$ = $V_{CC(off)}$ + 100 mV | $I_{VIN(LIM)}$ | | 30 | | mA |
| Off−State Leakage Current (xMTTXG) | $V_{CC}$ = Open, $V_{IN}$ = 160 V, $V_{UVLO}$ = 0 | $I_{VIN(OFF)}$ | | | 100 | μA |
| Off−State Leakage Current (xDNR2G) | $V_{CC}$ = Open, $V_{IN}$ = 120 V, $V_{UVLO}$ = 0 | $I_{VIN(OFF)}$ | | | 100 | μA |
| **SUPPLY CIRCUIT** | | | | | | |
| Supply Voltage<br>Startup Threshold<br><br>Minimum Operating Voltage | <br>$V_{CC}$ increasing<br><br>$V_{CC}$ decreasing | <br>$V_{CC(on)}$<br><br>$V_{CC(off)}$ | <br>$V_{CC(REG)}$ – 350 mV<br><br>6.2 | <br><br>6.5 | <br>$V_{CC(REG)}$ – 100 mV<br><br>6.8 | V |
| Supply Over−Voltage Protection | | $V_{CC(OVP)}$ | | 28 | | V |
| VCC OVP Detection Filter Delay | | $t_{VCCOVP(DLY)}$ | | 3 | | μs |
| Startup Delay | Measured from $V_{CC(ON)}$ to SS | $t_{ON(Dly)}$ | | | 25 | μs |
| Supply Current<br>SHDN<br>STBY<br>Enable<br>Fault | <br>$V_{UVLO}$ = 0 V<br>$V_{UVLO}$ = 0.7 V<br>$C_{DRV}$ = Open, $V_{COMP}$ = 2 V<br>$V_{FLT}$ = 0 V | <br>$I_{CC(SHDN)}$<br>$I_{CC(STBY)}$<br>$I_{CC(EN)}$<br>$I_{CC(FLT)}$ | <br>–<br>–<br>–<br>– | <br>–<br>–<br>–<br>– | <br>50<br>750<br>4<br>500 | <br>μA<br>μA<br>mA<br>μA |
| **CURRENT SENSE** | | | | | | |
| Current Limit Comparator Threshold | NCP12700CDNR2G<br>Other parts | $V_{CS(LIM)}$ | 235<br>465 | 250<br>495 | 265<br>525 | mV |
| Propagation Delay From Current Sense Limit to DRV Low | Step $V_{CS}$ from 0 – 0.6 V | $t_{CS(DLY)}$ | – | – | 75 | ns |
| Short Circuit Protection (SCP) Current Limit Threshold | NCP12700CDNR2G<br>Other parts | $V_{SCP(LIM)}$ | | 312.5<br>625 | | mV |
| Propagation Delay From Short Circuit Limit to DRV Low | $V_{CS}$ = 0.75 V | $t_{SCP(DLY)}$ | – | – | 75 | ns |
| Short Circuit Counter | $V_{CS}$ = 0.75 V | $N_{SCP}$ | | 4 | | |
| CS Leading Edge Blanking (LEB) | | $t_{LEB(CS)}$ | 75 | 100 | 125 | ns |
| SCP Leading Edge Blanking | | $t_{LEB(SCP)}$ | 45 | 60 | 75 | ns |
| CS LEB Pull−down Resistance | | $R_{PD(LEB)}$ | | – | 55 | Ω |
| Overload Timer Duration | $V_{CS}$ = 0.6 V | $t_{CS(OVLD)}$ | 24 | 30 | 36 | ms |
| Applied Slope Compensation @ Current Limit Comparator | $V_{COMP}$ = Open; Measured at $D_{80\%}$<br>NCP12700CDNR2G<br>Other parts | $V_{SLP(ILIM)}$ | <br>35<br>83 | <br>50<br>102 | <br>65<br>123 | mV |
| Duty Cycle Where Slope Compensating Ramp Begins | | $D_{40\%}$ | | 40 | | % |
| **COMP SECTION** | | | | | | |
| PWM to COMP Gain Through Resistor Divider | $V_{COMP}$ = 2 V | $K_{PWM}$ | | 6 | | |
| PWM Propagation Delay to DRV Low | $V_{COMP}$ = 2 V, Step from CS 0– 0.4 V | $t_{PWM(Dly)}$ | | – | 75 | ns |
| COMP Open Pin Voltage | | $V_{COMP(open)}$ | 4 | 4.7 | | V |
| COMP Output Current | $V_{COMP}$ = 0 | $I_{COMP}$ | 0.84 | 1 | 1.2 | mA |
| Maximum Duty Cycle | $V_{COMP}$ = Open | $D_{MAX}$ | 76 | 80 | 84 | % |



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**Table 4. ELECTRICAL CHARACTERISTICS** ($V_{IN}$ = 12 V, $V_{CC}$ = 12 V, $V_{COMP}$ = Open, $V_{FLT}$ = Open, $C_{DRV}$ = 1 nF, $R_T$ = 49.9k, $V_{CS}$ = 0 V, $V_{SS}$ = Open, $V_{UVLO}$ = 1.2, for typical values $T_J$ = 25°C, for min/max values, $T_J$ is – **40**°C to **125**°C, unless otherwise noted)

| Characteristics | Test Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **COMP SECTION** | | | | | | |
| COMP Skip Threshold | | $V_{COMP(skip)}$ | | 300 | | mV |
| COMP Skip Hysteresis | | $V_{COMP\ (skip_hys)}$ | | 25 | | mV |
| Minimum Duty Cycle | $V_{COMP}$ = 0 | $D_{MIN}$ | | | 0 | % |
| Applied Slope Compensation @ PWM Comparator | $V_{COMP}$ = 2 V; Measured at $D_{80\%}$<br>NCP12700CDNR2G<br>Other parts | $V_{SLP(PWM)}$ | <br>30<br>77 | <br>40<br>98 | <br>50<br>117 | mV |
| **SOFT START** | | | | | | |
| Soft−Start Open Pin Voltage | | $V_{SS(open)}$ | | 5.0 | | V |
| Soft−Start End Threshold | | $V_{SS(end)}$ | 2.85 | 3 | 3.15 | V |
| Soft−Start Current | $V_{SS}$ = 3 V | $I_{SS}$ | 12 | 15 | 18 | μA |
| Soft−Start to CS Divider | NCP12700CDNR2G<br>Other parts | $K_{SS}$ | | 12<br>6 | | |
| Soft−Start Discharge Resistance | | $R_{SS(DIS)}$ | | | 100 | Ω |
| **OSCILLATOR** | | | | | | |
| Oscillator Frequency 1 | | $F_{OSC1}$ | 185 | 200 | 215 | kHz |
| Oscillator Frequency 2 | $R_T$ = 100 kΩ | $F_{OSC2}$ | 95 | 100 | 105 | kHz |
| Oscillator Frequency 3 | $R_T$ = 20 kΩ | $F_{OSC3}$ | 450 | 500 | 550 | kHz |
| Oscillator Frequency 4 | $R_T$ = 9.09 kΩ | $F_{OSC4}$ | | 1000 | | kHz |
| **UNDER−VOLTAGE LOCKOUT (UVLO)** | | | | | | |
| Standby Threshold | $V_{UVLO}$ increasing | $V_{STBY(th)}$ | 0.35 | 0.5 | 0.65 | V |
| Reset Threshold | $V_{UVLO}$ decreasing | $V_{RST(th)}$ | 0.3 | 0.45 | 0.6 | V |
| Standby Hysteresis | $V_{UVLO}$ decreasing | $V_{STBY(HYS)}$ | | 50 | | mV |
| Standby Detection RC Filter | | $t_{STBY(DLY)}$ | | 5 | | μs |
| UVLO Threshold | $V_{UVLO}$ increasing | $V_{UVLO(th)}$ | 765 | 800 | 830 | mV |
| UVLO Threshold Hysteresis | $V_{UVLO}$ decreasing | $V_{UVLO(HYS)}$ | | 15 | | mV |
| UVLO Hysteresis Current | | $I_{UVLO(HYS)}$ | 4.5 | 5 | 5.5 | μA |
| UVLO Detection Delay Filter | $V_{UVLO}$ = $V_{UVLO(th)}$ – 20 mV | $t_{UVLO(DLY)}$ | 0.5 | | 1 | μs |
| **OVER−POWER PROTECTION (OPP)** | | | | | | |
| UVLO Voltage Above Which OPP Applied | | $V_{OPP(START)}$ | | 1 | | V |
| OPP Gain | | $Gm_{(OPP)}$ | 135 | 150 | 165 | μA / V |
| Maximum Current (Operating Point) | $V_{UVLO}$ = 2.33 V | $I_{CS(OPP1)}$ | 180 | 200 | 220 | μA |
| Maximum Current | $V_{UVLO}$ = 4 V | $I_{CS\ (OPP_MAX)}$ | | 200 | | μA |
| COMP Threshold Voltage Above Which OPP is Applied | | $V_{OPP(0\%)}$ | | 0.8 | | V |
| COMP Threshold Voltage For 100% OPP | | $V_{OPP(100\%)}$ | | 2 | | V |
| **GATE DRIVE** | | | | | | |
| DRV Rise Time | $V_{DRV}$ = 1.2 V to 10.8 V | $t_{DRV(rise)}$ | 6 | 10 | 15 | ns |
| DRV Fall Time | $V_{DRV}$ = 10.8 V to 1.2 V | $t_{DRV(fall)}$ | 2.5 | 4 | 10 | ns |
| DRV Source Current | $V_{DRV}$ = 6 V | $I_{DRV(SRC)}$ | | 1.0 | | A |



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**Table 4. ELECTRICAL CHARACTERISTICS** ($V_{IN}$ = 12 V, $V_{CC}$ = 12 V, $V_{COMP}$ = Open, $V_{FLT}$ = Open, $C_{DRV}$ = 1 nF, $R_T$ = 49.9k, $V_{CS}$ = 0 V, $V_{SS}$ = Open, $V_{UVLO}$ = 1.2, for typical values $T_J$ = 25°C, for min/max values, $T_J$ is − **40**°C to **125**°C, unless otherwise noted)

| Characteristics | Test Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **GATE DRIVE** | | | | | | |
| DRV Sink Current | $V_{DRV}$ = 6 V | $I_{DRV(SNK)}$ | | 2.8 | | A |
| DRV Clamp Voltage | $V_{CC}$ = 20 V, $R_{DRV}$ = 10 kΩ | $V_{DRV(clamp)}$ | 10 | 12 | 14 | V |
| Minimum DRV Voltage | $V_{CC}$ = $V_{CC(OFF)}$ + 100 mV, $R_{DRV}$ = 10 kΩ | $V_{DRV(MIN)}$ | 6 | | | V |
| **FAULT PROTECTION** | | | | | | |
| Fault Source Current | | $I_{FLT}$ | 80 | 85 | 90 | μA |
| OTP Fault Threshold | | $V_{FLT(OTP)}$ | 0.47 | 0.5 | 0.53 | V |
| OTP Detection Filter Delay | | $t_{OTP(DLY)}$ | 10 | 20 | 30 | μs |
| OTP Fault Recovery Threshold | | $V_{FLT(REC)}$ | 0.846 | 0.9 | 0.954 | V |
| OVP Fault Threshold | | $V_{FLT(OVP)}$ | 2.8 | 3 | 3.2 | V |
| OVP Detection Filter Delay | | $t_{OVP(DLY)}$ | 3 | 5 | 7 | μs |
| Fault Clamp Voltage | $V_{FLT}$ = Open | $V_{FLT(CLAMP)}$ | 1.13 | 1.35 | 1.57 | V |
| Fault Clamp Resistance | | $R_{FLT(CLAMP)}$ | | 1.6 | | kΩ |
| Auto−recovery Timer | | $t_{AR}$ | 0.8 | 1 | 1.2 | s |
| **THERMAL SHUTDOWN** | | | | | | |
| Thermal Shutdown | | $T_{SHDN}$ | 150 | 165 | 180 | °C |
| Thermal Shutdown Hysteresis | | $T_{SHDN(hys)}$ | | 25 | | °C |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



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## APPLICATION INFORMATION

The NCP12700 is a fixed frequency, peak current mode, PWM controller containing all of the features necessary for implementing single−ended power converter topologies. The device features an ultra−wide range, high voltage startup regulator capable of regulating $V_{CC}$ across an input voltage range of 9 – 120 V (xDNR2G) or 9 – 200 V (xMTTXG). The controller is designed for high speed operation including a programmable oscillator capable of operating from 100 kHz to 1 MHz and total propagation delays less than 75 ns in the PWM path. The NCP12700 integrates slope compensation to prevent subharmonic oscillations and an Input Voltage Compensation / Over−Power Protection (OPP) feature that limits the converter power delivery capability across input voltage, easing system thermal design. The controller offers an adjustable soft−start, input voltage UVLO protection, and a suite of protection features including cycle−by−cycle current limit and a FLT pin with a NTC interface for system thermal protection. The UVLO pin also features a shutdown comparator which allows for an externally applied pull−down signal to disable switching and bring the controller into a low quiescent state.

### Ultra−Wide Range HV Startup Regulator

The NCP12700 features a high voltage startup regulator capable of operating across input voltage ranges of 9−120 V (xDNR2G) or 9−200 V (xMTTXG). The ultra−wide range capability of the regulator allows for direct connection of VIN to the converter input voltage without requiring external components. The regulator's input voltage capabilities support a wide range of industrial, medical, telecom, and transportation applications.

Figure 4 details the operation of the startup regulator. When VIN is applied, the regulator will immediately begin sourcing current to charge $V_{CC}$. Initially the startup will supply approximately 10 mA. Once $V_{CC}$ builds up to ~ 3 V, the control loop for the HV regulator will activate and the source current will be regulated to 30 mA until $V_{CC}$ reaches the $V_{CC(REG)}$ level of 8 V. The HV startup is a linear regulator which can continue to supply and regulate $V_{CC}$ at 8 V. The recommended $V_{CC}$ capacitance to ensure stability of the regulator is 1 – 10 μF.

While the $V_{CC}$ voltage is below the $V_{CC(ON)}$ threshold the controller will remain in a low quiescent state to allow for rapid charging of $V_{CC}$ and fast startup of the application. Once the $V_{CC}$ voltage reaches the $V_{CC(ON)}$ threshold, approximately 200 mV below the $V_{CC(REG)}$ level, the controller will exit the low quiescent state and begin delivering drive pulses. While the output voltage is building up, the startup regulator will continue to supply the current necessary to maintain $V_{CC}$ at the $V_{CC(REG)}$ level. For low input voltage applications, the startup regulator has been designed to guarantee a minimum of 15 mA source capability with 2 V of headroom.

In typical applications an auxiliary winding will be used to provide bias to $V_{CC}$ once the converter is switching. This allows for the most efficient operation of the system. Once the auxiliary winding pulls the $V_{CC}$ voltage above $V_{CC(REG)}$, the HV regulator will shut off. In normal operation the $V_{CC}$ voltage can be biased above the voltage at VIN and can support voltages up to 28 V. A $V_{CC}$ OVP protection feature will trigger at 28 V, disabling switching of the converter to prevent the auxiliary winding voltage from damaging the controller.



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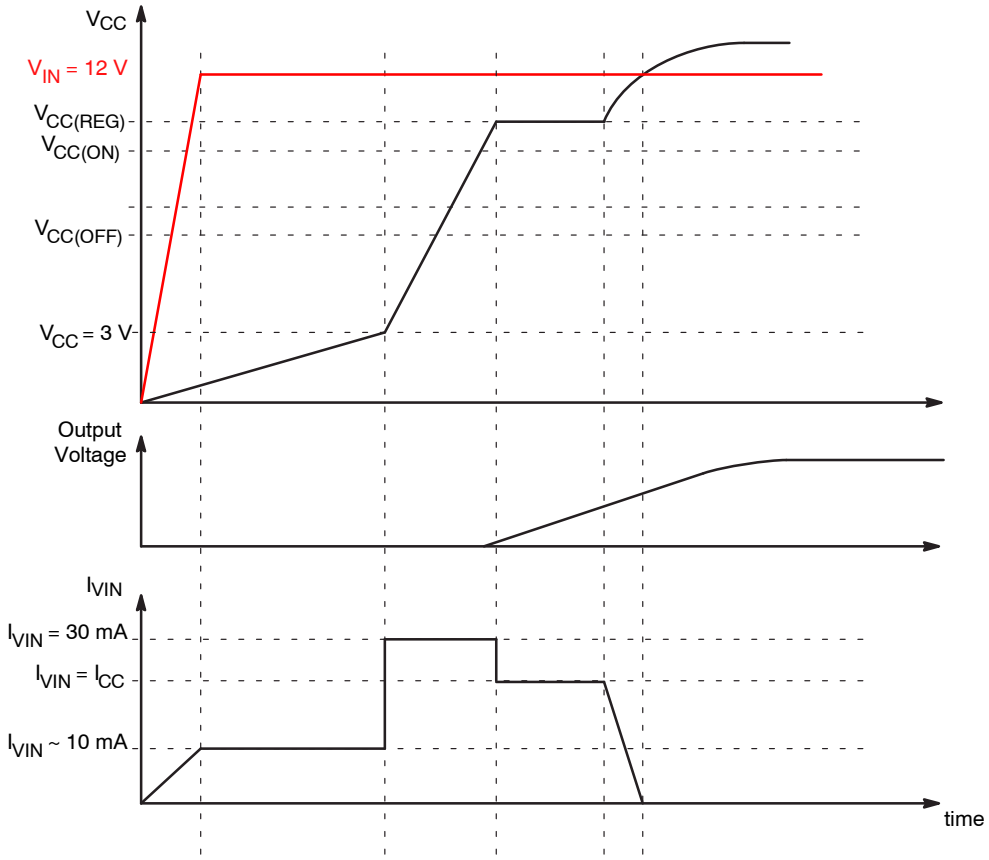



**Figure 4. Startup Timing Diagram**

Once the device has begun delivering drive pulses it will remain active as long as $V_{CC}$ remains above the $V_{CC(OFF)}$ threshold of 6.5 V. Either the auxiliary winding or the HV startup regulator will provide the bias necessary to keep $V_{CC}$ above this level. If $V_{CC}$ does drop below the $V_{CC(OFF)}$ threshold the controller will inhibit drive pulses, the device will reset and once again enter a low quiescent state. This should only occur if the input voltage to the converter has been removed but can also be an indication of excessive external loading on $V_{CC}$.

### Input Voltage UVLO Detection

The NCP12700 features line voltage UVLO detection to ensure that the converter becomes operational only after meeting a minimum input voltage threshold thereby protecting the converter from thermal stress at low input voltages. A functional block diagram of the UVLO detection circuitry is shown in Figure 5. The input line voltage is monitored through a resistor divider network allowing the user to set the thresholds for when to enable and disable the converter. Typical pull−down resistors in the divider network will be in the range of 5 – 20 kΩ and pull−up resistors will typically be in the range of 50 – 500 kΩ. External capacitive filtering on the order of 10 nF is also advisable.

When input voltage is initially applied to the converter the device will be in a shutdown/reset (SHDN) state until the UVLO voltage crosses the $V_{STBY(th)}$ threshold of 0.5 V. In the SHDN state the device consumption will be limited to the $I_{CC(SHDN)}$ value of 50 μA. When the UVLO voltage goes above $V_{STBY(th)}$ the device transitions into standby mode and the consumption increases to the $I_{CC(STBY)}$ limit of 750 μA maximum. The low current consumption in the shutdown and standby modes allow $V_{CC}$ to rapidly charge to the $V_{CC(ON)}$ threshold.

Once $V_{CC}$ has charged to $V_{CC(ON)}$ the device will enable drive pulses when the UVLO voltage exceeds the $V_{UVLO(th)}$ of 0.8 V and disables drive pulses when the UVLO voltage falls below 0.8 V by $V_{UVLO(HYS)}$. Prior to enabling drive pulses the device also activates a pull−down current source, $I_{UVLO(HYS)}$, of 5 μA. The current source works in combination with $V_{UVLO(HYS)}$ to set the input voltage hysteresis for enabling and disabling switching operation of the converter. A resistor, $R_{UVLO(HYS)}$, can be used to provide additional hysteresis between the enable and disable thresholds. Equation 1 and Equation 2 can be used to calculate the necessary component values in the resistor divider network.



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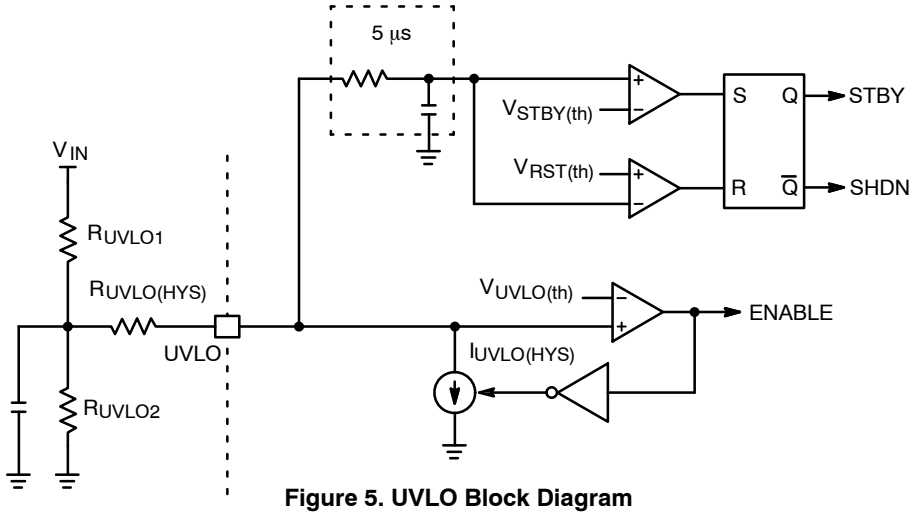



**Figure 5. UVLO Block Diagram**

$$V_{IN,START} = \left(V_{UVLO(th)} + \left(\frac{R_{UVLO1}R_{UVLO2}}{R_{UVLO1} + R_{UVLO2}} + R_{UVLO(HYS)}\right) \times I_{UVLO(HYS)}\right)\left(\frac{R_{UVLO1} + R_{UVLO2}}{R_{UVLO2}}\right) \quad \text{(eq. 1)}$$

$$V_{IN,STOP} = \left(V_{UVLO(th)} - V_{UVLO(HYS)}\right) \times \left(\frac{R_{UVLO1} + R_{UVLO2}}{R_{UVLO2}}\right) \quad \text{(eq. 2)}$$

### Input Voltage Compensation / Over−Power Protection

$$P = 0.5 \times L \times \left(I^2_P - I^2_V\right) \times f_{SW} \quad \text{(eq. 3)}$$

In a CCM flyback converter the output power capability is defined by Equation 3 where $I_P$ is the peak transformer current, $I_V$ is the valley or minimum transformer current, L is the primary inductance, and $f_{SW}$ is switching frequency. In a DCM flyback converter the valley current becomes 0 and Equation 3 still applies. The peak current capability of the converter can be impacted by several variables including input voltage and the operating duty cycle due to the internal slope compensation in the NCP12700. Managing the peak current limit over the operating input voltage range will limit the total power capability and ease system thermal design.

The NCP12700 features the Input Voltage Compensation / Over−Power Protection (OPP) circuitry shown in Figure 6. The Over−Power Protection circuit functions as a transconductance amplifier which senses an image of the input line voltage through the UVLO pin. When the UVLO voltage crosses the $V_{OPP(START)}$ threshold, typically 1 V, the OTA begins sourcing a current out of the CS pin. The current injected out of the CS pin will be according to Equation 4 where the typical transconductance, $G_{m(OPP)}$, is 150 μA/V and the maximum current is limited to the $I_{CS(OPP_MAX)}$ value of 200 μA.

$$I_{CS(OPP)} = G_{m(OPP)} \cdot \left(V_{UVLO} - V_{OPP(START)}\right) \quad \text{(eq. 4)}$$

Good SMPS design practice for current mode control includes a small RC filter in series between the current sense resistor and the CS pin of the controller. Typical values for the resistor in the RC filter are 500 – 1 kΩ. The user can then limit the peak current capability of the converter by setting the $R_{CS}$ resistor value and can reduce the peak current capability of the converter by 20 – 40% with these values.

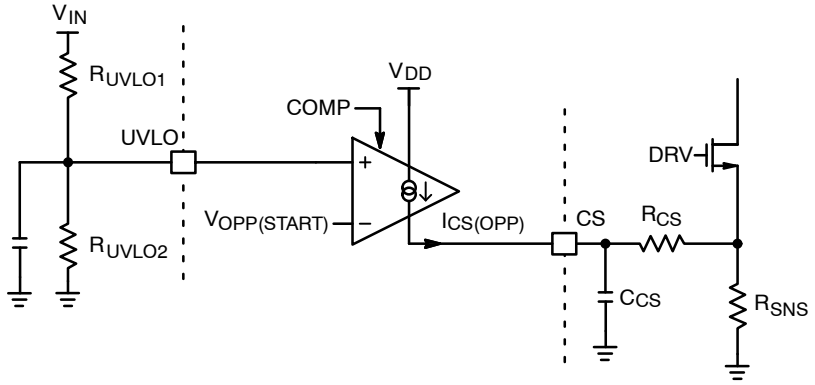



**Figure 6. Over−Power Protection Diagram**



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Another aspect of the Over−Power Protection feature is that the current sourced out of the CS pin is modulated as a function of the COMP voltage to ensure that the current is only available when necessary. This is detailed in Figure 7 below with typical values for $V_{OPP(0\%)}$ = 0.8 V and $V_{OPP(100\%)}$ = 2 V. The typical values of 0.8 V and 2 V equate to ~ 27% and 67% of the full load capability of the device, hence the OPP current should begin being applied at 27% load and should ramp up to 100% OPP current at 67% load.

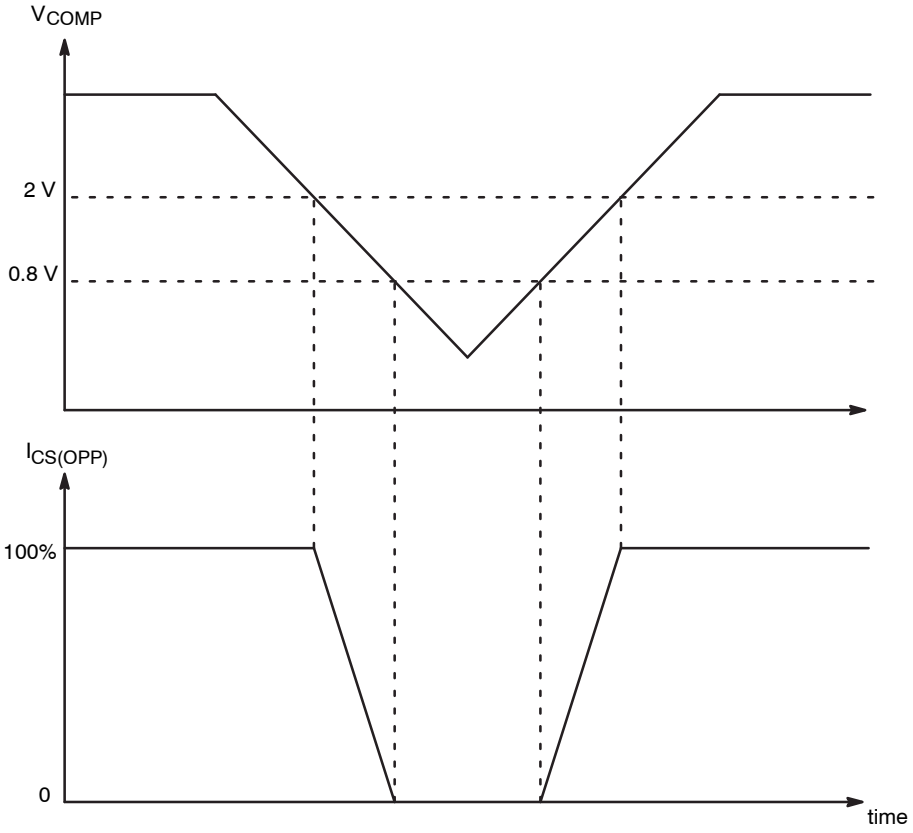



**Figure 7. OPP Current Profile vs. COMP Voltage**



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## PWM OPERATION

### RT Pin & Oscillator

The oscillator in the NCP12700 uses an external resistor from the RT pin to ground to set the switching frequency of the converter. The frequency set by the RT resistor follows

$$F_{OSC} = \frac{1}{RT \times 100 \times 10^{-12}} \quad \text{(eq. 5)}$$

where $F_{OSC}$ is the switching frequency. The curve in Figure 8 below shows the Oscillator frequency vs. RT resistor for values between ~10 kΩ to 100 kΩ. The NCP12700 is designed to operate between 100 kHz and 1 MHz but will have tighter tolerance at lower switching frequencies.

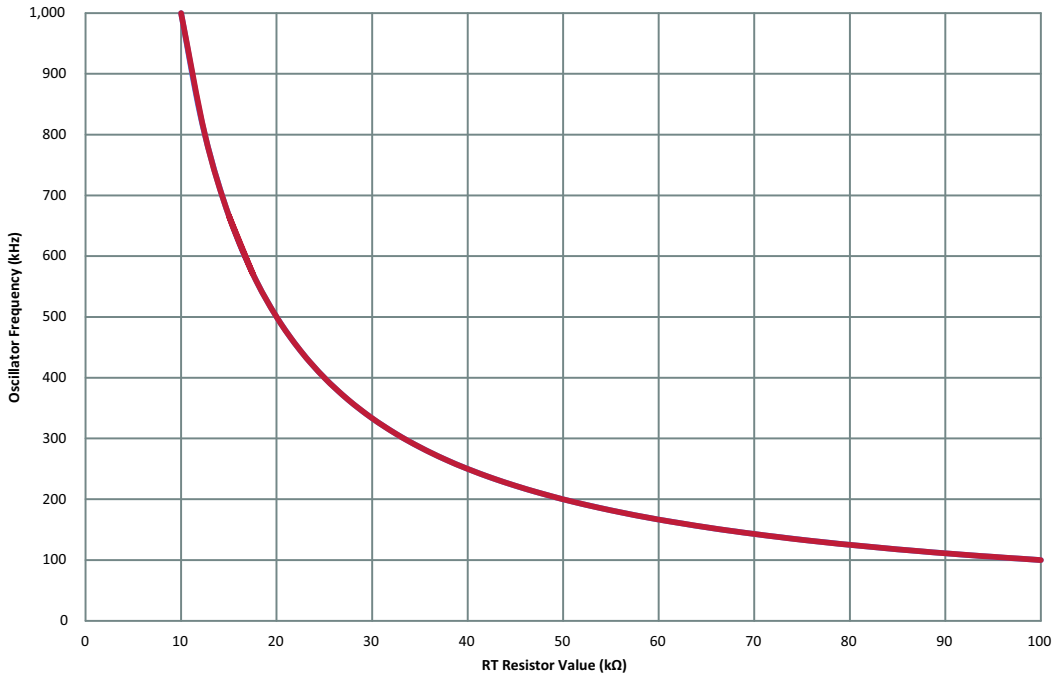



**Figure 8. Oscillator Frequency vs. RT Resistor Value**

### Gate Driver (DRV)

The NCP12700 is equipped with a gate driver for driving the primary side MOSFET. The driver applies $V_{CC}$ up to the clamped voltage, $V_{DRV(clamp)}$, of 12 V as a high signal and 0 V to the gate of the power MOSFET as a low signal. The rate of charging and discharging of the gate of the MOSFET is dependent upon the input capacitance of the MOSFET and the impedance of the driver. The NCP12700 is equipped with an $I_{DRV(SRC)}$ pull−up current, typically 1 A, and a pull down current of $I_{DRV(SNK)}$, typically 2.8 A ensuring fast turn on/off transitions of the power MOSFET and minimizing the switching losses.

### PWM Reset Path

The NCP12700 is intended for isolated DC−DC converters where the control loop compensation circuitry is located on the secondary side of the power converter. The converter output voltage is compared against a reference voltage and an error amplifier produces a compensated error signal which is communicated to the NCP12700 through an optocoupler. The compensated error signal interfaces with the COMP pin where it is divided down by a 5R/R voltage divider and sent to the PWM S/R to modulate the switching duty cycle. A detailed functional diagram of the PWM path is shown in Figure 9. The PWM comparator compares the attenuated error signal from the COMP pin to the current ramp signal sensed at the CS pin to determine when the drive pulse should be terminated. This comparator serves as the primary modulation path for the converter duty cycle.



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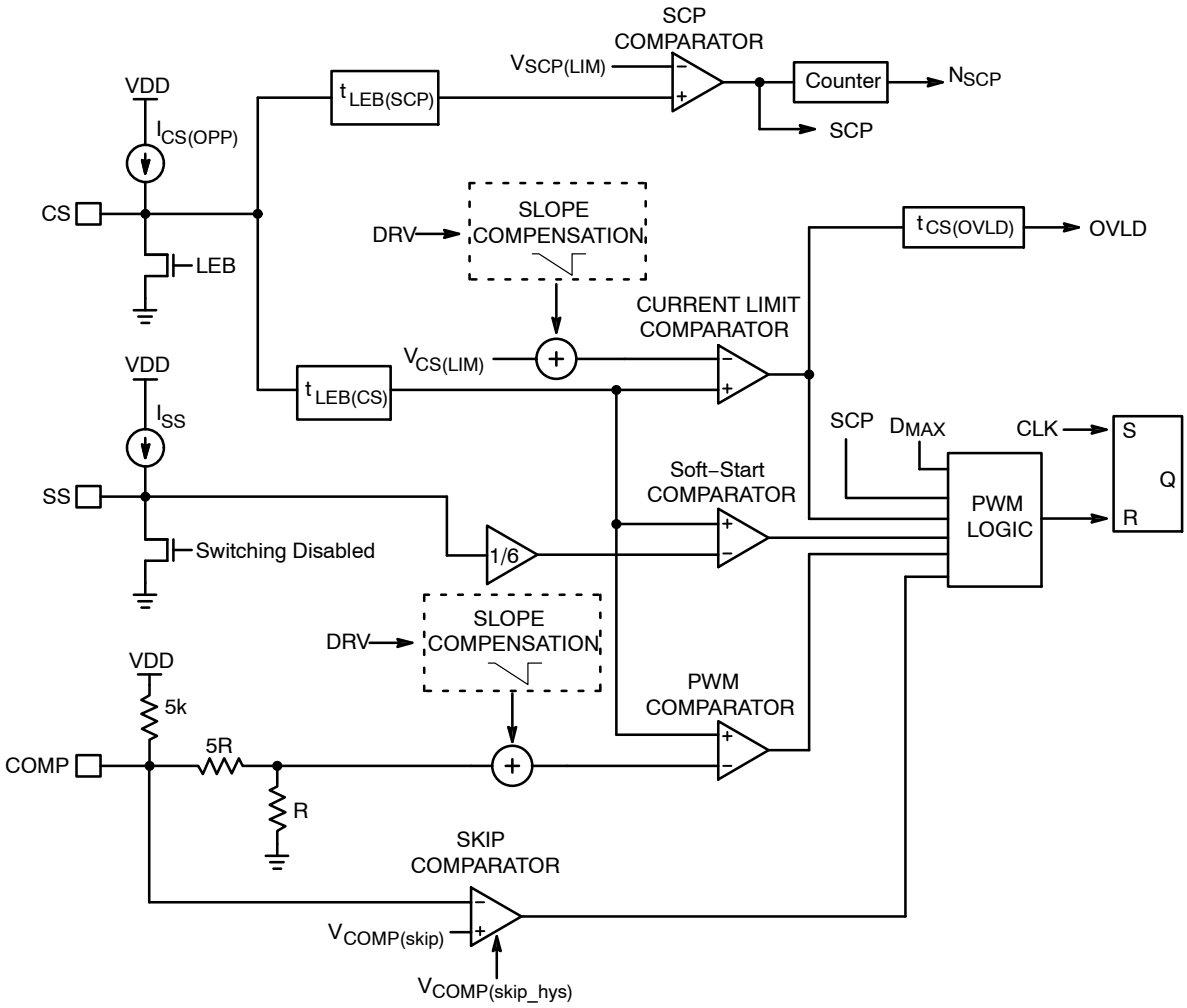



**Figure 9. NCP12700 PWM Path**

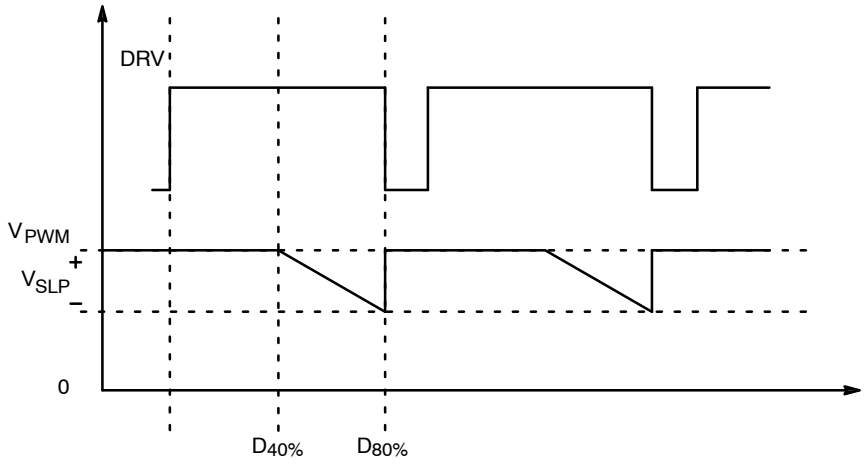



**Figure 10. Slope Compensation Timing Diagram**

### Slope Compensation

In fixed frequency peak current mode control, converters operating at duty cycles greater than 50% of the switching period are susceptible to sub−harmonic oscillation, characterized by successive switching cycles with alternating wide and narrow pulse−widths. To avoid sub−harmonic oscillation the NCP12700 implements an internal slope compensation circuit which is applied to the attenuated COMP signal at the input of the PWM comparator.

The slope compensation timing diagram is shown in Figure 10. The compensating ramp begins reducing the



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attenuated COMP voltage when the switching duty cycle is nominally 40% and reduces the voltage by a peak, $V_{SLP(PK)}$, at the 80% duty cycle limit. The slope compensating ramp is synchronized to the duty cycle of the oscillator, effectively adjusting itself based on the switching frequency, providing the converter with a compensating dv/dt ramp appropriate for the particular switching frequency. An image of the slope compensating ramp is also applied at the input of the Current Limit comparator to prevent sub−harmonic oscillations from occurring during overload conditions. The chart below summarizes the dv/dt of the compensating ramp at some common operating frequencies.

| $F_{SW}$ (kHz) | $T_{SW}$ (μs) | D = 40% (μs) | D = 80% (μs) | $V_{SLP}$ (mV) | Ramp (mV/μs) |
|---|---|---|---|---|---|
| 100 | 10.00 | 4.00 | 8.00 | 98 / 40 | 25 / 10 |
| 200 | 5.00 | 2.00 | 4.00 | 98 / 40 | 49 / 20 |
| 250 | 4.00 | 1.60 | 3.20 | 98 / 40 | 61 / 25 |
| 330 | 3.03 | 1.21 | 2.42 | 98 / 40 | 81 / 33 |
| 400 | 2.50 | 1.00 | 2.00 | 98 / 40 | 98 / 40 |
| 500 | 2.00 | 0.80 | 1.60 | 98 / 40 | 123 / 50 |

### Cycle−by−Cycle Current Limit and Overload Protection

The NCP12700 implements cycle−by−cycle current limiting with a dedicated Current Limit Comparator. The input to the comparator is the primary FET current ramp sensed at the CS pin. If the sensed voltage exceeds the current limit threshold, $V_{CS(LIM)}$, then the drive pulse is terminated. There are device options for $V_{CS(LIM)}$ of 250 mV and 495 mV. The Current Limit Comparator is very fast with a total propagation delay, $t_{CS(DLY)}$, of 75 ns maximum ensuring that drive pulses are quickly terminated minimizing current overshoot in the converter.

The Current Limit comparator also triggers an overload timer, $t_{CS(OVLD)}$, nominally 30 ms, and will disable drive pulses and take the device into a Fault mode when the timer has expired. The 30 ms timer allows the converter to sustain a short term overload but still protects the converter from thermal overstress in the event of a continuously applied overload condition. The overload timer is also an integrating timer, it will continue ramping up while the Current Limit Comparator is terminating drive pulses but will begin ramping down, not reset completely, if the drive pulse is terminated by another signal such as the PWM comparator. This operation is depicted in Figure 11.

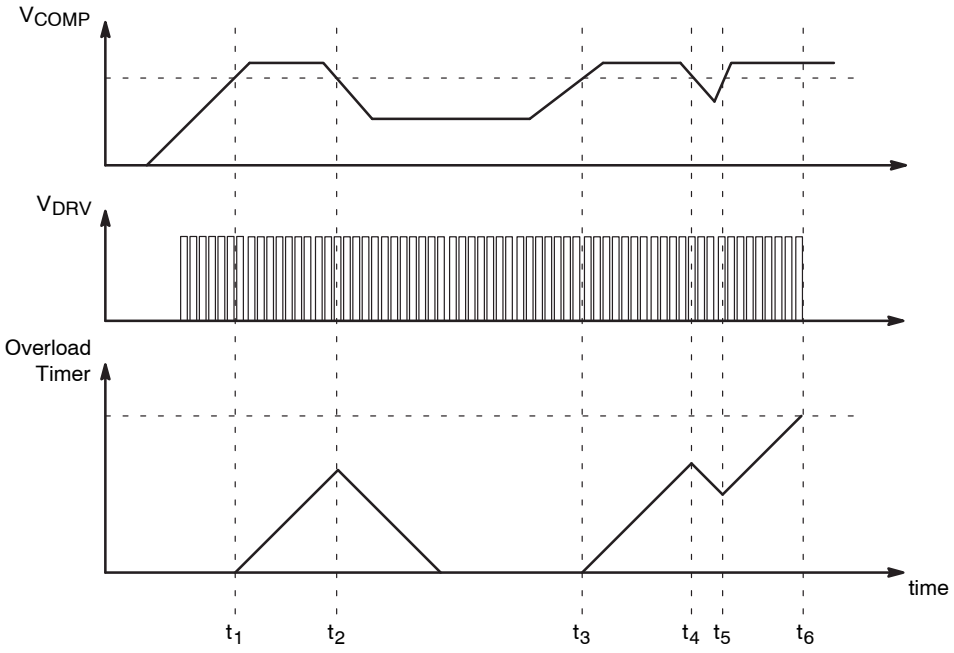



**Figure 11. Integrating Overload Timer**

### Short Circuit (SCP) Comparator

The NCP12700 also includes a fast Short Circuit Comparator with a threshold, $V_{SCP(LIM)}$, of 312.5 mV and 625 mV. In certain extreme fault conditions such as a shorted secondary side rectifier or a shorted winding in the transformer it may be possible to sense an abnormally high current pulse at the CS pin and disable drive pulses to


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prevent the converter from further damage. If the voltage at the CS pin rapidly exceeds $V_{SCP(LIM)}$ and the SCP comparator trips, then the drive pulse will be terminated and a counter will be incremented. If the SCP comparator trips on 4 consecutive drive pulses then drive pulses will be disabled and the controller is put into the Fault mode.

### Leading Edge Blanking (LEB)

Converters operating in peak current mode control require a high quality current ramp signal to ensure stable and clean PWM operation. In the NCP12700 the current ramp signal is sensed at the CS pin and is routed through a LEB circuit which blanks the current sense information for a brief period after the DRV voltage is delivered to the primary MOSFET. The LEB prevents noise generated during the switching transition from terminating drive pulses prematurely. The blanking is performed by an internal pulldown switch and series disconnect switch. The internal pulldown switch has an on resistance, $R_{PD(LEB)}$, specified as 55 ohms maximum. The pulldown switch is turned on whenever the DRV is low and remains on for a period of time equal to $t_{LEB(SCP)}$, 60 ns typical, after the DRV is set high.

After $t_{LEB(SCP)}$ has expired the current ramp signal is delivered to the SCP comparator allowing it to sense an abnormal overcurrent situation. A longer series LEB, $t_{LEB(CS)}$, of 100 ns continues to hold open the signal path to the CS and PWM comparators. This switch closes when $t_{LEB(CS)}$ has expired, allowing the CS information to be delivered to the other two comparators. In addition to the LEB network, the user of the controller will usually place a small RC filter in between the current sense components and the CS pin to provide noise suppression. The resistor value in the RC filter is typically in the range of 500 – 1 kΩ, sized appropriately for the Over−Power protection feature, and the capacitor value is typically chosen to provide a time constant for the RC filter of about 50 – 100 ns.

### Skip Comparator

For a power converter operating at light loads it is sometimes desired to skip drive pulses in order to maintain output voltage regulation or improve the light load efficiency of the system. The NCP12700 features a dedicated Skip Comparator which monitors the voltage at the COMP pin and blanks drive pulses if the COMP voltage falls below the $V_{COMP(skip)}$ threshold of 300 mV. To re−enable new drive pulses, the COMP voltage must exceed a skip hysteresis, $V_{COMP(skip_hys)}$ of 25 mV above the 300 mV threshold. The skip hysteresis is designed to prevent the converter from oscillating in and out of skip mode due to noise on the COMP pin.

### Maximum Duty Cycle

The NCP12700 also includes a maximum duty cycle clamp which terminates a drive pulse which has been high for $D_{MAX}$ of the switching period. The default value of $D_{MAX}$ will be 80%.

### Soft Start

The soft start feature in the NCP12700 is implemented with a dedicated comparator that compares the current ramp signal from the CS pin against an attenuated soft start ramp generated at the SS pin. Prior to enabling switching, an internal pull−down transistor with an on resistance, $R_{SS(DIS)}$, of 100 Ω is activated to discharge the external soft start capacitor and hold the SS pin to GND. Once switching is enabled the pull−down transistor is released and a current source, $I_{SS}$, of 15 μA charges the soft start capacitor forming the soft start ramp voltage. The soft start ramp voltage is then divided down by a factor of $K_{SS}$ and fed into the soft start comparator which resets drive pulses when the CS voltage exceeds the soft start voltage. The soft start comparator will continue to reset drive pulses until another comparator enters the reset path which typically occurs when the secondary side control loop responds allowing the PWM comparator to take control.

The NCP12700 monitors the external soft start voltage and sets a flag when the voltage exceeds 3 V, declaring that the soft start period has ended. At 3 V, the drive pulse reset control will have been handed off to either the PWM comparator or the Current limit comparator. The SS_END flag is used internally by the controller for fault management, gating detection of certain faults that may be erroneously triggered during power up of the converter. This is shown in the FLT pin block diagram of Figure 12.

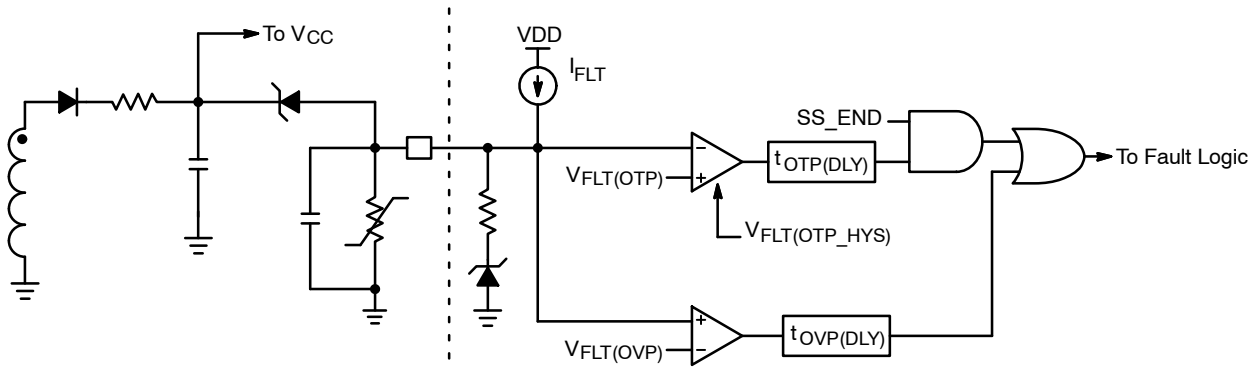



**Figure 12. FLT Pin Block Diagram**



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### Fault (FLT) Pin

The FLT pin is intended to provide the system with a NTC interface for thermal protection and a pull−up fault which can be coupled to the auxiliary winding to provide output over−voltage protection. The FLT pin can also be used as a general purpose fault where it interfaces with a simple pull−down BJT, open collector comparator, or optocoupler for monitoring of secondary side faults. The internal circuitry includes a precision pull−up current source, $I_{FLT}$, of 85 μA and a window comparator to signal a fault whenever the pin voltage goes below the OTP fault threshold, $V_{FLT(OTP)}$, of 0.5 V or above the OVP fault threshold, $V_{FLT(OVP)}$, of 3 V. Both of the fault comparators also include a delay filter to prevent noise or glitches from setting the fault. The over−temperature fault filter, $t_{OTP(DLY)}$, is nominally 20 μs and the over−voltage fault filter, $t_{OVP(DLY)}$, is typically 5 μs. An external filter capacitor is also advisable.

Both faults have an option to permanently latch off the controller or restart after a 1 s auto−recovery period. The OVP fault is intended to monitor an auxiliary winding and when triggered, the controller will disable switching which will inhibit the aux winding from generating voltage and allow the controller to restart after the auto−recovery timer has expired. If the OVP fault comparator is continuously held above 3 V, the NCP12700 will remain in the fault mode and not restart.

The OTP fault detection is gated by the SS_END flag to prevent the comparator from triggering while the external filter capacitor charges up. Once the SS_END flag is set the OTP fault can be acknowledged so there is a practical limit on the size of the filter capacitor. Equation 6 and Equation 7 should assist the user with properly setting the external capacitance of the fault pin.

$$t_{SS_END} = \frac{C_{SS} \times V_{SS_END}}{I_{SS}} \quad \text{(eq. 6)}$$

$$C_{FLT} < \frac{I_{FLT} \times t_{SS_END}}{V_{FLT(OTP)}} \quad \text{(eq. 7)}$$

When the OTP fault is triggered the NCP12700 will again disable drive pulses and transition into a fault mode. The OTP fault is auto−recoverable based on the auto−recovery timer and a hysteresis set by the $V_{FLT(REC)}$ threshold of 0.9 V. The auto−recovery timer must expire and the voltage at the fault pin must exceed 0.9 V. This methodology guarantees a minimum amount of time for the system to recover from thermal overstress but will not allow the converter to restart unless the hysteresis is met. Given the $I_{FLT}$ and $V_{FLT(OTP)}$ specifications the critical NTC resistance for declaring a fault is ~ 5.9 kΩ. The critical resistance for recovering from the OTP fault becomes ~ 10.6 kΩ. This fault recovery threshold provides for about ~20°C of hysteresis for many NTC resistors.

### Summary of Fault Handling

The NCP12700 has 6 fault detectors which will place the device into the fault mode. In the fault mode switching is inhibited and the controller bias is maintained by the HV startup regulator. The controller also reduces current consumption to $I_{CC(FLT)}$, 500 μA maximum, so that the regulator is not thermally overstressed. The NCP12700 remains in the fault mode until the fault signal has been cleared and/or the auto−recovery timer has expired. The fault signal can be cleared when the fault detector senses that the fault has been removed or by a controller reset which occurs if $V_{CC}$ drops below $V_{CC(OFF)}$ or the UVLO pin is pulled below the $V_{RST(th)}$ level. Below is a brief summary of the different fault detectors and their basic operation.

- Thermal Shutdown (TSD): Thermal shutdown is declared when the internal junction temperature of the device exceeds the $T_{SHDN}$ temperature of 165°C. The thermal shutdown fault is auto−recoverable when the device junction temperature reduces to $T_{SHDN}$ − $T_{SHDN(hys)}$ where $T_{SHDN(hys)}$ is typically 25°C.
- Fault OTP: An OTP fault is declared when fault pin voltage decreases below the $V_{FLT(OTP)}$ threshold of 0.5 V and the OTP filter, $t_{OTP(DLY)}$, expires. The OTP filter delay is typically 20 μs. The OTP fault is blanked at startup until the SS_END flag has been set to allow the external capacitance of the pin to charge up. For the device to recover from the Fault OTP, the auto−recovery timer must expire and the voltage at the fault pin must recover to $V_{FLT(REC)}$ value of 0.9 V.
- Fault OVP: The OVP fault is declared when fault pin the voltage exceeds the $V_{FLT(OVP)}$ threshold of 3 V and the OVP filter, $t_{OVP(DLY)}$, expiring. The OVP filter delay is typically 5 μs. The OVP fault is cleared when the auto−recovery timer expires. There is no hysteresis on the OVP fault but if the pin voltage is permanently held above 3 V, DRV will pulses will be permanently inhibited.
- Overload (OVLD): The OVLD fault is set when the overload timer, $t_{OVLD}$, expires. The overload timer is an integrating timer which counts up as long as the Current Limit comparator is terminating DRV pulses. The typical value for $t_{OVLD}$ is 30 ms. The controller will recover from the OVLD fault when the auto−recovery timer expires.
- SCP Fault: The SCP fault occurs when the $N_{SCP}$ counter has reaches 4 consecutive DRV pulses terminated by the SCP comparator. The controller will recover from the SCP fault when the auto−recovery timer expires.
- $V_{CC}$ OVP: The $V_{CC}$ OVP is set when $V_{CC}$ voltage exceeds the $V_{CC(OVP)}$ threshold of 28 V and the $V_{CC}$ OVP filter, $t_{VCC_OVP(DLY)}$, expires. The $V_{CC}$ OVP filter is typically 3 μs. $V_{CC}$ OVP will permanently latch the device off so that it remains in the Fault mode indefinitely until the controller is reset.


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## EVALUATION BOARD DESIGNS

Two evaluation boards have been developed to highlight the features of the NCP12700. Detailed schematics, operating waveforms, and bill of materials are available in the design notes, DN05108 and DN05109. DN05108 describes the operation of a 9 – 36 V input flyback converter delivering 12 V out at 15 W. This evaluation board switches at 200 kHz and operates in both continuous and discontinuous conduction modes. The key performance specifications are shown in Table 5 below.

**Table 5. LOW VOLTAGE FLYBACK EVALUATION BOARD SPECIFICATIONS**

| | **Evaluation Board # 1** |
|---|---|
| **Vin** | 9 – 36 V Operating |
| **Vo** | 12 V – 1.25 A |
| **Po** | 15 W |
| | **Specifications** |
| **Startup time** | < 30 ms |
| **Full Load Efficiency** | > 87 % |
| **Transient Response** | < 250 μs |
| **Over Power Protection** | 120% – 150% |
| **Over Voltage Protection** | 16 VDC Max |
| **No Load Output Ripple** | 200 mVpp Max |
| **No Load Power Dissipation** | 120 mW Max |
| **Input Current in SHDN** | < 1 mA |

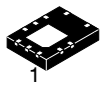
DN05109 describes the operation of a 18 – 160 V input flyback converter delivering 12 V out at 15 W. This demonstration board switches at 100 kHz and operates in discontinuous conduction mode across the entire input voltage range. The key performance specifications are shown in Table 6.

**Table 6. WIDE RANGE FLYBACK EVALUATION BOARD SPECIFICATIONS**

| | **Evaluation Board # 2** |
|---|---|
| **Vin** | 18 – 160 V Operating |
| **Vo** | 12 V – 1.25 A |
| **Po** | 15 W |
| | **Specifications** |
| **Startup time** | < 20 ms |
| **Full Load Efficiency** | > 85 % |
| **Transient Response** | < 250 μs |
| **Over Power Protection** | 115% – 155% |
| **Over Voltage Protection** | 16 VDC Max |
| **No Load Output Ripple** | 150 mVpp Max |
| **No Load Power Dissipation** | 500 mW Max |
| **Input Current in SHDN** | < 1 mA |



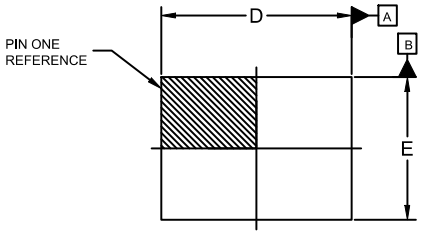
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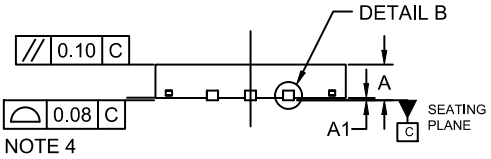
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ISSUE C

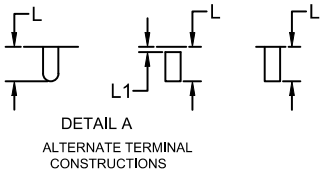
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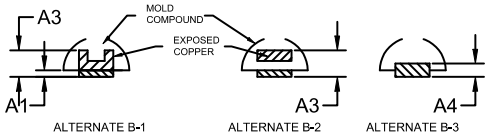


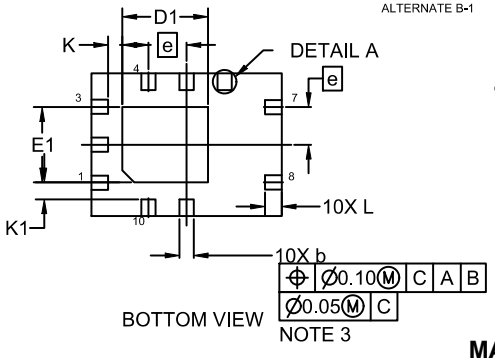

TOP VIEW




SIDE VIEW




BOTTOM VIEW

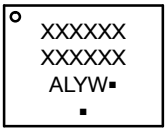
DETAIL B
ALTERNATE
CONSTRUCTION

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 0.20 AND 0.25 FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE PLATED TERMINALS.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | --- | 0.05 |
| A3 | | 0.20 REF | |
| A4 | | 0.10 REF | |
| b | 0.25 | 0.30 | 0.35 |
| D | 3.90 | 4.00 | 4.10 |
| D1 | 1.75 | 1.80 | 1.85 |
| E | 2.90 | 3.00 | 3.10 |
| E1 | 1.53 | 1.58 | 1.63 |
| e | | 0.80 BSC | |
| K | | 0.30 REF | |
| K1 | | 0.36 REF | |
| L | 0.30 | 0.35 | 0.40 |
| L1 | | 0.05 REF | |

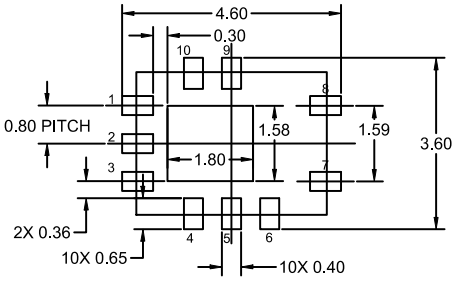
**GENERIC MARKING DIAGRAM***




XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.




RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

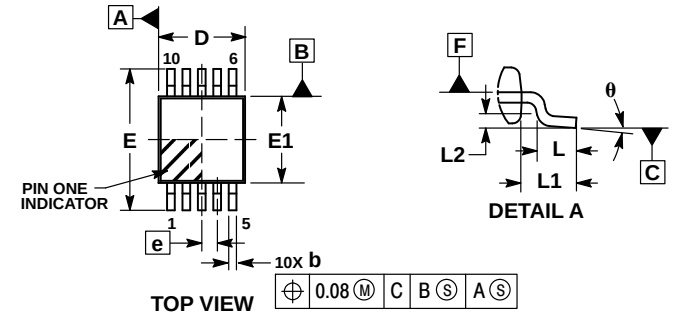
| | | |
|---|---|---|
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| **DESCRIPTION:** | **WQFN10 4x3, 0.8P** | **PAGE 1 OF 1** |

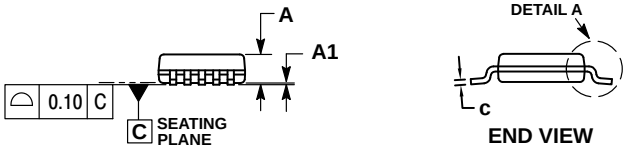
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**SCALE 1:1**

**MSOP10, 3x3**
CASE 846AE
ISSUE A

DATE 20 JUN 2017

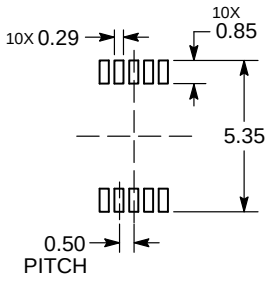



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 MM IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. DIMENSION E DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 MM PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | --- | --- | 1.10 |
| A1 | 0.00 | 0.05 | 0.15 |
| A2 | 0.75 | 0.85 | 0.95 |
| b | 0.17 | --- | 0.27 |
| c | 0.13 | --- | 0.23 |
| D | 2.90 | 3.00 | 3.10 |
| E | 4.75 | 4.90 | 5.05 |
| E1 | 2.90 | 3.00 | 3.10 |
| e | 0.50 BSC | | |
| L | 0.40 | 0.70 | 0.80 |
| L1 | 0.95 REF | | |
| L2 | 0.25 BSC | | |
| θ | 0° | --- | 8° |

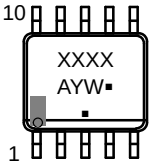
## RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present and may be in either location. Some products may not follow the Generic Marking.

| | | | |
|---|---|---|---|
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| **DESCRIPTION:** | **MSOP10, 3X3** | | **PAGE 1 OF 1** |

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