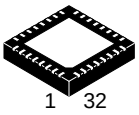
2.5 V / 3.3 V Low Noise Multi-Rate Clock Generator

NB3H5150



QFN32
MN SUFFIX
CASE 485CE

MARKING DIAGRAM*



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information on page 18 of this data sheet.

Description

The NB3H5150 is a high performance Multi−Rate Clock generator which simultaneously synthesizes up to four different frequencies from a single PLL using a 25 MHz input reference. The reference frequency can be provided by a crystal, LVCMOS/LVTTL, LVPECL, HCSL or LVDS differential signals. The REFMODE pin will select the reference source.

Three output banks (CLK1A/CLK1B to CLK3A/CLK3B) produce user selectable frequencies of: 25 MHz, 33.33 MHz, 50 MHz, 100 MHz, 125 MHz, or 156.25 MHz and have ultra−low noise/jitter performance of less than 0.3 ps.

The fourth output bank (CLK4A/CLK4B) can produce the following integer and FRAC−N frequencies in pin−strap mode: 33.33 MHz, 66.66 MHz, 100 MHz, 106.25 MHz, 125 MHz, 133.33 MHz, 155.52 MHz, 156.25 MHz or 161.1328 MHz.

Each output block can create two single−ended in−phase LVCMOS outputs or one differential pair of LVPECL outputs.

Each of the four output blocks is independently powered by a separate VDDO, 2.5 V/3.3 V for LVPECL, 1.8 V/2.5 V/3.3 V for LVCMOS.

The serial (I^2C and SMBUS) interface can be used to load register files into the NB3H5150 to program a variety of functions including the frequencies and output levels of each output which can be individually enabled and disabled.

Features

- Flexible Input Reference − 25 MHz Crystal, Oscillator, Single−Ended or Differential Clock
- Four Independent User−Programmable Clock Frequencies from 25 MHz to 250 MHz
- Independently Configurable Outputs:
  Up to Eight LVCMOS Single Ended outputs or,
  Up to Four Differential LVPECL Outputs or any combination of LVCMOS and LVPECL
- Flexible Input/Core and Output Power Supply Combinations:
  VDD (Core) = 3.3 V ±5% or 2.5 V ±5%
  $VDDO_n$ (Outputs) = 3.3 V ±5% or 2.5 V ±5% or 1.8 V ±5% (LVCMOS Only)
- Independent Power Supply for each Output Bank
- 300 ps max Output Rise and Fall Times, LVPECL
- 1000 ps max Output Rise and Fall Times, LVCMOS
- 300 fs maximum RMS Phase Jitter Interger−N (CLK1:4) 156.25 MHz
- 1 ps maximum RMS Phase Jitter FRAC−N (CLK4) 155.52 MHz
- I^2C / SMBus Compatible Interface
- −40°C to +85°C Ambient Operating Temperature
- Zero ppm Multiplication Error
- Fractional Divide Ratios for Implementing Arbitrary FEC/Inverse−FEC Ratios
- For Additional Pin−strap Frequency and Output Type Combinations, Contact **onsemi** Sales Office
- 32−Pin QFN, 5 mm x 5 mm
- This is a Pb−Free Device

Applications

- Telecom
- Networking
- Ethernet
- SONET

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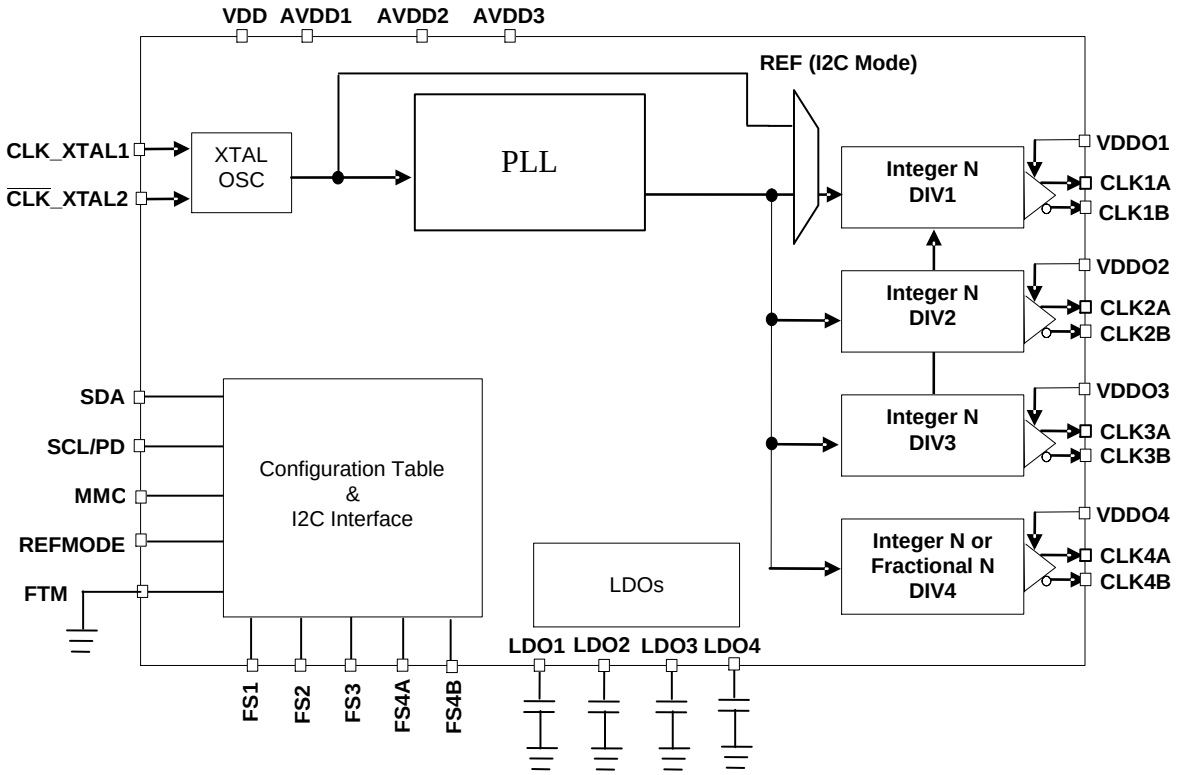


Figure 1. Simplified Block Diagram of NB3H5150

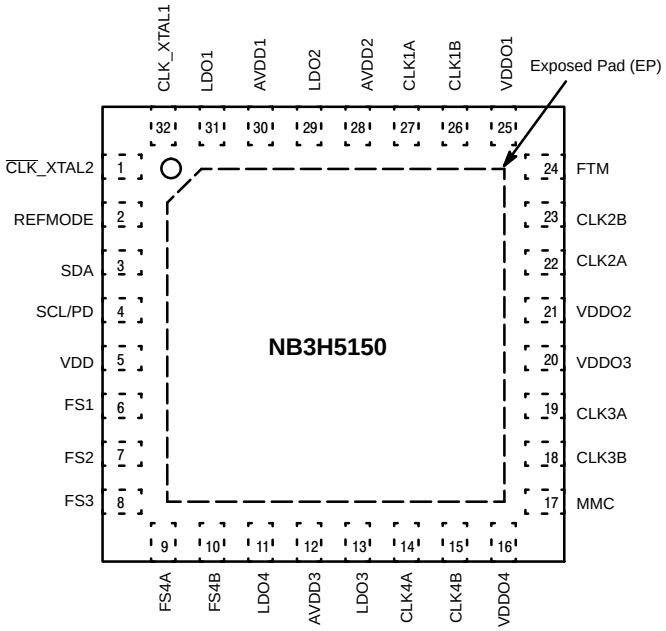


Figure 2. 32−Lead QFN Pinout (Top View)

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Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	$\overline{\text{CLK}}$_XTAL2	Crystal or LVPECL/LVDS Input	Crystal Output or Differential Clock Input (complementary); If CLK_XTAL1 is used as single−ended input, $\overline{\text{CLK}}$_XTAL2 must be connected to ground. See Table 2.
2	REFMODE	LVTTL/LVCMOS Input	Reference Input Select to either use a crystal, or overdrive with a single−ended or differential input; see Table 2. Internal pull−down.
3	SDA	LVTTL/LVCMOS Input	Serial Data Input for I2C/SMBus compatible; Defaults High when left open; internal pull−up. 5V tolerant.
4	SCL/PD	LVTTL/LVCMOS Input	Serial Clock Input for I2C/SMBus compatible; Defaults High when left open; internal pull−up. SCL/PD is also a device power−down pin (when High) in pin−strap mode only. 5V tolerant.
5	VDD	Power	3.3 V / 2.5 V Positive Supply Voltage for the Inputs and Core
6	FS1	LVTTL/LVCMOS Input	Frequency Select 1 for DIV1, CLK1A & CLK1B; Three–level input buffer; Default is mid−logic level; internal RPull−up and RPull−down. See Table 3.
7	FS2	LVTTL/LVCMOS Input	Frequency Select 2 for DIV2, CLK2A & CLK2B; Three–level input buffer; Default is mid−logic level; internal RPull−up and RPull−down. See Table 3.
8	FS3	LVTTL/LVCMOS Input	Frequency Select 3 for DIV3, CLK3A, & CLK3B; Three–level input buffer; Default is mid−logic level; internal RPull−up and RPull−down. See Table 3.
9	FS4A	LVTTL/LVCMOS Input	Frequency Select 4A for DIV4, CLK4A & CLK4B; Three–level input buffer; Default is mid−logic level; internal RPull−up and RPull−down. See Table 4.
10	FS4B	LVTTL/LVCMOS Input	Frequency Select 4B for DIV4, CLK4A & CLK4B; Three–level input buffer; Default is mid−logic level; internal RPull−up and RPull−down. See Table 4.
11	LDO4	Power	1.8 V LDO − Install Power Conditioning Bypass Capacitor to Ground
12	AVDD3	Power	3.3 V / 2.5 V Positive Supply Voltage for Analog circuits. AVDD3 = VDD.
13	LDO3	Power	1.8V LDO − Install Power Conditioning Bypass Capacitor to Ground
14	CLK4A	Output	LVCMOS (single−ended) or Non− Inverted Differential LVPECL Clock A for Channel 4 Output
15	CLK4B	Output	LVCMOS (single−ended) or Inverted Differential LVPECL Clock B for Channel 4 Output
16	VDDO4	Power	3.3 V / 2.5 V / 1.8 V Positive Supply Voltage for the CLK4A/4B Outputs
17	MMC	LVTTL/LVCMOS Input	Mix Mode Control Pin for use as a combination of FSn settings and I2C setting for the CLK(n) outputs in the I2C mode; see Table 5. No logic level default; use a RPull−up resistor for High or a RPull−down resistor for Low.
18	CLK3B	Output	LVCMOS (single−ended) or Inverted Differential LVPECL Clock B for Channel 3 Output
19	CLK3A	Output	LVCMOS (single−ended) or Non−Inverted Differential LVPECL Clock A for Channel 3 Output
20	VDDO3	Power	3.3 V / 2.5 V / 1.8 V Positive Supply Voltage for the CLK3A/3B Outputs
21	VDDO2	Power	3.3 V / 2.5 V / 1.8 V Positive Supply Voltage for the CLK2A/2B Outputs
22	CLK2A	Output	LVCMOS (single−ended) or Non− Inverted Differential LVPECL Clock A for Channel 2 Output
23	CLK2B	Output	LVCMOS (single−ended) or Inverted Differential LVPECL Clock B for Channel 2 Output
24	FTM		Factory Test Mode. Must connect this pin to Ground.
25	VDDO1	Power	3.3 V / 2.5 V / 1.8 V Positive Supply Voltage for the CLK1A/1B Outputs
26	CLK1B	Output	LVCMOS (single−ended) or Inverted Differential LVPECL Clock B for Channel 1 Output
27	CLK1A	Output	LVCMOS (single−ended) or Non−Inverted Differential LVPECL Clock A for Channel 1 Output
28	AVDD2	Power	3.3 V / 2.5 V Positive Supply Voltage for Analog circuits. AVDD2 = VDD.
29	LDO2	Power	1.8 V LDO − Install Power Conditioning Bypass Capacitor to Ground
30	AVDD1	Power	3.3 V / 2.5 V Positive Supply Voltage for Analog circuits. AVDD1 = VDD.
31	LDO1	Power	1.8 V LDO − Install Power Conditioning Bypass Capacitor to Ground

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Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
32	CLK_XTAL1	Crystal or LVTTL/LVCMOS or LVPECL/LVDS Input	Crystal Input or Single−Ended or Differential Clock Input; If CLK_XTAL1 is used as single−ended input, $\overline{\text{CLK}}$_XTAL2 must be connected to ground. See Table 2.
EP	Exposed Pad	Ground	Ground – Negative Power Supply is connected via the Exposed Pad . The Exposed Pad (EP) on the QFN−32 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat sinking conduit. The pad is electrically connected to the die,carries all power supply return currents and must be electrically connected to GND.

1. All VDD, AVDDn, VDDOn, EP (GND) pins must be externally connected to a power supply for proper operation. VDD and AVDDn must all be at the same voltage.

NB3H5150 BASIC OPERATION

Introduction

The NB3H5150 is a Multi−Rate Clock Generator. The clock reference for the PLL can be either a 25 MHz crystal, single−ended LVCMOS or LVTTL signal or a differential LVPECL, LVDS or HCSL signal.

There are two modes of operation for the NB3H5150, Pin−Strap and I^2C.

In the **Pin−Strap Mode**, the user can select any of the defined output frequencies for each of the four output banks as specified in Tables 3 and 4 via the three−level Frequency Select pins: FS1, FS2, FS3, FS4A and FS4B.

In the **I^2C mode**, the user can select one of the approved register files. Each register file is an expanded selection of output frequencies and level combinations, output enable/disable and bypass mode functions.

CLKnA & CLKnB − Output Frequency and Output Level Selection

There are four output banks: CLK1A&B, CLK2A&B and CLK3A&B are integer only divider outputs, whereas CLK4A&B can be set or programmed as an integer or fractional divider.

The output levels for each output bank can be LVPECL (differential) or LVCMOS (two single−ended). Output Enable / Disable functions are available in I^2C only.

CLK1, 2, 3 and 4 outputs are not phase−aligned, in PLL or PLL bypass modes.

Power−On Output Default

Upon power−up, all four outputs will be forced to and held at static LVPECL levels (CLKnA = Low, CLKnB = High) until the PLL is stable. The PLL will be stable before any of the output Clocks, CLKnx, are enabled.

SDA & SCL/PD − Serial Data Interface – I2C

The NB3H5150 incorporates a two−wire Serial Data Interface to expand the flexibility and function of the NB3H5150 clock generator.

The I^2C interface pins, SCL and SDA, are used to load register files into the NB3H5150.

These register files will configure the internal registers to achieve an expanded selection of output frequencies and levels combinations for each of the four output blocks.

Subsequent changes in the registers can then be performed with another register file to modify any of the output frequencies or output modes.

OE, Output Enable

An OE, Output Enable/Disable function is available only in the I^2C mode by loading a register file, such that any individual output bank can be enabled or disabled. In LVCMOS modes outputs will disable LOW for CLKnA and CLKnB, while the LVPECL mode outputs will disable CLKnA = Low and CLKnB = High.

Mixed Mode Control (MMC)

In the I^2C mode, the Mixed Mode Control (MMC) pin is used for a combination of FSn settings and I2C settings to control the CLK(n) outputs' function as defined in Table 5.

REFMODE – Select a Crystal or External Clock Input Interface (See Table 2)

The REFMODE pin will select the reference input for the CLK_XTAL1 and $\overline{\text{CLK}}$_XTAL2 pins to use either a crystal, an overdriven single−ended or differential input.

When using a crystal, set the REFMODE pin to a LOW. The CLK_XTAL1 and $\overline{\text{CLK}}$_XTAL2 input pins will accept a 25 MHz crystal.

When using a direct−coupled differential input, set the REFMODE pin to a HIGH.

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When REFMODE is HIGH, the CLK_XTAL1 and $\overline{\text{CLK}}$_XTAL2 differential input pins have internal AC coupling capacitors selected with self−bias circuity for the differential input buffer. This differential buffer will directly accept any differential signal including LVPECL, LVDS, HCSL or CML. Drive the CLK_XTAL1 pin with the true signal and the $\overline{\text{CLK}}$_XTAL2 pin with the complementary signal.

When overdriving the CLK_XTAL1 input pin with a single−ended signal set REFMODE to a HIGH, and connect $\overline{\text{CLK}}$_XTAL2 to Ground. The input has internal AC coupling capacitor with self−bias circuitry.

Table 2. CRYSTAL INPUT INTERFACE AND REFMODE TRUTH TABLE

Input Mode Crystal/External Clock	REFMODE	CLK_XTAL1	CLKb_XTAL2
Crystal	LOW	Use a Crystal	Use a Crystal
Any Differential Input	HIGH	Overdrive with True Input	Overdrive with Complementary Input
Single−Ended Input	HIGH	Overdrive	Connect to Ground

LVCMOS Outputs

LVCMOS outputs are powered with VDDOn = 3.3 V, 2.5 V or 1.8 V

A 33 Ω series terminating resistor may be used on each clock output if the metal trace is longer than one inch.

Any unused LVCMOS output can be left floating, but there should be no metal trace attached to the package pin.

LVPECL Differential Outputs

The differential LVPECL outputs are powered with VDDO = 3.3 V or 2.5 V and must be properly loaded. See Figure 10.

Any unused differential output pair should either be left floating or terminated.

REF Out

In the PLL bypass mode available via I^2C, the input reference frequency can be routed to CLK1A and CLK1B as phase aligned LVCMOS or differential LVPECL outputs with the same frequency. The output frequency and duty cycle equals the input frequency and duty cycle.

Power Supplies

The NB3H5150 has several power supply pins:

- VDD is the supply voltage for the input and digital core circuitry.
- AVDD1, AVDD2 and AVDD3 powers the core analog circuits. VDD = AVDD1 = AVDD2 = AVDD3.
- VDDO1, VDDO2, VDDO3 and VDDO4 are individual power supplies for each of the four CLKnA/B output banks.

Upon power−up, all four VDDOn pins must be connected to a power supply, even if only one output is being used.

Any combination of VDD and VDDOn power supply voltages is allowed.

A power supply filtering scheme in Figure 8 is recommended for best device performance.

When all VDD, AVDDn and VDDOn pins reach their minimum voltage per Table 8, the NB3H5150 will operate at the proper output frequencies.

EP Exposed Pad

The exposed pad on the bottom side of the package must be connected to Ground.

LDO Pins

The NB3H5150 has integrated low noise 1.8 V Low−Drop−Out (LDO) voltage regulators which provide power internal to the NB3H5150.

The LDOs require decoupling capacitors in the range of 1 μF to 10 μF for compensation and high frequency PSR.

When powered−down, the device turns off the LDOs and enters a low power shutdown mode consuming less than 1 mA.

FTM

This is a Factory Test Mode pin and must be connected to the Ground of the application for proper operation.

PIN−STRAP / FSn Frequency Select MODE: (see Tables 3 and 4)

The NB3H5150 can be configured to operate in pin−strap mode where the control pins FSnA/B can be set to generate the necessary clock outputs of the device.

Prerequisites:

- SDA and SCL/PD must be Low at all times while in pin−strap mode to enable FS control. If SDA ever goes High, pin−strap is exited and the only way to go back is to power cycle the device.
- Mixed Mode Control pin (MMC) level will be IGNORED.

Sequencing:

1. Upon device power−up (assuming SCL is LOW)
   A All four CLK(n) frequency and output type selections will be pre−loaded according to the FS pin settings, but all four outputs will be held at static LVPECL levels (CLKnA = Low, CLKnB = High) until the PLL has become stable.
   B After the PLL is stable, all CLK(n) output type selections (i.e. LVPECL or LVCMOS) will

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become effective and will begin to output the selected frequencies.

2. Subsequent changes to any FS pin(s) will cause the associated CLK(n) output(s) to momentarily go to static levels, and then to resume at the new frequency; CLK(n) will follow the FS(n) pin programmable Tables 3 and 4 for output frequencies and interface levels.
   Note that in changing from LVPECL to LVCMOS (or vice−versa), output logic levels cannot be guaranteed. This is because the receiver inputs are not likely to change in a given application, and the LVPECL output loading in the application will also not change. It is logical to presume that the output type will be predetermined and fixed. Therefore, in a system/application, the user should be aware that subsequent change to the FS pin should only change frequency, and not output type.
3. Power off/on cycle will repeat the entire sequence
4. **Power Down**
   To initiate the Power−Down mode, the SDA pin must be LOW and remain LOW. If the SCL/PD pin is taken HIGH at any time, the device enters a complete power−down mode with a current consumption of less than 1 mA for the entire device. When SCL/PD is subsequently taken LOW, the device will function as though power were removed and re−applied. That is, sequencing will begin at #1.
   Power−down is also available via I^2C with a register file.

FS(n) Pin Programmable Selection of Output Frequencies and Levels

Table 3. NB3H5150 − CLK1A:3A & CLK1B:3B OUTPUT FREQUENCY SELECT TABLE WITH 25 MHz CRYSTAL

Logic Level	FS1 (CLK1) (MHz)	FS2 (CLK2) (MHz)	FS3 (CLK3) (MHz)
Low	50.00 (LVCMOS)	156.25 (LVPECL)	156.25 (LVPECL)
Mid / Float*	33.33 (LVCMOS)	25.00 (LVPECL)	125.00 (LVCMOS)
High	25.00 (LVCMOS)	125.00 (LVPECL)	100.00 (LVPECL)

*(Default)

Table 4. NB3H5150 − CLK4A & CLK4B OUTPUT FREQUENCY SELECT TRUTH TABLE (MHz) WITH 25 MHz CRYSTAL*

FS4A	FS4B	CLK4 (MHz)	Divider Type
Low	Low	33.33 (LVCMOS)	Integer
Low	Mid / Float	66.66 (LVCMOS)	Fractional
Low	High	133.33 (LVCMOS)	Fractional
Mid / Float	Low	155.52 (LVPECL)	Fractional
Mid / Float*	Mid / Float*	156.25 (LVPECL)	Integer
Mid / Float	High	125.00 (LVPECL)	Integer
High	Low	106.25 (LVPECL)	Fractional
High	Mid / Float	100.00 (LVCMOS)	Integer
High	High	161.1328 (LVPECL)	Fractional

*(Default)

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I²C MODE: (see Table 5)

Some features that are not available in pin−strap mode can be obtained in I2C mode, such as Output Enable/Disable, By−Pass mode and Power−Down. In addition, output frequency and output levels can also be I2C controlled.

The NB3H5150 I2C Programming Guide can be found on the NB3H5150 web site. This application note provides details on configuring the NB3H5150 by writing to registers in the NB3H5150 with approved register files through the I2C/SMBus interface.
http://www.onsemi.com/pub/Collateral/NB3H5150%20I2C%20PROGRAMMING%20GUIDE%20%20..PDF

Register Files can be generated by the factory upon request.

Prerequisites:

- SDA and SCL must be connected to I²C SMBus
- SDA must be logic High.

1. Upon device power−up.
   A All four frequencies and output type selections will be preloaded according to the FSn pin settings, but all four outputs will be held at static LVPECL levels until the PLL has become stable.
   NOTE: After power up, changes to FS pins will be blocked from controlling device operation.
   B Once the PLL is stable, the Mixed Mode Control pin (MMC) is checked:
   i. If MMC is LOW, all CLK(n) outputs will remain at static LVPECL levels.
   ii. If MMC is HIGH and FS4A is LOW, CLK1, CLK2, and CLK3 outputs will remain at static LVPECL levels.
   CLK4A/4B output frequency and output levels will become active after PLL stabilization time according to FS4A and FS4B pin selection in Table 4.
   After power up, changes to all pins will be ignored.
   iii. If MMC is HIGH and FS4A MID or HIGH, CLK1, CLK2, and CLK3 output frequency and type will become active after PLL stabilization time according to their respective FS1, FS2 and FS3 pin selection in Table 3.
   CLK4A/4B outputs remain at Static LVPECL Levels.
   After power up, changes to all pins will be ignored except the SDA and SCL inputs.
   iv. The FS4A and FS4B pins set the bus address when MMC pin is LOW (see Table 5, I2C Device Address Table).
   C The I²C interface can now be used to load register files into the NB3H5150. In I²C Mode, configuration of Output Enables, output frequency, output levels of each output, specific block power−down control, bypass mode, etc. are all possible.
   D Any outputs which were held in static level mode (described above) will be released for operation.

CLK(n) outputs will be active at the programmed frequencies and levels.

CLK(n) outputs will react to any subsequent changes to the I²C bus.

If any output channel is not programmed, then output is loaded from FSn pins.

A Power Cycle will clear all previous register information and I²C mode will repeat to number 1 in the power up sequence.

To simplify device configuration, **onsemi** provides desktop software, that can be downloaded from http://www.onsemi.com/pub/Collateral/NB3H5150_GUI.ZIP which will operate in conjunction with the NB3H5150 evaluation board (EVB). The NB3H5150 GUI manual can also be found on the web site.

When the software is connected to an NB3H5150 EVB, it can control the selection of numerous clock output frequencies for each of the four CLK outputs and the output type as well as Output Enable/Disable.

I²C Programmable Selection of Output Frequency and Level

Each register file can be loaded from GUI into the demo board, or loaded into the I²C port of the device.

Table 5. SDA, SCL AND MMC CONTROL PINS FOR OUTPUT FUNCTION

Mode	SDA	SCL/PD	MMC	Comments	Outputs (Note 2)	
					CLK1, CLK2, CLK3	CLK4
Pin−Strap FS Mode	L	L	X	Normal Operation	Toggle per Table 3	Toggle per Table 4
Power−Down	L	H	X		Off	Off
I²C (Note 3)	Dynamic	Dynamic	X	I2C Mode Is Active After Mixed Mode Power−Up Sequence	Active Per I2C Map	Active Per I²C Map

2. All outputs are static until after the PLL is stable.
3. Any changes to the device configuration after power−up are made by reading and writing to registers through the I2C interface.
4. Don't care state unless device address is matched by controller address.

X = don't care

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Table 5. SDA, SCL AND MMC CONTROL PINS FOR OUTPUT FUNCTION

Mode	SDA	SCL/PD	MMC	Comments	Outputs (Note 2)	
					CLK1, CLK2, CLK3	CLK4
Mixed Mode	H Note 4	H Note 4	L		Static LVPECL Logic Levels	Static LVPECL Logic Levels
	H Note 4	H Note 4	H FS4A = L		Static LVPECL Logic Levels	Active per Table 4
	H Note 4	H Note 4	H FS4A = M or H		Active per Table 3	Static LVPECL Logic Levels

2. All outputs are static until after the PLL is stable.
3. Any changes to the device configuration after power−up are made by reading and writing to registers through the I2C interface.
4. Don't care state unless device address is matched by controller address.

X = don't care

Table 6. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model Charge Device Model	> 2 kV > 150 V > 500 V
Moisture Sensitivity (Note 5) 32−QFN		Level 1
Flammability Rating Oxygen Index: 28 to 34		UL 94 V−0 @ 0.125 in
Transistor Count		245, 894
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

5. For additional information, see Application Note AND8003/D.

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Table 7. MAXIMUM RATINGS

Symbol	Parameter	Condition	Rating	Unit
V_{DD}	Positive Power Supply – Core	GND = 0 V	3.63	V
AV_{DDn}	Positive Power Supply – Analog	GND = 0 V	3.63	V
V_{DDOn}	Positive Power Supply – Outputs	GND = 0 V	3.63	V
V_{IO}	Positive Input/Output Voltage	GND = 0 V	−0.5 to V_{DD} +0.5	V
V_I	Positive Input Voltage SDA and SCL	GND = 0 V	5.5	V
T_A	Operating Temperature Range	QFN−32	−40 to +85	°C
T_{stg}	Storage Temperature Range		−65 to +150	°C
θ_J	Maximum Junction Temperature		125	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 6) QFN−32 QFN−32	0 lfpm 500 lfpm	31 27	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case) (Note 6) QFN−32		12	°C/W
T_J	Maximum Junction Temperature		125	°C
T_{sol}	Wave Solder Pb−Free, 10 sec		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
6. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

Table 8. DC CHARACTERISTICS

V_{DD} = AV_{DDn} = 3.3 V ±5% or 2.5 V ±5%; V_{DDOn} = 3.3 V ±5% or 2.5 V ±5% or 1.8 V ±5%; GND = 0 V; T_A = −40°C to 85°C

Symbol	Characteristic	Min	Typ	Max	Unit
POWER SUPPLY / CURRENT (Note 12)					
V_{DD}/AV_{DDn}	Core Power Supply V_{DD} = AV_{DDn} = 3.3 V	3.135	3.3	3.465	V
	V_{DD} = AV_{DDn} = 2.5 V	2.375	2.5	2.625	
V_{DDOn}	Output Power Supply V_{DDOn} = 3.3 V	3.135	3.3	3.465	
	V_{DDOn} = 2.5 V	2.375	2.5	2.625	
	V_{DDOn} = 1.8 V (LVCMOS only)	1.71	1.8	1.89	
I_{DD}/I_{ADDn}	Core and Input Power Supply Current for V_{DD} and A_{VDDn}				mA
	V_{DD} = 3.3 V CLK4 Integer		60	75	
	CLK4 Frac−N		75	90	
	V_{DD} = 2.5 V CLK4 Integer		55	70	
	CLK4 Frac−N		70	85	
I_{DDOn}	Output Buffer Power Supply Current for V_{DDOn}				mA
	Incremental I_{DDO} Current by One Output Bank and Output Type				
	LVPECL − One differential LVPECL output pair (CLKnA & CLKnB)				
	Frequency Independent V_{DDO} = 3.3 V		40	50	
	V_{DDO} = 2.5 V		40	50	
	LVCMOS − Two LVCMOS outputs (CLKnA & CLKnB)				
	V_{DDO} = 3.3 V		20	25	
	V_{DDO} = 2.5 V		17	23	
	V_{DDO} = 1.8 V		15	21	
$I_{DD}PWRDN$	Power Down Current SCL/PD = High		100		μA

LVPECL OUTPUTS (Note 7 and 8) V_{DDOn} = 3.3 V ±5% or 2.5 V ±5%; See Figure 10

V_{OH}	Output HIGH Voltage	V_{DDO} − 1.200		V_{DDO} − 0.895	V
V_{OL}	Output LOW Voltage	V_{DDO} − 2.000		V_{DDO} − 1.600	V
V_{SWING}	$V_{OUT\ PK-PK}$ Voltage Swing	550	720	900	mV

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Table 8. DC CHARACTERISTICS

V_{DD} = AV_{DDn} = 3.3 V ±5% or 2.5 V ±5%; V_{DDOn} = 3.3 V ±5% or 2.5 V ±5% or 1.8 V ±5%; GND = 0 V; T_A = −40°C to 85°C

Symbol	Characteristic		Min	Typ	Max	Unit
LVCMOS OUTPUT; See Figure 12						
V_{OH}	Output HIGH Voltage IOH = 12 mA		V_{DDO} – 0.5		V_{DDO}	V
V_{OL}	Output LOW Voltage IOL = 12 mA		GND		0.5	V
R_{OUT}	Output Impedance			15		Ω
CRYSTAL INPUT DRIVEN SINGLE−ENDED (REFMODE = 1) (see Figure 3 and 5) (Note 9)						
V_{IHSE}	CLK_XTAL1 Single−Ended Input HIGH Voltage		200		V_{DD}	mV
V_{ILSE}	CLK_XTAL1 Single−Ended Input LOW Voltage		GND		V_{IHSE} − 200	mV
V_{th}	Input Threshold Reference Voltage Range		100		V_{DD} − 100	mV
V_{ISE}	Single−Ended Input Voltage (V_{IH} – V_{IL})		200		V_{DD}	mV
CRYSTAL INPUTS DRIVEN DIFFERENTIALLY (REFMODE = 1) (see Figure 4 and 6) (Note 11)						
V_{IHD}	Differential Input HIGH Voltage		100		V_{DD}	mV
V_{ILD}	Differential Input LOW Voltage		GND		V_{IHD} – 100	mV
V_{ID}	Differential Input Voltage (V_{IHD} – V_{ILD})		100		V_{DD}	mV
V_{CMR}	Input Common Mode Range (Differential Configuration) (Note 10) (Figure 8)		50		V_{DD} − 50	mV
I_{IH}	Input HIGH Current CLK_XTAL1 and CLKb_XTAL2		−10		10	μA
I_{IL}	Input LOW Current CLK_XTAL1 & CLKb_XTAL2		−10		10	μA
LVCMOS − CONTROL AND SDA & SCL/PD INPUTS						
V_{IH}	Input HIGH Voltage for MMC & REFMODE Pins	V_{DD} = 3.3 V V_{DD} = 2.5 V	2.1 1.75		V_{DD}	V
V_{IH}	Input HIGH Voltage for SDA & SCL/PD Pins	V_{DD} = 3.3 V V_{DD} = 2.5 V	2.1 1.75		5.5	V
V_{IL}	Input LOW Voltage for Control Pins and SDA & SCL/PD	V_{DD} = 3.3 V V_{DD} = 2.5 V	GND		0.7 0.7	V
I_{IH}	Input HIGH Current		−150		150	μA
I_{IL}	Input LOW Current		−150		150	μA
VIH_{tri}	Tri−Level Input High Voltage (FSn pins)		V_{DD} x 75%		V_{DD}	V
		V_{DD} = 3.3 V	2.48		V_{DD}	
		V_{DD} = 2.5 V	1.88		V_{DD}	
VIM_{tri}	Tri−Level Input Med Voltage (FSn pins)		V_{DD} x 40%		V_{DD} x 60%	V
		V_{DD} = 3.3 V	1.32		1.98	
		V_{DD} = 2.5 V	1.00		1.67	
VIL_{tri}	Tri−Level Input Low Voltage (FSn pins)		GND		V_{DD} x 25%	V
		V_{DD} = 3.3 V	0.00		0.83	V
		V_{DD} = 2.5 V	0.00		0.63	
RIN	Input Impedance			10		kΩ
CIN	Input Capacitance − Crystal pins; REFMODE = H			2		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

7. LVPECL Outputs loaded with 50 Ω to V_{DDO} – 2 V for proper operation.
8. LVPECL Output parameters vary 1:1 with V_{DDO}.
9. VIH, VIL, V_{th}, and VISE parameters must be complied with simultaneously.
10. V_{CMR} min varies 1:1 with GND, V_{CMR} max varies 1:1 with V_{DD}.
11. V_{IHD}, V_{ILD}, V_{ID} and V_{CMR} parameters must be complied with simultaneously.
12. I_{DD} / V_{DD} is independent of I_{DDOn}/ V_{DDOn}

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Table 9. AC CHARACTERISTICS

V_{DD} = AV_{DDn} = 3.3 V ±5% or 2.5 V ±5%; V_{DDO} = 3.3V ±5% or 2.5 V ±5% or 1.8 V ±5%; GND = 0 V; T_A = −40°C to 85°C (Note 13)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{CLKIN}	External Clock / Crystal Input Frequency − PLL Mode	−1000 ppm	25	+1000 ppm	MHz
f_{INBP}	External Clock Input Frequency – PLL Bypass Mode I²C Mode; f_{in} = f_{out}	1		50	MHz
$f_{CLK1,2,3}$	CLK1, CLK2, CLK3 Typical Output Clock Frequencies; f_{in} = 25 MHz		25 33.33 50 100 125 156.25		MHz
f_{CLK4}	CLK4 Outputs Typical Output Clock Frequencies; f_{in} = 25 MHz Resolution of 1 Hz Integer Frac−N		66.66 106.23 133.33 155.52 161.1328		MHz
fSDA/SCL	Serial Data and Clock Rates		100k		bps
t_{PWSCL}	Serial Clock Pulse Width	1			μs
$t_{w\mu}$	Time SCL/PD Pin must be Held Low to “Wake−up” the Device	100			ns
t_{DC}	Output Clock Duty Cycle (Crystal or Reference Duty Cycle = 50%) PLL Mode; <1 ns t_r / t_f LVPECL f_{out} = 156.25 MHz LVCMOS f_{out} = 33.33 MHz PLL Bypass Mode; Input Duty Cycle = 50%, V_{INPP} ≥ 1.2 V	 47.5 47.5 45	 50 50	 52.5 52.5 55	%
Φ_N	Phase Noise (Integer−N) fout = 156.25 MHz, fin = 25 MHz Crystal, LVPECL 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz 20 MHz		 −115 −130 −140 −145 −153 −153		dBc
Φ_N	Phase Noise (Integer−N) fout = 100 MHz, fin = 25 MHz Crystal, LVCMOS 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz 20 MHz		 −120 −136 −142 −145 −156 −156		dBc
Φ_N	Phase Noise (Frac−N) fout = 155.52 MHz, fin = 25 MHz Crystal, LVPECL 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz 20 MHz		 −115 −127 −131 −135 −152 −153		dBc
Φ_N	Phase Noise (Frac−N) fout = 133.33 MHz, fin = 25 MHz Crystal, LVCMOS 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz 20 MHz		 −117 −126 −126 −131 −153 −153		dBc
$t_{jit}(\Phi)$	RMS Phase Jitter − 25 MHz Crystal (Note 15) Integration Range:12 kHz − 20 MHz fout = 156.25 MHz, Integer CLK_n fout = 155.52 MHz; Frac−N CLK4			 300 1000	fs
$t_{jit}(\Phi)$	Additive RMS Phase Jitter (PLL Bypass in I²C Mode) Integration Range:12 kHz − 5 MHz fout = 25 MHz, CLK1 LVCMOS		50		fs
tpd	Input to Output Propagation Delay (PLL Bypass in I²C Mode) 25 MHz		5		ns

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Table 9. AC CHARACTERISTICS

V_{DD} = AV_{DDn} = 3.3 V ±5% or 2.5 V ±5%; V_{DDO} = 3.3V ±5% or 2.5 V ±5% or 1.8 V ±5%; GND = 0 V; T_A = −40°C to 85°C (Note 13)

Symbol	Characteristic	Min	Typ	Max	Unit
PSRR	Ripple Induced Phase Spur Level 100 kHz & 1 MHz, 100 mVpp, Ripple Injected on V_{DD}/AV_{DDn} ≤ 100 MHz		−60		dBc
t_r /t_f	Output Rise/Fall Times (CLKnA/CLKnB), 20% − 80% of $VDDO_n$ fout = 156.25 Mhz LVPECL fout = 33.33 Mhz @ VDDO = 3.3 V LVCMOS – 5 pF	 120 500	 200 800	 300 1000	ps
V_{INPP}	Input Voltage Swing (Differential Configuration) (Note 14)	100		1200	mV
Stabilization Time	Stabilization Time From Power−up V_{DD} = 3.3 V to First Edge Out Upon Reprogram – (Pin−Strap mode), Change of Configuration Power−up to Static Output Levels – (Pin−Strap mode) Power−up to I^2C Ready		5 3 1 5	6 3 	ms
t_{PWRDWN}	Time to Power Down, SCL/PD Low−to−High	50	100	200	µs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

13. Measured by using a 25 MHz crystal as clock source. All LVPECL outputs are loaded with an external R_L = 50 Ω to V_{DDO} – 2 V (Figure 9); LVCMOS outputs loaded with R_S = 33 Ω, C_L = 5 pF, 5” 50 Ω trace, (Figure 11).
14. Input and output voltage swings are single−ended measurements operating in a differential mode.
15. V_{DD} = 3.3 V, V_{DDO} = 2.5 V (LVPECL) or 1.8 V (LVCMOS).

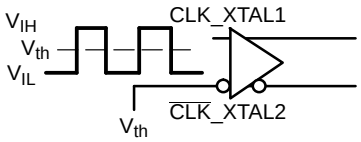


Figure 3. Differential Input Driven Single−Ended

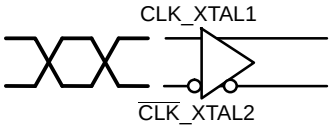


Figure 4. Differential Inputs Driven Differentially

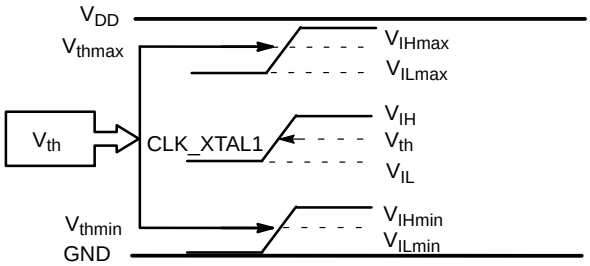


Figure 5. V_{th} Diagram

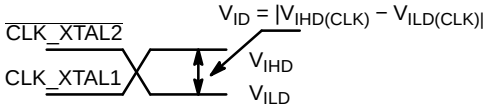


Figure 6. Differential Inputs Driven Differentially

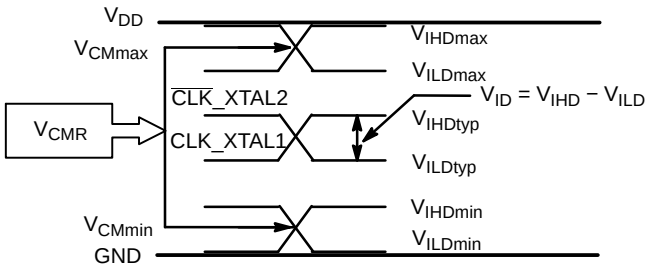


Figure 7. V_{CMR} Diagram

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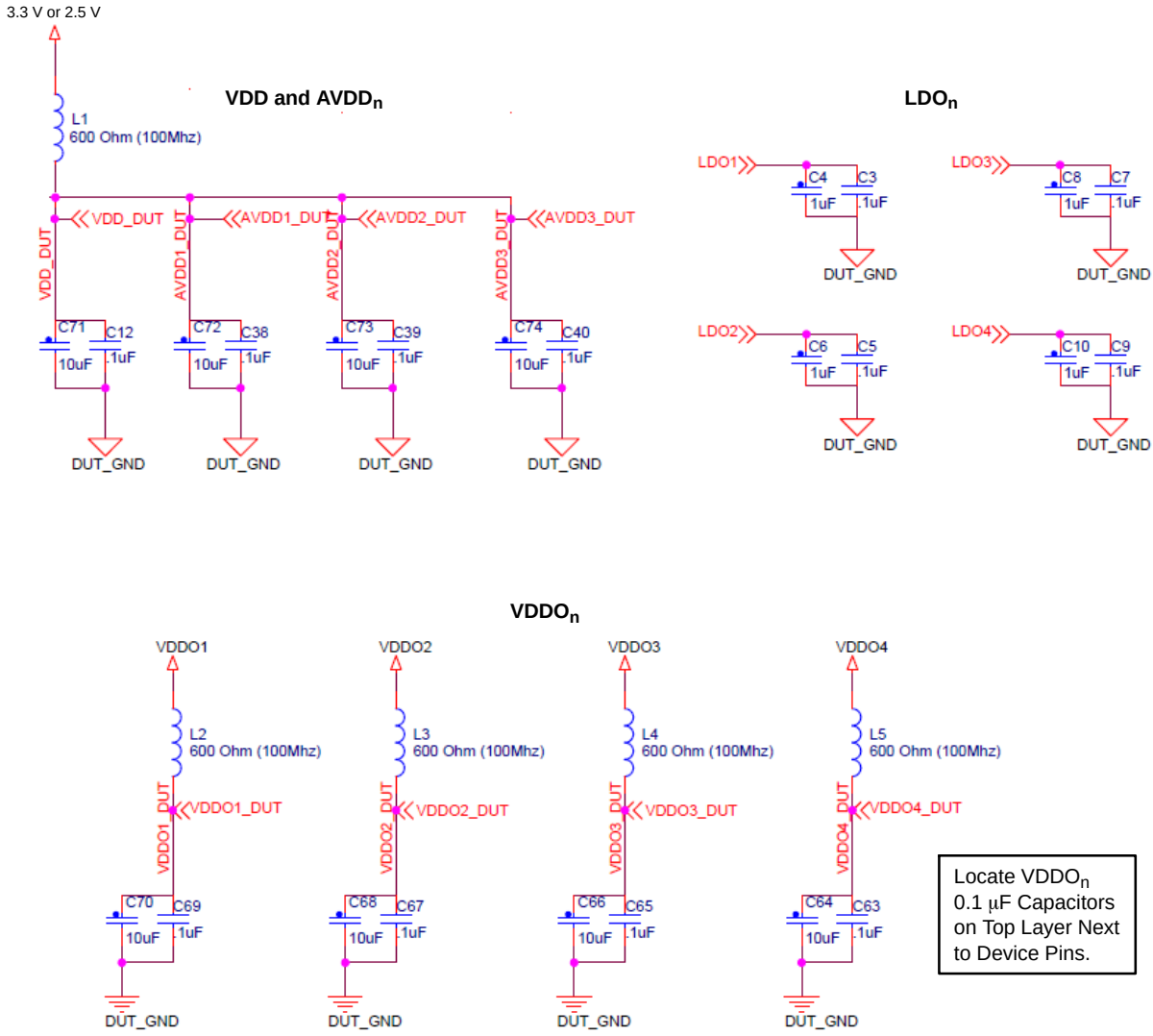


Figure 8. NB3H5150 Power Supply Filter Schemes

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Table 10. RECOMMENDED CRYSTAL SPECIFICATIONS

Crystal	Fundamental AT−Cut
Frequency	25 MHz
Load Capacitance	16 pF − 20 pF
Shunt Capacitance, C0	7 pF Max
Equivalent Series Resistance	50 Ω Max
Initial Accuracy at 25°C	± 20 ppm
Temperature Stability	± 30 ppm
Aging	± 20 ppm
C0/C1 Ratio	250 Max
Crystal max Drive Level	100 μW

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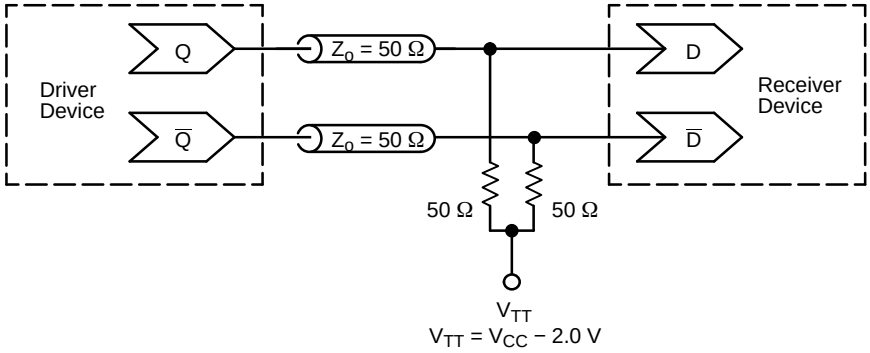


Figure 9. Typical Termination for LVPECL Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

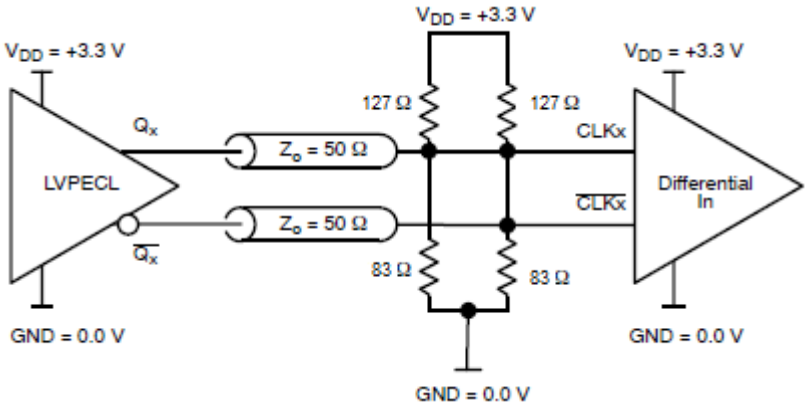


Figure 10. Optional LVPECL output Loading and Termination

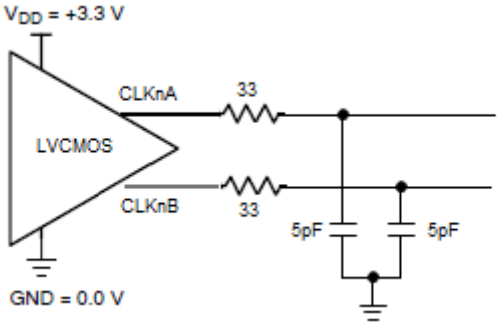


Figure 11. Typical LVCMOS Output Test Setup for Evaluation

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Interfacing from 3.3 V LVPECL to LVDS

Since the output levels V_{OH} and V_{OL} of 3.3 V LVPECL are more positive than the input range of LVDS receiver, a special interface is required. (See Figures 12 and 13). Furthermore, the open emitter design of the ECL output structure needs proper termination, which can be implemented with a resistor divider network to generate proper LVDS DC levels (eq. 1).

$$R_{E1} + R_{E2} = R_E \quad \text{(eq. 1)}$$

The resistor divider network will divide the output common mode voltage of LVPECL (V_{CM}(LVPECL)) to input common mode voltage of LVDS (V_{CM}(LVDS)).

$$\frac{R_{E2}}{R_{E1} + R_{E2}} = \frac{V_{CM(LVDS)}}{V_{CM(LVPECL)}} \quad \text{(eq. 2)}$$

Where:

R_{E1} = partial emitter current bias resistor

R_{E2} = partial emitter current bias resistor

$R_E = R_{E1} + R_{E2}$, the total emitter current bias resistor (see AND8020)

V_{CM}(LVPECL) = Common Mode Voltage

V_{CM}(LVDS) = Common Mode Voltage

3.3 V LVPECL output will be able to drive an LVDS receiver with or without an internal 100 Ω termination resistor.

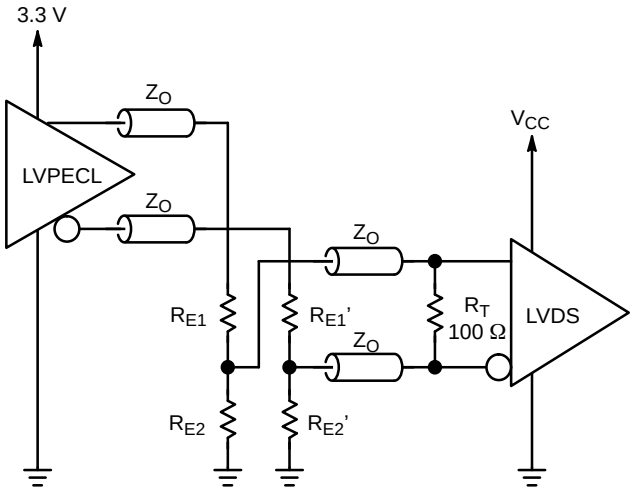


Figure 12. Interfacing 3.3 V LVPECL to LVDS

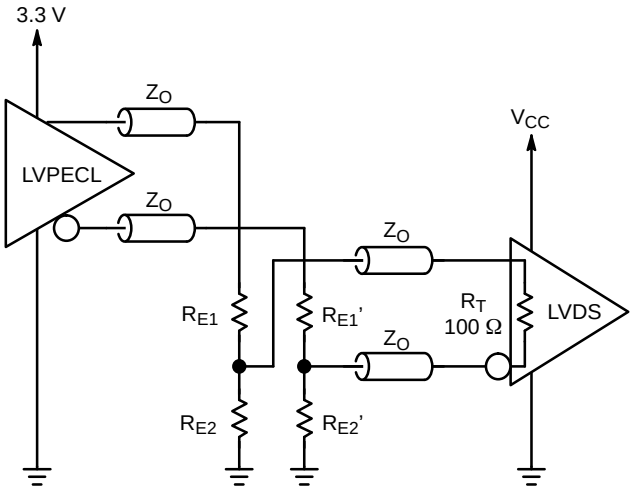


Figure 13. Interfacing LVPECL to LVDS with Internal 100 Ω Termination Resistor

Examples:

For 50 Ω controlled impedance, the resistor values for 3.3V LVPECL converted to LVDS voltage levels are as follows:

R_{E1} = 55 Ω

R_{E2} = 95 Ω

$R_{E1} + R_{E2} = R_E$ = 150 Ω

R_T = 100 Ω

V_{CM}(LVPECL) = 1.9 V

V_{CM}(LVDS) = 1.2 V

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Interfacing from 2.5 V LVPECL to LVDS

Provided that the LVDS receiver can tolerate large input voltage peak to peak amplitude, the 2.5 V LVPECL output can be directly interfaced to an LVDS receiver using proper ECL termination. The 2.5 V LVPECL output will be able to drive an LVDS receiver with or without internal 100 Ω termination resistor. (See Figures 14, 15 and 16).

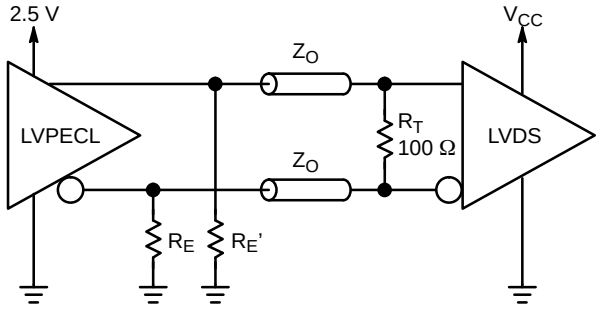


Figure 14. Interfacing 2.5 V LVPECL to LVDS with External 100 Ω Termination Resistor

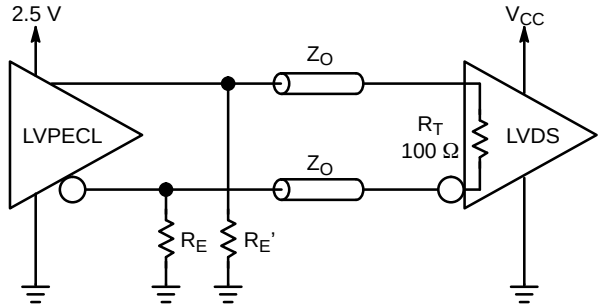


Figure 15. Interfacing 2.5 V LVPECL to LVDS with Internal 100 Ω Termination Resistor

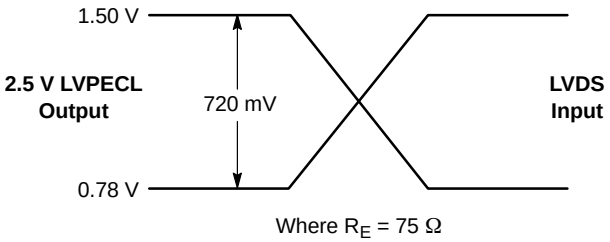


Figure 16. PSPICE Simulation Levels of 2.5V LVPECL to LVDS Interface with Example Resistor Values

Furthermore, a series termination can be used to reduce the amplitude of the signal as described in AND8020 application note, by placing R_S resistor between the driver and the transmission line. (See Figures 17, 18 and 19).

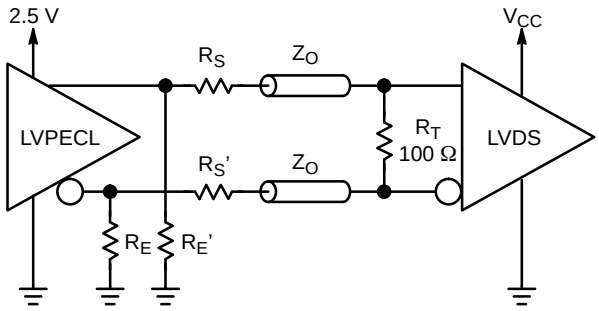


Figure 17. Interfacing 2.5 V LVPECL to LVDS with Series R_S and External 100 Ω Termination Resistor

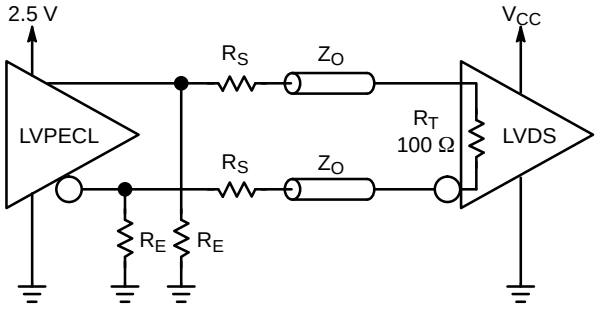


Figure 18. Interfacing 2.5 V LVPECL to LVDS with Series R_S and Internal 100 Ω Termination Resistor

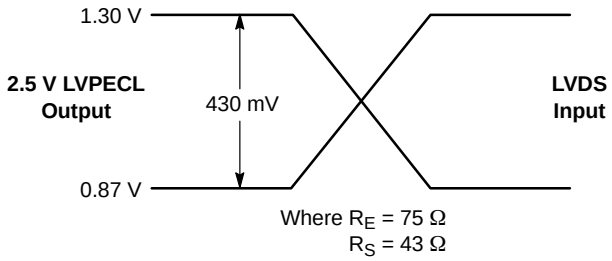


Figure 19. PSPICE Simulation Levels of 2.5V LVPECL to LVDS Interface with Series R_S Resistor

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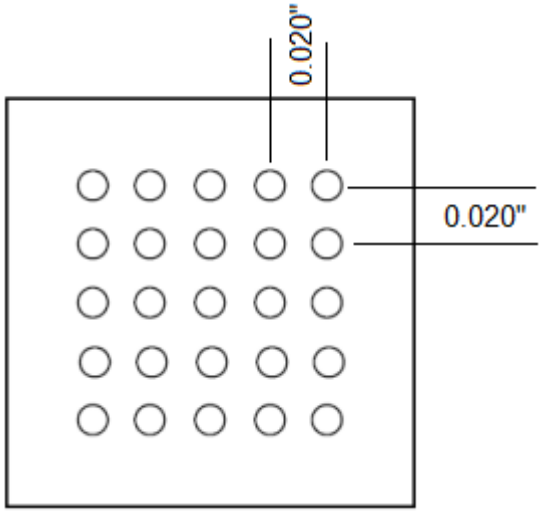


Figure 20. Via Layout Recommendation for Exposed Pad, QFN−32 Package

The exposed pad on the NB3H5150 QFN−32 package carries all of the power supply return currents. It is therefore important that the necessary current capability be satisfied, as well as the thermal transfer from the die to the PCB. Figure 20 shows a recommended via layout pattern for the exposed pad. Via spacing = 0.02”, filled vias preferred.

ORDERING INFORMATION

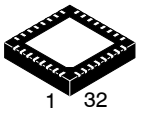
Device	Marking	Tables	Package	Shipping†
NB3H5150MNTXG	NB3H 5150	3 & 4	QFN32 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

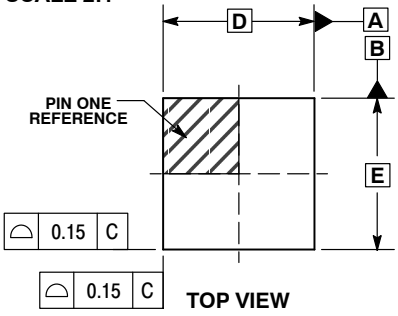
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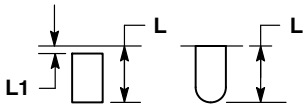
QFN32 5x5, 0.5P
CASE 485CE
ISSUE O

DATE 07 FEB 2012

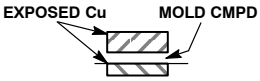


SCALE 2:1

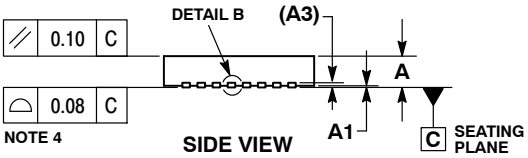


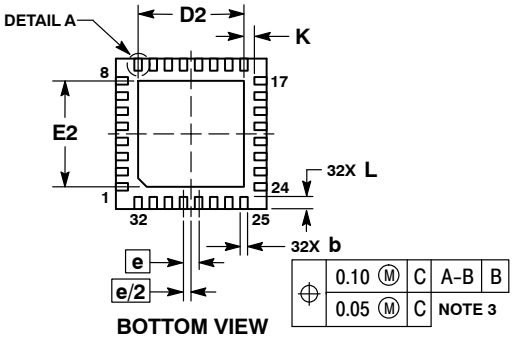


DETAIL A
ALTERNATE CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION

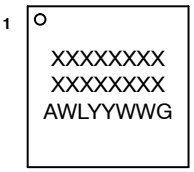




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.20	0.30
D	5.00 BSC	
D2	3.40	3.60
E	5.00 BSC	
E2	3.40	3.60
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15

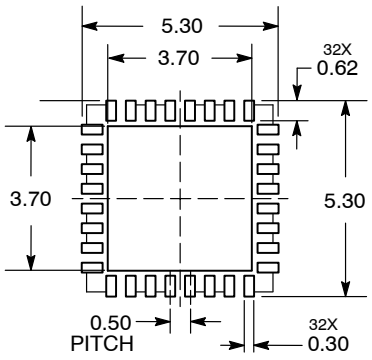
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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