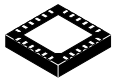
# 3.3V / 2.5V / 1.8V / 1.5V 2:1:5 LVCMOS Fanout Buffer

# NB3F8L3005C



QFN24
G SUFFIX
CASE 485DJ

## Description

The NB3F8L3005C is a 2:1:5 Clock / Data fanout buffer operating on a 3.3 V / 2.5 V Core $V_{DD}$ and two flexible 3.3 V / 2.5 V / 1.8 V / 1.5 V $VDDO_x$ supplies which must be equal or less than $V_{DD}$.

A Mux selects between a Crystal input, or a differential/SE Clock / Data inputs. Differential Inputs accept LVPECL, LVDS, HCSL, or SSTL and Single−Ended levels. The MUX control line, SEL selects CLK/$\overline{\text{CLK}}$, or Crystal input pins per Table 3. The Crystal input is disabled when a Clock input is selected. Output enable pin, OE, synchronously forces a High Impedance state (Hi−Z) when Low per Table 4.

Outputs consist of five single−ended LVCMOS outputs.

## Features

- Five LVCMOS / LVTTL Outputs up to 200 MHz
- Differential Inputs Accept LVPECL, LVDS, HCSL, SSTL, or LVCMOS/LVTTL
- Crystal Interface
- Crystal Input Frequency Range: 10 MHz to 50 MHz
- Output Skew: 10 ps Typical
- Additive RMS Phase Jitter @ 156.25 MHz, (12 kHz – 20 MHz): 0.03 ps (Typical)
- Synchronous Output Enable
- Output Defined Level When Input is Floating
- Power Supply Modes:
  - Single 3.3 V ± 5%
  - Single 2.5 V ± 5%
  - Mixed 3.3 V ± 5% Core/2.5 V ± 5% Output Operating Supply
  - Mixed 3.3 V ± 5% Core/1.8 V ± 0.2 V Output Operating Supply
  - Mixed 3.3 V ± 5% Core/1.5 V ± 0.15 V Output Operating Supply
  - Mixed 2.5 V ± 5% Core/ 1.8 V ± 0.2 V Output Operating Supply
  - Mixed 2.5 V ± 5% Core /1.5 V ± 0.15 V Output Operating Supply
- Two Separate Output Bank Power Supplies
- Industrial Temperature Range: −40°C to 85°C
- These are Pb−Free Devices

## MARKING DIAGRAM


| | |
|---|---|
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

## ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

## Applications

- Clock Distribution
- Networking and Communications
- High End Computing
- Wireless and Wired Infrastructure

## End Products

- Servers
- Ethernet Switch/Routers
- ATE
- Test and Measurement

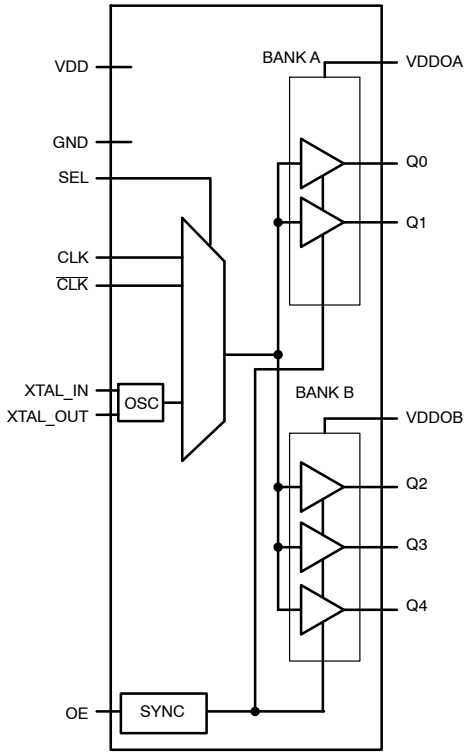



**Figure 1. Simplified Logic Diagram**

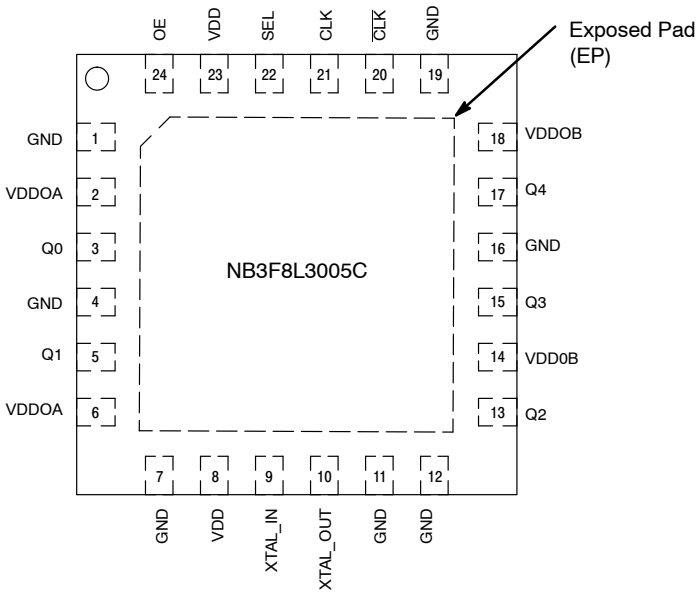



**Figure 2. Pinout Configuration** (Top View)

**Table 1. PIN DESCRIPTION**

| Number | Name | Type | Input Default | Description |
|---|---|---|---|---|
| 3, 5 | Q0, Q1 | LVCMOS | | Outputs – Bank A |
| 13, 15, 17 | Q2, Q3, Q4 | LVCMOS | | Outputs – Bank B |
| 2, 6 | VDDOA | Power | | Positive Supply Pins for Bank A Outputs Q0 – Q1 |
| 14, 18 | VDDOB | Power | | Positive Supply Pins for Bank B Outputs Q2 – Q4 |
| 1, 4, 7, 11, 12, 16, 19 | GND | GND | | Ground Supply |
| 8, 23 | VDD | Power | | $V_{DD}$ Positive Supply pin for Core and Inputs. |
| 9 | XTAL_IN | XTAL OSC / CLK Input | | Crystal Oscillator Interface or External Clock Source at LVCMOS Levels |
| 10 | XTAL_OUT | XTAL OSC Output | | Crystal Interface |
| 20 | $\overline{CLK}$ | Diff / SE Input | Pullup / Pulldown | Inverting differential clock input |
| 21 | CLK | Diff / SE Input | Pulldown | Non-inverting clock input |
| 22 | SEL | LVCMOS / LVTTL Input | Pulldown | Input clock select. See Table 3 for function. Input Pulldown |
| 24 | OE | LVCMOS / LVTTL Input | Pulldown | Output Enable Control. See Table 4 for function. |
| – | EP | – | | The Exposed Pad (EP) on the QFN−24 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat−sinking conduit. The pad is electrically connected to the die, and must be electrically connected to GND. |

1. All VDD, $VDDO_x$ and GND pins must be externally connected to a power supply to guarantee proper operation. Bypass each $V_{DD}$ and $VDDO_x$ with 0.01 μF CAP to GND.

**Table 2. PIN CHARACTERISTICS**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | 4 | | pF |
| $R_{PU}$ | Input Pullup Resistor | | 50 | | kΩ |
| $R_{PD}$ | Input Pulldown Resistor | | 50 | | kΩ |
| $C_{PD}$ | Power Dissipation Capacitance (per output)<br>VDDO = 3.3 V<br>VDDO = 2.5 V<br>VDDO = 1.8 V<br>VDDO = 1.5 V | | | | pF |
| $R_{OUT}$ | Output Impedance<br>VDDO = 3.3 V<br>VDDO = 2.5 V<br>VDDO = 1.8 V<br>VDDO = 1.5 V | | 20 | | Ω |

## FUNCTION TABLES

**Table 3. CLOCK ENABLE (SELx) FUNCTION TABLE**

| SEL Input | Selected Input Clock |
|---|---|
| 0 | CLK/$\overline{CLK}$ |
| 1 | Crystal Osc Input |

**Table 4. CLOCK OUTPUT ENABLE (OE) FUNCTION TABLE**

| OE Input | $Q_n$ Outputs |
|---|---|
| 0 | Disabled, High Impedance |
| 1 | Outputs Enabled |

**Table 5. CLK INPUT VS. OUTPUT STATUS**

| Input Condition | Output |
|---|---|
| CLK/$\overline{CLK}$ = OPEN | Logic LOW |
| CLK/$\overline{CLK}$ = GND | Undefined |
| CLK = HIGH; $\overline{CLK}$ = LOW | Logic HIGH |
| CLK = LOW; $\overline{CLK}$ = HIGH | Logic LOW |

**Table 6. CRYSTAL CHARACTERISTICS**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Mode of Oscillation | Fundamental | | | |
| Frequency | 10 | | 50 | MHz |
| Equivalent Series Resistance (ESR) | | | 50 | Ω |
| Shunt Capacitance | | | 7 | pF |
| Drive Power | | | 100 | μW |

**Table 7. ATTRIBUTES**

| Characteristic | | Value |
|---|---|---|
| ESD Protection | Human Body Model<br>Machine Model | >2 kV<br>200 V |
| Moisture Sensitivity Level (Note 2) | QFN24 | MSL 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in |
| Transistor Count | | 474 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

2. For additional information, see Application Note AND8003/D.

**Table 8. MAXIMUM RATINGS** (Note 3)

| Symbol | Parameter | | Condition | Rating | Unit |
|---|---|---|---|---|---|
| $V_{DD}$, $VDDO_x$ | Positive Power Supply | | GND = 0 V | 4.6 | V |
| $V_I$ | Input Voltage<br>XTAL_IN<br>Diff, SELx, OE Inputs | | | <br>$0 \le V_I \le V_{DD}$<br>$-0.5 \le V_I \le V_{DD} + 0.5$ | V |
| $V_O$ | Output Voltage | | | $-0.5 \le V_O \le VDDO_x + 0.5$ | V |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | QFN24<br>QFN24 | 0 lfpm<br>500 lfpm | 37<br>32 | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | QFN24 | (Note 3) | 11 | °C/W |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

**Table 9. POWER SUPPLY CHARACTERISTICS** $V_{DD} \geq V_{DDO}$; $V_{DD}$ = 3.3 V ± 5% (3.135 V to 3.465 V) or $V_{DD}$ = 2.5 V ±5% (2.375 V to 2.625 V) and $V_{DDOx}$ = 3.3 V ± 5% (3.135 V to 3.465 V) or 2.5 V ± 5% (2.375 V to 2.625 V) or 1.8 V ± 0.2 V (1.6 V to 2.0 V) or 1.5 V ± 0.15 V (1.35 V to 1.65 V); $T_A$ = −40°C to 85°C

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | $V_{DD}$ Power Supply Current | $f_{IN}$ = 0 MHz<br>$V_{DDO}$ = 3.3 V, $f_{IN}$ = 100 MHz<br>$V_{DDO}$ = 2.5 V, $f_{IN}$ = 100 MHz | | 30<br>30<br>20 | 38 | mA |
| $I_{DDO}$ | $V_{DDO}$ Power Supply Current | OE = 0, no load<br>$V_{DDO}$ = 3.3 V, OE = 1, $f_{IN}$ = 100 MHz<br>$V_{DDO}$ = 2.5 V, OE = 1, $f_{IN}$ = 100 MHz | | 0.1<br>7<br>5 | | mA |
| $I_{DD}$ + $I_{DDO}$ | Total Device Current with Loads on All Outputs | OE = 1, $f_{IN}$ = 100 MHz<br>OE = 0 | | 48<br>16 | | mA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

**Table 10. DC CHARACTERISTICS** $T_A$ = −40°C to 85°C

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | LVCMOS / LVTTL Input High Voltage (OE, SEL) | $V_{DD}$ = 3.3 V ±5%<br>$V_{DD}$ = 2.5 V ± 5% | 1.6<br>1.3 | | $V_{DD}$ + 0.3<br>$V_{DD}$ + 0.3 | V |
| $V_{IL}$ | LVCMOS / LVTTL Input Low Voltage (OE, SEL) | $V_{DD}$ = 3.3 V ±5%<br>$V_{DD}$ = 2.5 V ± 5% | −0.3<br>−0.3 | | 0.8<br>0.4 | V |
| $I_{IH}$ | Input High Current<br>OE, SEL<br>CLK/$\overline{CLK}$ | <br>$V_{DD}$ = $V_{IN}$ = 3.465 V<br>$V_{DD}$ = $V_{IN}$ = 3.465 V or 2.625 V | | | <br>100<br>100 | μA |
| $I_{IL}$ | Input Low Current<br>OE, SEL<br>CLK<br>$\overline{CLK}$ | <br>$V_{DD}$ = 3.465 V; $V_{IN}$ = 0.0 V<br>$V_{DD}$ = 3.465 V or 2.625 V $V_{IN}$ = 0.0 V<br>$V_{DD}$ = 3.465 V or 2.625 V $V_{IN}$ = 0.0 V | <br>−5<br>−5<br>−150 | | <br>5 | μA |
| $V_{OH}$ | Output High Voltage | | $V_{DDO}$ − 0.1 | | | V |
| $V_{OL}$ | Output Low Voltage | $VDDO_x$ = 3.3 V ± 5% or 2.5 V ± 5% | | | 0.5 | V |
| | | $VDDO_x$ = 1.8 V ± 0.2 V | | | 0.4 | |
| | | $VDDO_x$ = 1.5 V ± 0.15 V | | | 0.37 | |
| $V_{PP}$ | Peak−to−Peak Input Voltage<br>$V_{IL}$ > −0.3 V CLKx/$\overline{CLKx}$ | $V_{DD}$ = 3.3 V ±5% or $V_{DD}$ = 2.5 V ± 5% | 0.15 | | 1.3 | V |
| $V_{IHCMR}$ | Input High Level Common Mode Range<br>$V_{CM}$ = $V_{IH}$; $V_{IL}$ > −0.3 V CLKx/$\overline{CLKx}$ | $V_{DD}$ = 3.3 V ±5% or $V_{DD}$ = 2.5 V ± 5% | 0.5 | | $V_{DD}$ − 0.85 | V |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

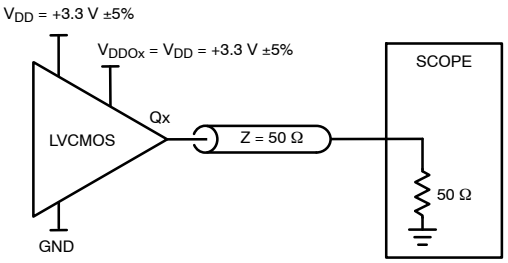
**Table 11. AC CHARACTERISTICS** $V_{DD} \geq V_{DDO}$; $V_{DD}$ = 3.3 V ± 5% (3.135 V to 3.465 V) or $V_{DD}$ = 2.5 V ±5% (2.375 V to 2.625 V) and $V_{DDOx}$ = 3.3 V ± 5% (3.135 V to 3.465 V) or 2.5 V ± 5% (2.375 V to 2.625 V) or 1.8 V ± 0.2 V (1.6 V to 2.0 V) or 1.5 V ± 0.15 V (1.35 V to 1.65 V); $T_A$ = −40°C to 85°C

| Symbol | Parameter | | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | Using External Crystal | | 10 | | 50 | MHz |
| | | Using External Clock Source (Note 4) | | DC | | 200 | MHz |
| $t_{sk(o)}$ | Output Skew (Notes 5 and 6) | | | | 10 | 25 | ps |
| $t_{JITTER\Phi}$ | Additive RMS Phase Jitter (Integrated 12 kHz – 20 MHz) $f_C$ = 156.25 MHz | Input clock from CLK/$\overline{CLK}$ | $V_{DDOx}$ = 3.3 V ± 5% | | 0.03 | | ps |
| | | | $V_{DDOx}$ = 2.5 V ± 5% | | 0.03 | | |
| | | | $V_{DDOx}$ = 1.8 V ± 0.2 V | | 0.03 | | |
| | | | $V_{DDOx}$ = 1.5 V ± 0.15 V | | 0.03 | | |
| | | External clock over drives crystal interface | $V_{DDOx}$ = 3.3 V ± 5% | | 0.03 | | |
| | | | $V_{DDOx}$ = 2.5 V ± 5% | | 0.03 | | |
| | | | $V_{DDOx}$ = 1.8 V ± 0.2 V | | 0.03 | | |
| | | | $V_{DDOx}$ = 1.5 V ± 0.15 V | | 0.03 | | |
| | | Input clock from crystal | $V_{DDOx}$ = 3.3 V ± 5% | | 0.03 | | |
| | | | $V_{DDOx}$ = 2.5 V ± 5% | | 0.03 | | |
| | | | $V_{DDOx}$ = 1.8 V ± 0.2 V | | 0.03 | | |
| | | | $V_{DDOx}$ = 1.5 V ± 0.15 V | | 0.03 | | |
| $t_R$ / $t_F$ | Output Rise/Fall Time (20% and 80%) $C_L$ = 10 pF | | $V_{DDOx}$ = 3.3 V ± 5% | 150 | 350 | 500 | ps |
| | | | $V_{DDOx}$ = 2.5 V ± 5% | 150 | 350 | 500 | |
| | | | $V_{DDOx}$ = 1.8 V ± 0.2 V | 150 | 350 | 600 | |
| | | | $V_{DDOx}$ = 1.5 V ± 0.15 V | 150 | 350 | 600 | |
| odc | Output Duty Cycle | | $V_{DDOx}$ = 3.3 V ± 5% | 45 | | 55 | % |
| | | | $V_{DDOx}$ = 2.5 V ± 5% | 40 | | 60 | |
| | | | $V_{DDOx}$ = 1.8 V ± 0.2 V | 40 | | 60 | |
| | | | $V_{DDOx}$ = 1.5 V ± 0.15 V | 40 | | 60 | |
| PSRR | Power Supply Ripple Rejection | | 100 kHz, 100 $mV_{PP}$ Ripple Injected on $V_{DD}$, $V_{DDO}$ = 2.5 V | | −44 | | dBc |
| $t_{EN}$ | Output Enable Time (Note 7) | OE | | | | 4 | cycles |
| $t_{DIS}$ | Output Disable Time (Note 7) | OE | | | | 4 | cycles |
| MUX_ISOLATION | MUX_ISOLATION | | 155.52 MHz | 55 | | | dB |

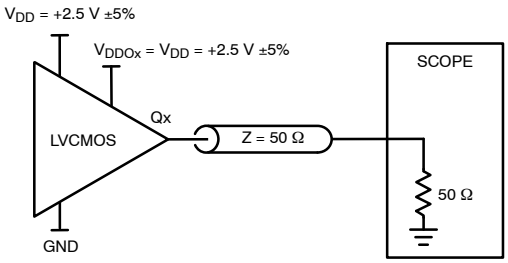
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

4. XTAL_IN can be overdriven relative to a signal a crystal would provide.
5. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $VDDO_x/2$.
6. This parameter is defined in accordance with JEDEC Standard 65.
7. These parameters are guaranteed by characterization. Not tested in production. See Parameter Measurement Information
8. AC parameters for LVCMOS are dependent upon output capacitive loading.

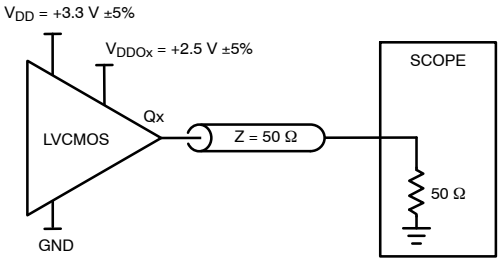
## PARAMETER MEASUREMENT INFORMATION



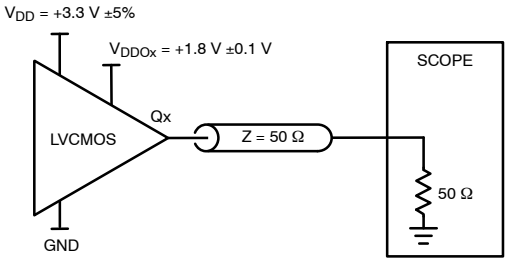

**3.3 V Core / 3.3 V Output Load AC Test Circuit**



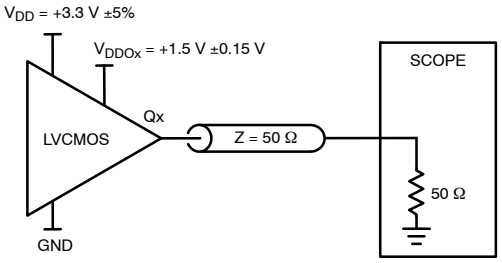

**2.5 V Core / 2.5 V Output Load AC Test Circuit**



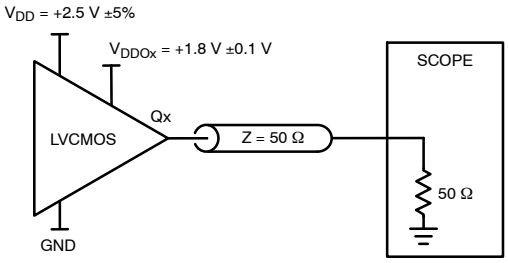

**3.3 V Core / 2.5 V Output Load AC Test Circuit**



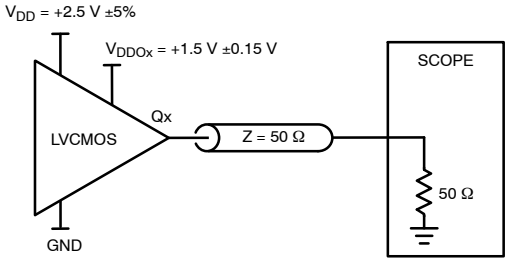

**3.3 V Core / 1.8 V Output Load AC Test Circuit**




**3.3 V Core / 1.5 V Output Load AC Test Circuit**




**2.5 V Core / 1.8 V Output Load AC Test Circuit**




**2.5 V Core / 1.5 V Output Load AC Test Circuit**

**Figure 3. Operational Supply and Termination Test Conditions**

## PARAMETER MEASUREMENT INFORMATION

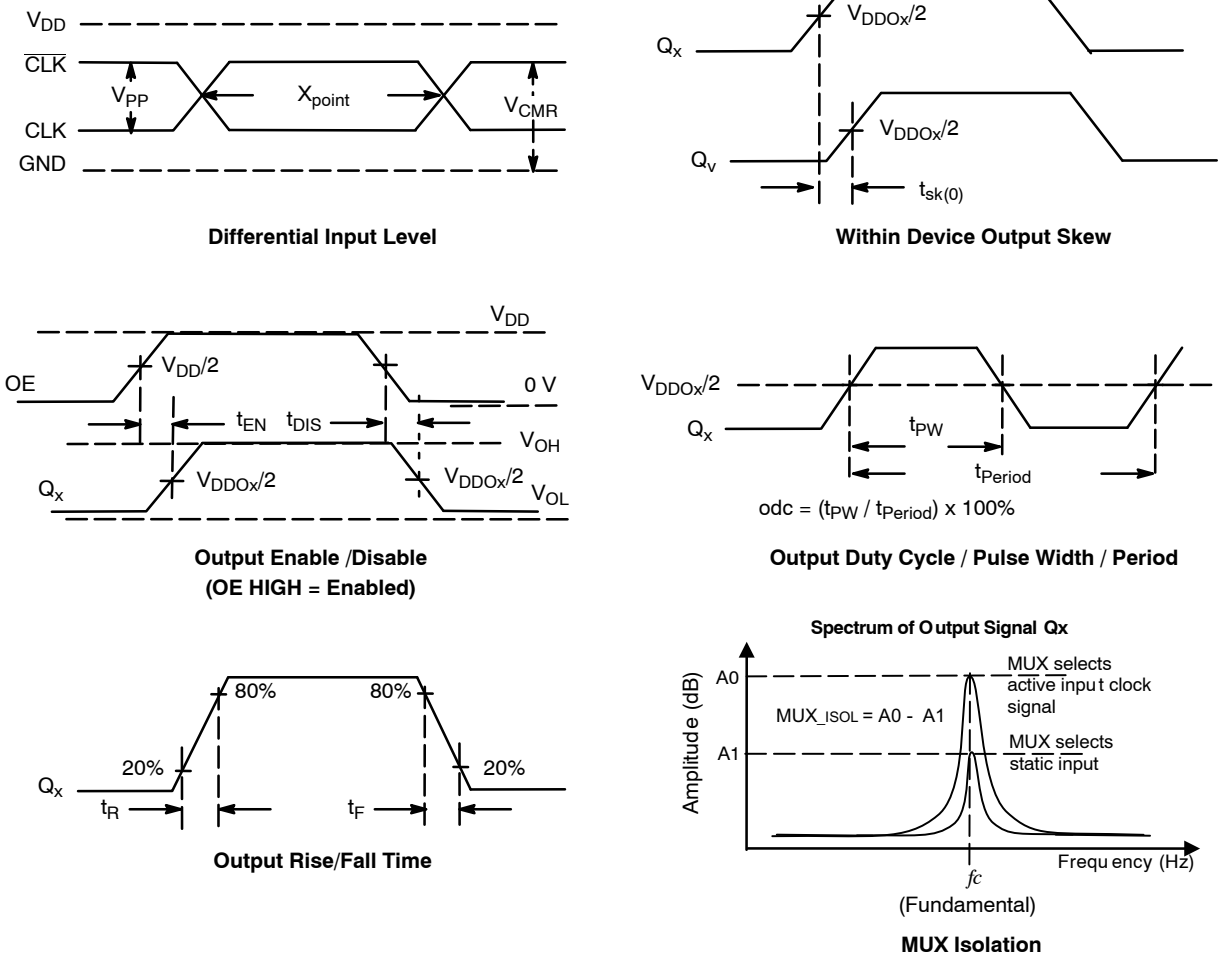



**Figure 4. Operational Waveforms and MUX Input Isolation Plot**

## APPLICATION INFORMATION

### Recommendations for Unused LVCMOS Output Pins

### Inputs:

### CLK/$\overline{\text{CLK}}$ Inputs

For applications not requiring the use of the differential input, both CLK and $\overline{\text{CLK}}$ can be left floating. Though not required, but for additional protection, a 1 kΩ resistor can be tied from CLK to ground.

### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1 kΩ resistor can be tied from XTAL_IN to ground.

### LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1 kΩ resistor can be used.

### Power Supplies

**VDD** is the power supply for the core and input circuitry.

**VDDOA** and **VDDOB** are two separate positive power supplies for two banks of outputs:

VDDOA pins 2 and 6 are connected internally for outputs Q0 – Q1.

VDDOB pins 14 and 18 are connected internally for outputs Q2 – Q4.

### Differential Input with Single−Ended Interconnect

Refer to Figure 5 to interconnect a single−ended to a Differential Pair of inputs. The reference bias voltage $V_{REF} = V_{DD}/2$ is generated by the resistor divider of R3 and R4. Bypass capacitor (C1) can filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. Adjust R1 and R2 to common mode voltage of the signal input swing to preserve duty cycle.

This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination by R1 and R2 will attenuate the signal amplitude in half. Termination may be done by using Rs or by using R1 and R2. First, Rs = 0 and then R3 and R4 in parallel should equal the transmission line impedance. For most 50 Ω applications, R1 and R2 can be 100 Ω. The differential input can handle full rail LVCMOS signaling, but it is recommended that the amplitude be reduced. The datasheet specifies a differential amplitude which needs to be doubled for a single ended equivalent stimulus. $V_{ILmin}$ cannot be less than −0.3 V and $V_{IHmax}$ cannot be more than $V_{DD}$ + 0.3 V. The datasheet specifications are characterized and guaranteed by using a differential signal.

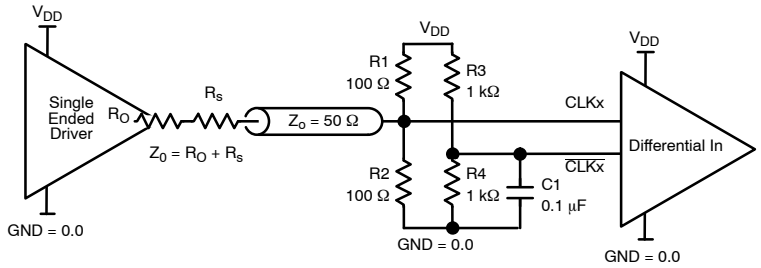



**Figure 5. Differential Input with Single−ended Interconnect**

### Crystal Input Interface

The device has been characterized with 18 pF parallel resonant crystals. The capacitor values, C1 and C2, shown in Figure 6 below as 15 pF were determined using an 18 pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

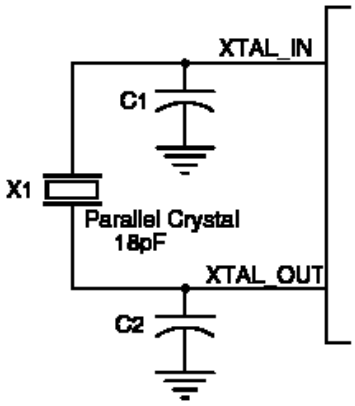



**Figure 6. Crystal Input Interface**

### CLOCK Overdriving the XTAL Interface

The XTAL_IN input can accept a single−ended LVCMOS signal through an AC coupling capacitor. A general LVCMOS interface diagram is shown in Figure 7 and a general LVPECL interface in Figure 8. The XTAL_OUT pin must be left floating. The maximum amplitude of the input signal should not exceed 2 V and the input edge rate can be as slow as 10 ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50 Ω applications, R1 and R2 can be 100 Ω. This can also be accomplished by removing R1 and making R2 50 Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

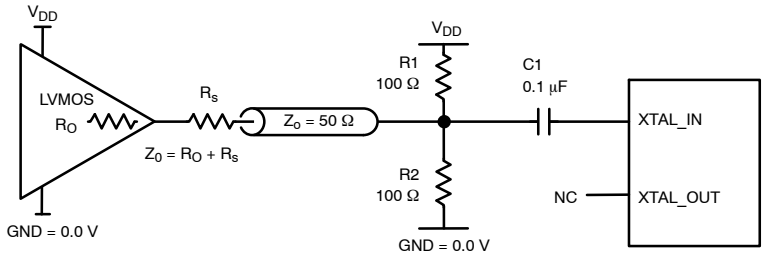



**Figure 7. General Diagram for LVCMOS Driver to XTAL Input Interface Use Rs or R1 / R2**

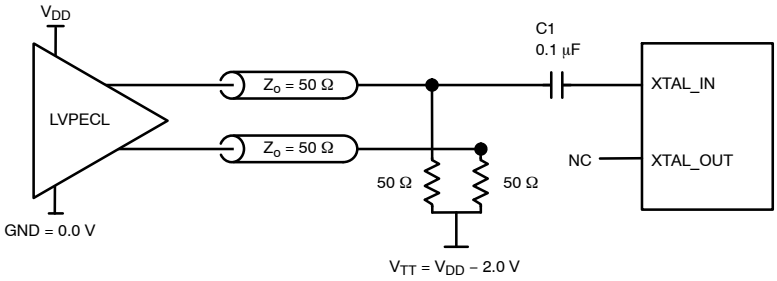



**Figure 8. General Diagram for LVPECL Driver to XTAL Input Interface**

### Differential Clock Input Interface

The CLK / $\overline{CLK}$ accept LVDS, LVPECL, SSTL, HCSL differential signals. Signals must meet the $V_{PP}$ and VCMR input requirements. Figures 9 to 13 show interface examples for the CLK / $\overline{CLK}$ input with built−in 50 Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

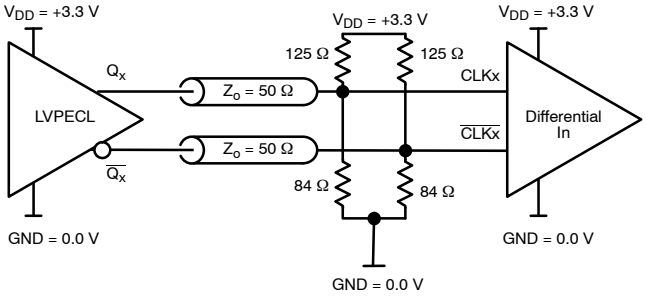



**Figure 9. CLK / $\overline{CLK}$ Input Driven by 3.3 V LVPECL Driver (Thevenin Parallel Termination)**

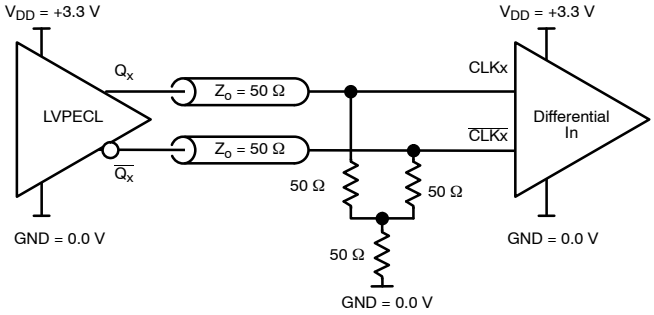



**Figure 10. CLK / $\overline{CLK}$ Input Driven by 3.3 V LVPECL Driver ("Y" Parallel Termination)**

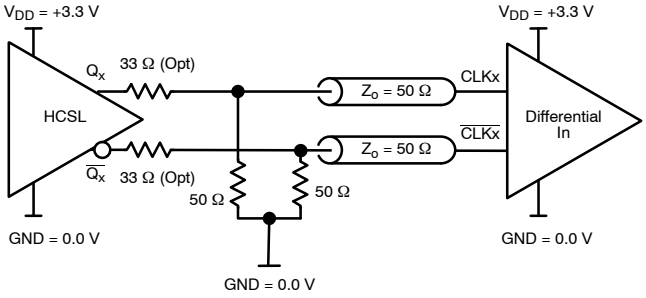



**Figure 11. CLK / $\overline{CLK}$ Input Driven by a 3.3 V HCSL Driver**

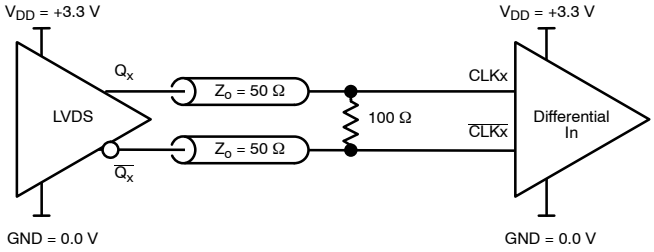



**Figure 12. CLK / $\overline{CLK}$ Input Driven by 3.3 V LVDS Driver**

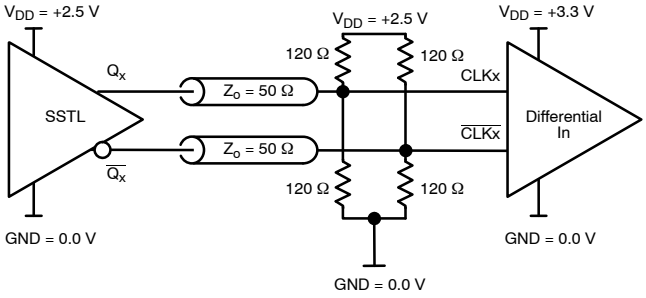



**Figure 13. CLK / $\overline{CLK}$ Input Driven by 2.5 V SSTL Driver**

### VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 14. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts. While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) is application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13 mils (0.30 to 0.33 mm) with 1 oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only.

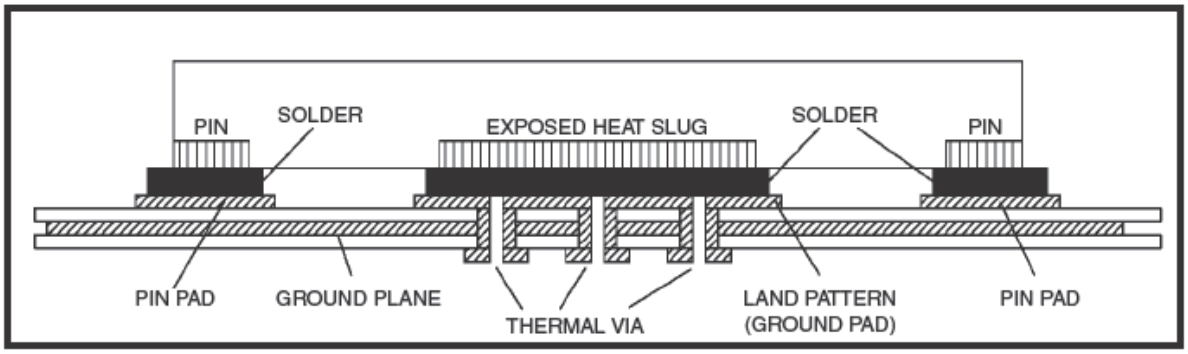



**Figure 14. Suggested Assembly for Exposed Pad Thermal Release Path – Cut−away View (not to scale)**

### ORDERING INFORMATION

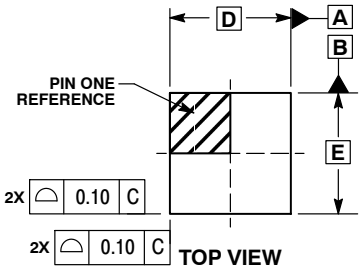
| Device | Package | Shipping† |
|---|---|---|
| NB3F8L3005CMNTXG | QFN24<br>(Pb−Free) | 3000 / Tape & Reel |
| NB3F8L3005CMNTBG | QFN24<br>(Pb−Free) | 1000 / Tape & Reel |

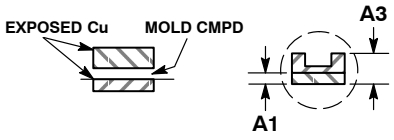
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**QFN24, 4x4, 0.5P**
CASE 485DJ
ISSUE O

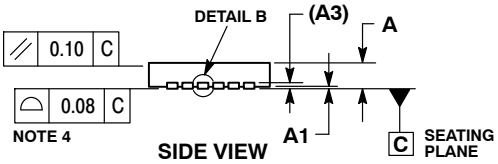
DATE 28 OCT 2013

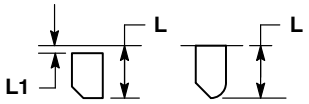
SCALE 2:1




**DETAIL B**
**ALTERNATE CONSTRUCTIONS**

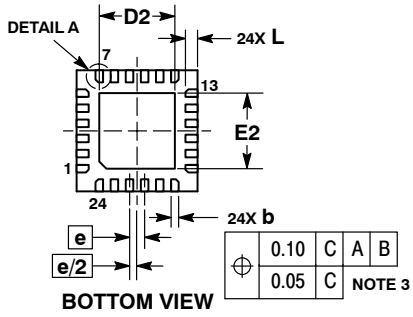


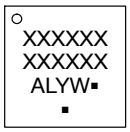

**DETAIL A**
**ALTERNATE CONSTRUCTIONS**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 0.90 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 4.00 BSC | |
| D2 | 2.40 | 2.60 |
| E | 4.00 BSC | |
| E2 | 2.40 | 2.60 |
| e | 0.50 BSC | |
| L | 0.30 | 0.50 |
| L1 | --- | 0.15 |




## GENERIC MARKING DIAGRAM*

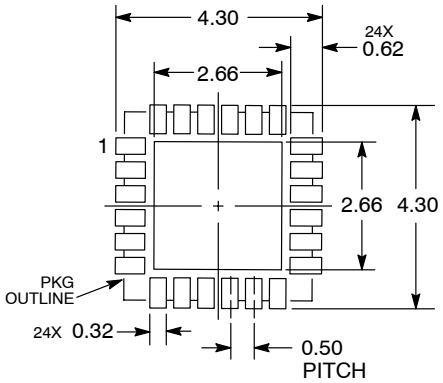



XXXXXX= Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

## RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON79518F** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **QFN24, 4X4, 0.5P** | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales