Hex Buffer

MC74VHC50, MC74VHCT50A

The MC74VHC50 and MC74VHCT50A are high speed CMOS quad Buffers fabricated with silicon gate CMOS technology. These achieve high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC50 inputs are compatible with standard CMOS levels while the MC74VHCT50A inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

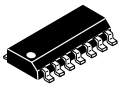
The MC74VHC50 and MC74VHCT50A internal circuits are composed of three stages, including a buffer output which provides high noise immunity and stable output. The input structures tolerate voltages up to 5.5 V, allowing the interface of 5 V systems to 3 V systems.

The MC74VHCT50A output structures provide protection when V_{CC} = 0 V. These output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

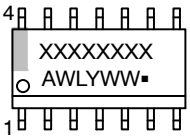
Features

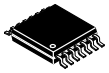
- High Speed: t_{PD} = 3.8 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25 °C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise: V_{OLP} = 0.8 V (Max)
- –Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable*
- These Devices are Pb-Free and are RoHS Compliant

MARKING DIAGRAMS

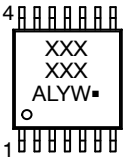


SOIC-14 NB
D SUFFIX
CASE 751A-03





TSSOP-14
DT SUFFIX
CASE 948G



XXXXXX	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ▪	= Pb-Free Package

FUNCTION TABLE

A Input	Y Output
L	L
H	H

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

© Semiconductor Components Industries, LLC, 2011

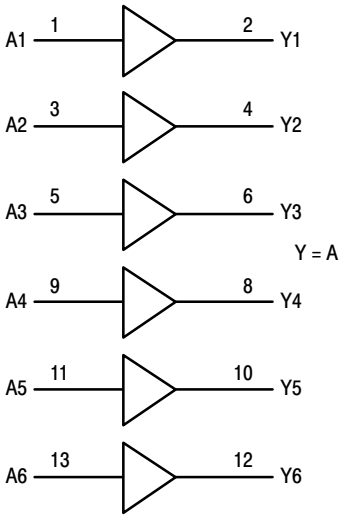


Figure 1. Logic Diagram

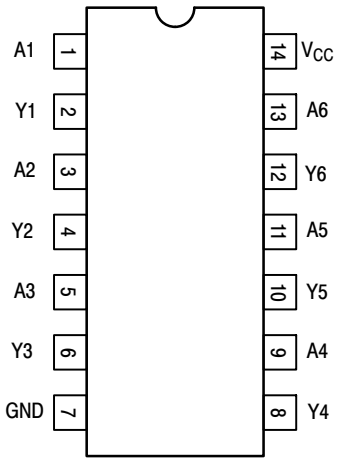


**Figure 2. Pinout:
14−Lead Packages
(Top View)**

Share Feedback
Your Opinion Matters

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_I	DC Input Voltage		−0.5 to +6.5	V
V_O	DC Output Voltage (**MC74VHC**)		−0.5 to V_{CC} + 0.5	V
	DC Output Voltage (**MC74VHCT**)	Active Mode (High or Low State) Tristate Mode (Note 1) Power-Off Mode (V_{CC} = 0 V)	−0.5 to V_{CC} + 0.5 −0.5 to +6.5 −0.5 to +6.5	
I_{IN}	DC Input Current, per Pin		±20	mA
I_{OUT}	DC Output Current, Per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±50	mA
I_{IK}	Input Clamp Current		−20	mA
I_{OK}	Output Clamp Current	MC74VHC MC74VHCT	±20 −20	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	SOIC-14 NB TSSOP-14	116 150	°C/W
P_D	Power Dissipation in Still Air at 25 °C	SOIC-14 NB TSSOP-14	1077 833	mW
MSL	Moisture Sensitivity		Level 1	–
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	–
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	> 2000 2000	V
$I_{LATCHUP}$	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

Share Feedback
Your Opinion Matters

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
MC74VHC					
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_I	DC Input Voltage (Note 5)		0	5.5	V
V_O	DC Output Voltage (Note 5)		0	V_{CC}	V
T_A	Operating Temperature		−55	+125	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 3.0 V to 3.6 V V_{CC} = 4.5 V to 5.5 V	0 0	100 20	ns/V
MC74VHCT					
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_I	DC Input Voltage (Note 5)		0	5.5	V
V_O	DC Output Voltage (Note 5)	Active Mode (High or Low State) Tristate Mode Power-Off Mode (V_{CC} = 0 V)	0 0 0	V_{CC} 5.5 5.5	V
T_A	Operating Temperature		−55	+125	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 4.5 V to 5.5 V	0	20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (MC74VHC50)

Symbol	Parameter	Test Conditions	V_{CC}	T_A = 25 °C			$T_A \le$ 85 °C		$T_A \le$ 125 °C		Unit
			(V)	Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	Minimum High-Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.0 3.15 3.85			1.5 2.0 3.15 3.85		1.5 2.0 3.15 3.85		V
V_{IL}	Maximum Low-Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OH} = −50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		V_{IN} = V_{IH} or V_{IL} I_{OH} = −4 mA I_{OH} = −8 mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V_{OL}	Maximum Low-Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50 μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL} I_{OL} = 4 mA I_{OL} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			2.0		20		40	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Share Feedback
Your Opinion Matters

AC ELECTRICAL CHARACTERISTICS (MC74VHC50)

Symbol	Parameter	Test Conditions	T_A = 25 °C			$T_A \le$ 85 °C		$T_A \le$ 125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Y	V_{CC} = 3.0 ± 0.3 V C_L = 15 pF		5.0	7.1		8.5		10.0	ns
		C_L = 50 pF		7.5	10.6		12.0		14.5	
		V_{CC} = 5.0 ± 0.5 V C_L = 15 pF		3.8	5.5		6.5		8.0	
		C_L = 50 pF		5.3	7.5		8.5		10.0	
C_{IN}	Maximum Input Capacitance			4	10		10		10	pF

		Typical @ 25 °C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 6)	18	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (MC74VHC50, C_L = 50 pF, V_{CC} = 5.0 V)

Symbol	Characteristic	T_A = 25 °C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.8	1.0	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−0.8	−1.0	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

Share Feedback
Your Opinion Matters

DC ELECTRICAL CHARACTERISTICS (MC74VHCT50A)

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25 °C Min	Typ	Max	$T_A \le$ 85 °C Min	Max	$T_A \le$ 125 °C Min	Max	Unit
V_{IH}	Minimum High-Level Input Voltage		3.0 4.5 5.5	1.4 2.0 2.0			1.4 2.0 2.0		1.4 2.0 2.0		V
V_{IL}	Maximum Low-Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50$ μA	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4$ mA $I_{OH} = -8$ mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V_{OL}	Maximum Low-Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50$ μA	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4$ mA $I_{OL} = 8$ mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5$ V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μA
I_{CCT}	Quiescent Supply Current	Input: $V_{IN} = 3.4$ V	5.5			1.35		1.50		1.65	mA
I_{OFF}	Output Leakage Current	$V_{OUT} = 5.5$ V	0.0			0.5		5.0		10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (MC74VHCT50A)

Symbol	Parameter	Test Conditions	T_A = 25 °C Min	Typ	Max	$T_A \le$ 85 °C Min	Max	$T_A \le$ 125 °C Min	Max	Unit
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input A to Y	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $C_L = 50$ pF		5.5 8.0	7.9 11.4	1.0 1.0	9.5 13.0			ns
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $C_L = 50$ pF		6.2 7.0	7.5 8.5		8.5 9.5		9.5 10.5	
C_{IN}	Maximum Input Capacitance			5	10		10		10	pF

		Typical @ 25 °C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 6)	18	pF

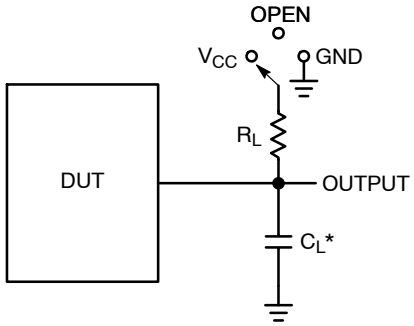
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

Share Feedback
Your Opinion Matters

NOISE CHARACTERISTICS (C_L = 50 pF, V_{CC} = 5.0 V)

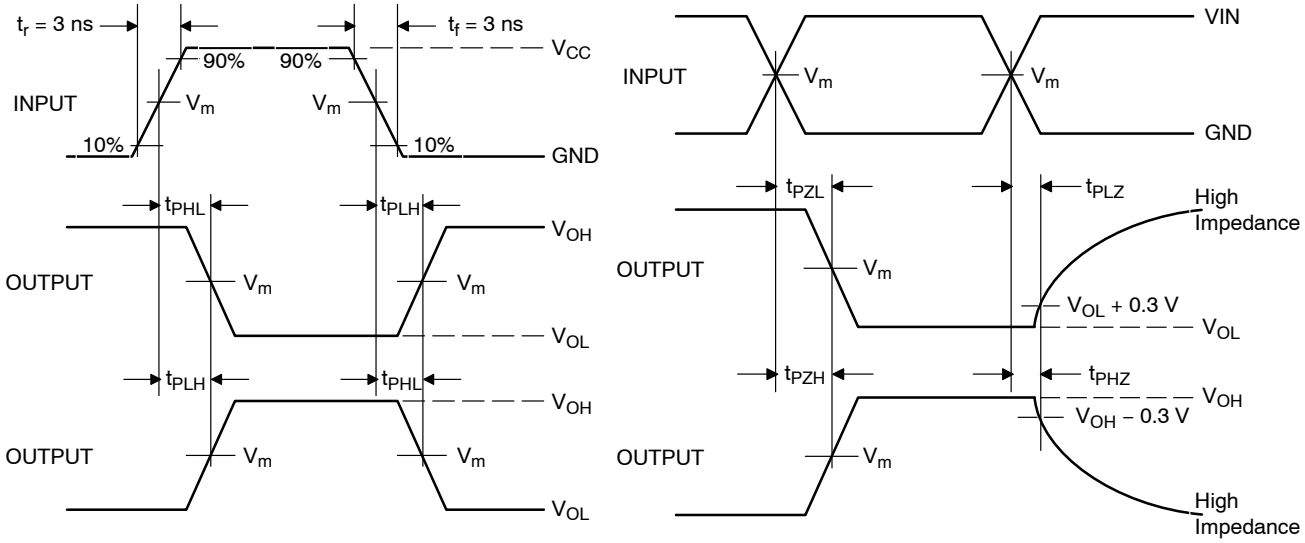
Symbol	Characteristic	T_A = 25 °C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.8	1.0	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−0.8	−1.0	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V



*C_L Includes probe and jig capacitance

Test	Switch Position	C_L	R_L
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table	1 kΩ
t_{PLZ} / t_{PZL}	V_{CC}		
t_{PHZ} / t_{PZH}	GND		

Figure 3. Test Circuit



Device	V_{IN}, V	V_m, V
MC74VHC50	V_{CC}	50% x V_{CC}
MC74VHCT50A	3 V	1.5 V

Figure 4. Switching Waveforms

Share Feedback
Your Opinion Matters

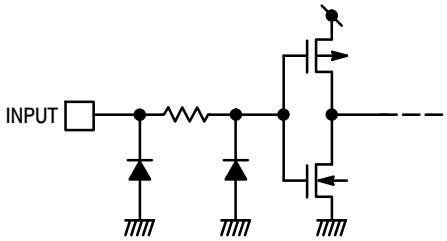


Figure 5. Input Equivalent Circuit

ORDERING INFORMATION

Device	Package	Marking	Shipping†
MC74VHC50DG	SOIC-14 NB	VHC50G	55 Units / Rail
MC74VHC50DR2G	SOIC-14 NB	VHC50G	2500 / Tape & Reel
MC74VHC50DTR2G	TSSOP-14	VHC 50	2500 / Tape & Reel
MC74VHC50DTR2G-Q*	TSSOP-14	VHC 50	2500 / Tape & Reel
MC74VHCT50ADR2G	SOIC-14 NB	VHCT50AG	2500 / Tape & Reel
MC74VHCT50ADTR2G	TSSOP-14	VHCT 50A	2500 / Tape & Reel
MC74VHCT50ADTR2G-Q*	TSSOP-14	VHCT 50A	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*–Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

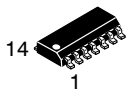
Share Feedback
Your Opinion Matters

REVISION HISTORY

Revision	Description of Changes	Date
9	Edits to the package name labels	10/12/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

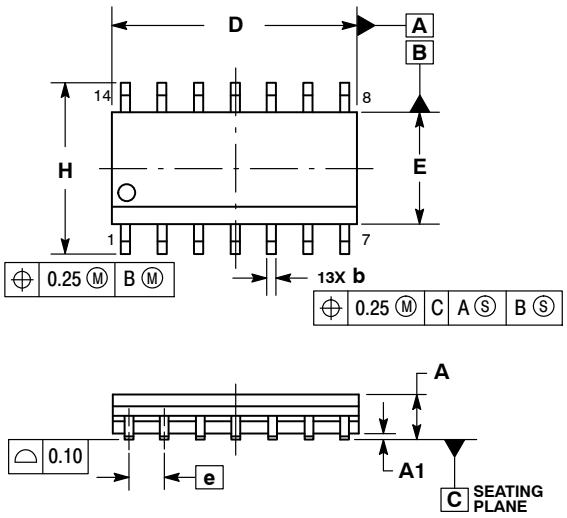
Share Feedback
Your Opinion Matters

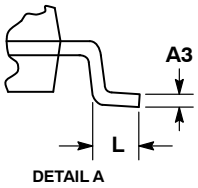


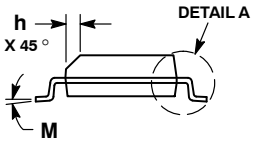
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



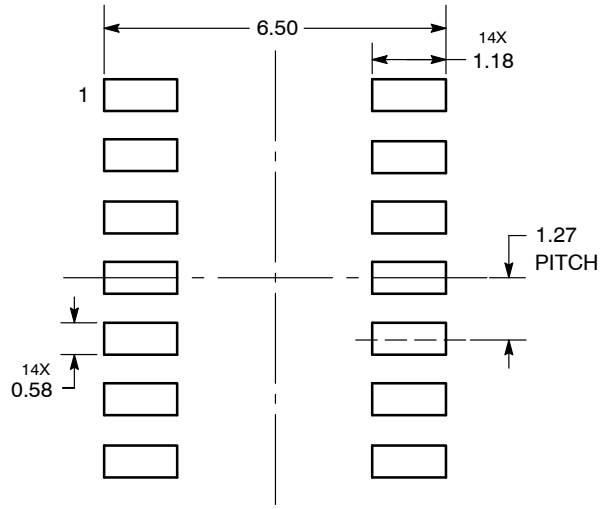




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

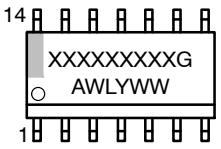
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42565B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOIC−14 NB**		**PAGE 1 OF 2**

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

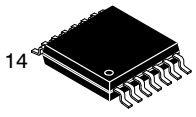
STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

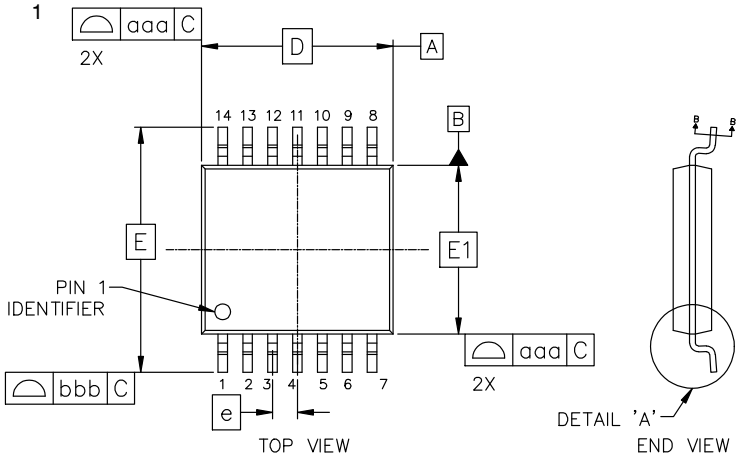
onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

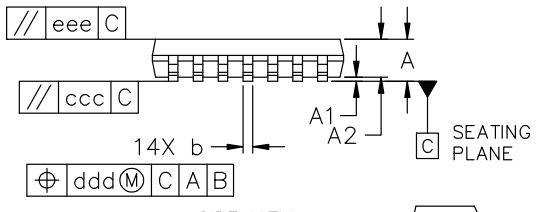
© Semiconductor Components Industries, LLC, 2019

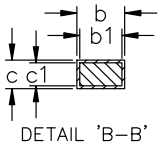


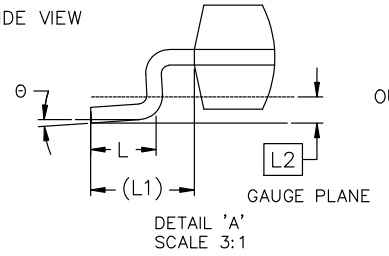
TSSOP−14 5.00x4.40x0.95, 0.65P
CASE 948G
ISSUE D

DATE 30 JUN 2026

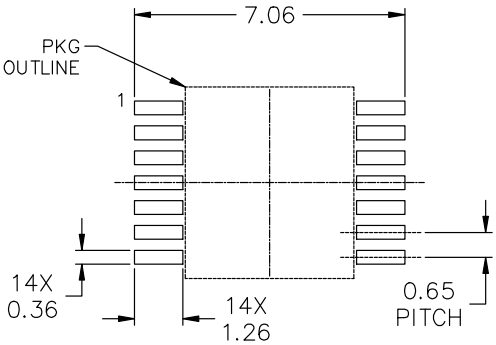








MILLIMETERS			
DIM	MIN	NOM	MAX
A	−−−	−−−	1.20
A1	0.05	0.10	0.15
A2	0.85	0.95	1.05
b	0.19	0.25	0.30
b1	0.19	0.22	0.25
c	0.09	0.15	0.20
c1	0.09	0.12	0.16
D	5.00 BSC		
E	6.40 BSC		
E1	4.40 BSC		
e	0.65 BSC		
L	0.50	0.63	0.75
L1	1.00 REF		
L2	0.25 BSC		
θ	0°	4°	8°
TOLERANCE FORM & POSITION			
aaa	0.10		
bbb	0.15		
ccc	0.08		
ddd	0.10		
eee	0.10		

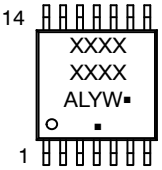


RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D DOES NOT INCLIDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASH70246A**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TSSOP−14 5.00x4.40x0.95, 0.65P**	**PAGE 1 OF 1**

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales