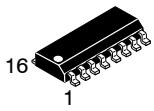
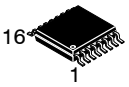
8-Bit Addressable Latch 1-of-8 Decoder

High-Performance Silicon-Gate CMOS

MC74HC259A, MC74HCT259A



SOIC−16
D SUFFIX
CASE 751B



TSSOP−16
DT SUFFIX
CASE 948F



QFN16
MN SUFFIX
CASE 485AW

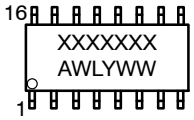
The MC74HC259A/MC74HCT259A is identical in pinout to the LS259. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. The MC74HCT259A inputs are compatible with standard CMOS and LSTTL outputs.

The device has four modes of operation as shown in the mode selection table. In the addressable latch mode, the data on Data In is written into the addressed latch. The addressed latch follows the data input with all non−addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs. In the one−of−eight decoding or demultiplexing mode, the addressed output follows the state of Data In with all other outputs in the LOW state. In the Reset mode all outputs are LOW and unaffected by the address and data inputs. When operating the device as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

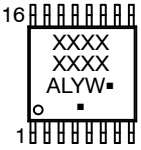
Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V (HC), 4.5 to 5.5 V (HCT)
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

MARKING DIAGRAMS



SOIC−16



TSSOP−16

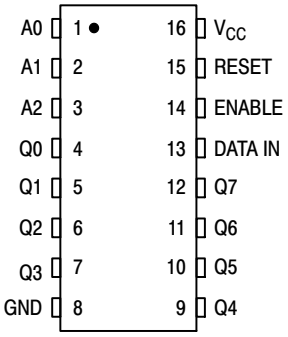


QFN16

XXXXXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



MODE SELECTION TABLE

Enable	Reset	Mode
L	H	Addressable Latch
H	H	Memory
L	L	8−Line Demultiplexer
H	L	Reset

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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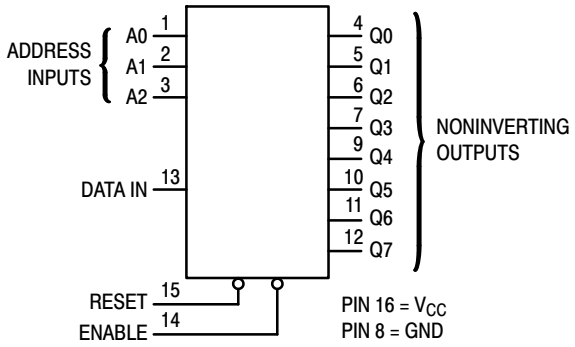

Figure 1. Logic Diagram

LATCH SELECTION TABLE

Address Inputs			
A_2	A_1	A_0	Latch Addressed
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to V_{CC}+0.5	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC}+0.5	V
I_{IN}	DC Input Diode Current, per Pin		±20	mA
I_{OUT}	DC Input Diode Current, Per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±50	mA
I_{IK}	Input Clamp Current (V_{IN} < 0 or V_{IN} > V_{CC})		±20	mA
I_{OK}	Output Clamp Current (V_{OUT} < 0 or V_{OUT} > V_{CC})		±20	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 1)	SOIC−16 QFN16 TSSOP−16	126 118 159	°C/W
P_D	Power Dissipation in Still Air at 25°C	SOIC−16 QFN16 TSSOP−16	995 1062 787	mW
MSL	Moisture Sensitivity		Level 1	−
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	−
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	2000 N/A	V
$I_{LATCHUP}$	Latchup Performance (Note 3)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76mm−by−114mm, 2−ounce copper trace no air flow per JESD51−7.
2. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.
3. Tested to EIA/JESD78 Class II.

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RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
MC74HC					
V_{CC}	DC Supply Voltage		2.0	6.0	V
V_{in}, V_{out}	DC Input, Output Voltage (Note 4)		0	V_{CC}	V
T_A	Operating Free−Air Temperature		−55	+125	°C
t_r, t_f	Input Rise or Fall Time	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns
MC74HCT					
V_{CC}	DC Supply Voltage		4.5	5.5	V
V_{in}, V_{out}	DC Input, Output Voltage (Note 4)		0	V_{CC}	V
T_A	Operating Free−Air Temperature		−55	+125	°C
t_r, t_f	Input Rise or Fall Time		0	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (MC74HC259A)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				− 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High−Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low−Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.80	0.5 0.9 1.35 1.80	0.5 0.9 1.35 1.80	V
V_{OH}	Minimum High−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 2.4$ mA $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 2.4$ mA $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	6.0	4	40	160	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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AC ELECTRICAL CHARACTERISTICS (MC74HC259A)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			− 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Data to Output (Figures 2, 3)	2.0 3.0 4.5 6.0	125 45 32 25	160 60 32 28	175 70 42 33	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Address Select to Output (Figures 2, 4)	2.0 3.0 4.5 6.0	150 60 32 28	175 70 40 30	200 80 45 35	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Enable to Output (Figures 2, 5)	2.0 3.0 4.5 6.0	150 60 32 28	175 70 40 30	200 80 45 35	ns
t_{PHL}	Maximum Propagation Delay, Reset to Output (Figures 2, 6)	2.0 3.0 4.5 6.0	110 36 22 19	125 45 26 23	160 60 32 28	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 2, 3)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance	–	10	10	10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)	30	pF

TIMING REQUIREMENTS (MC74HC259A)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			− 55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Address or Data to Enable (Figure 7)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_h	Minimum Hold Time, Enable to Address or Data (Figure 7)	2.0 3.0 4.5 6.0	1 1 1 1	1 1 1 1	1 1 1 1	ns
t_w	Minimum Pulse Width, Reset or Enable (Figure 5, 6)	2.0 3.0 4.5 6.0	70 27 15 13	90 32 19 16	100 36 22 19	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 3)	2.0 3.0 4.5 6.0	1000 600 500 400	1000 600 500 400	1000 600 500 400	ns

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DC ELECTRICAL CHARACTERISTICS (MC74HCT259A)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20$ μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20$ μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20$ μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 5.2$ mA	4.5	3.98	3.84	3.70	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20$ μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 5.2$ mA	4.5	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	5.5	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	5.5	4	40	160	μA

				≥ –55°C	25 to 125°C	
ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4V, Any One Input V_{in} = V_{CC} or GND, Other Inputs I_{out} = 0μA	5.5	2.9	2.4	mA

AC ELECTRICAL CHARACTERISTICS (MC74HCT259A)

Symbol	Parameter	Guaranteed Limit			Unit
		–55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Data to Output (Figures 2, 3)	32	32	42	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Address Select to Output (Figures 2, 4)	32	40	45	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Enable to Output (Figures 2, 5)	32	40	45	ns
t_{PHL}	Maximum Propagation Delay, Reset to Output (Figures 2, 6)	22	26	32	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 2, 3)	15	19	22	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)	30	pF

TIMING REQUIREMENTS (MC74HCT259A)

Symbol	Parameter	Guaranteed Limit			Unit
		–55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Address or Data to Enable (Figure 7)	15	19	22	ns
t_h	Minimum Hold Time, Enable to Address or Data (Figure 7)	1	1	1	ns
t_w	Minimum Pulse Width, Reset or Enable (Figure 5 or 6)	15	19	22	ns

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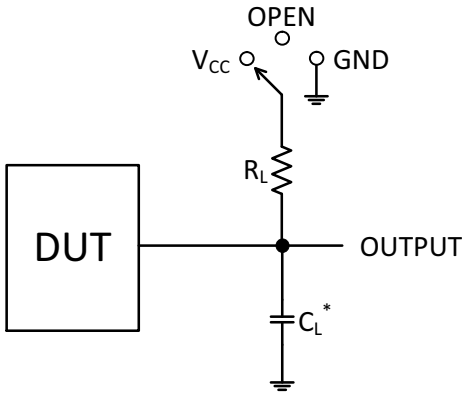
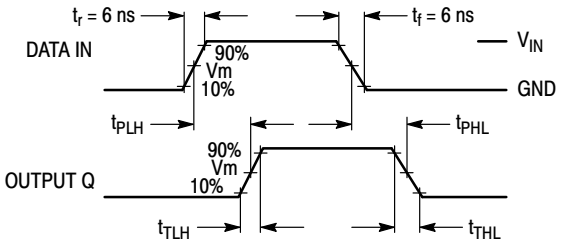


*C_L Includes probe and jig capacitance

Test	Switch Position	C_L	R_L
t_{PLH} / t_{PHL}	Open	50 pF	1 kΩ
t_{PLZ} / t_{PZL}	V_{CC}		
t_{PHZ} / t_{PZH}	GND		

Figure 2. Test Circuit

SWITCHING WAVEFORMS



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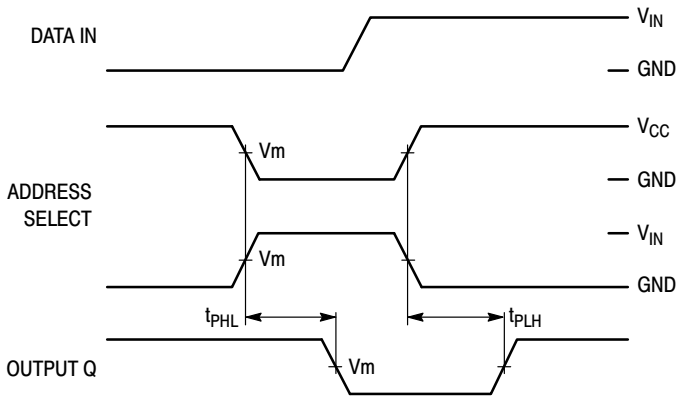

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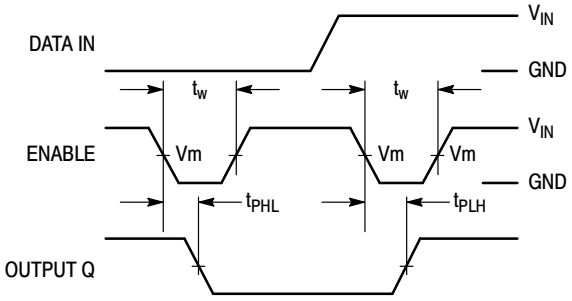

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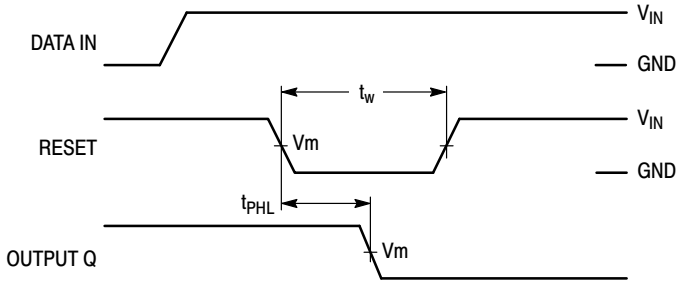

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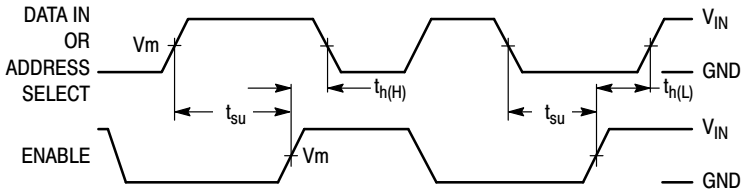

Figure 7.

Device	V_{IN}, V	V_m, V
MC74HC259A	V_{CC}	50% x V_{CC}
MC74HCT259A	3 V	1.3 V

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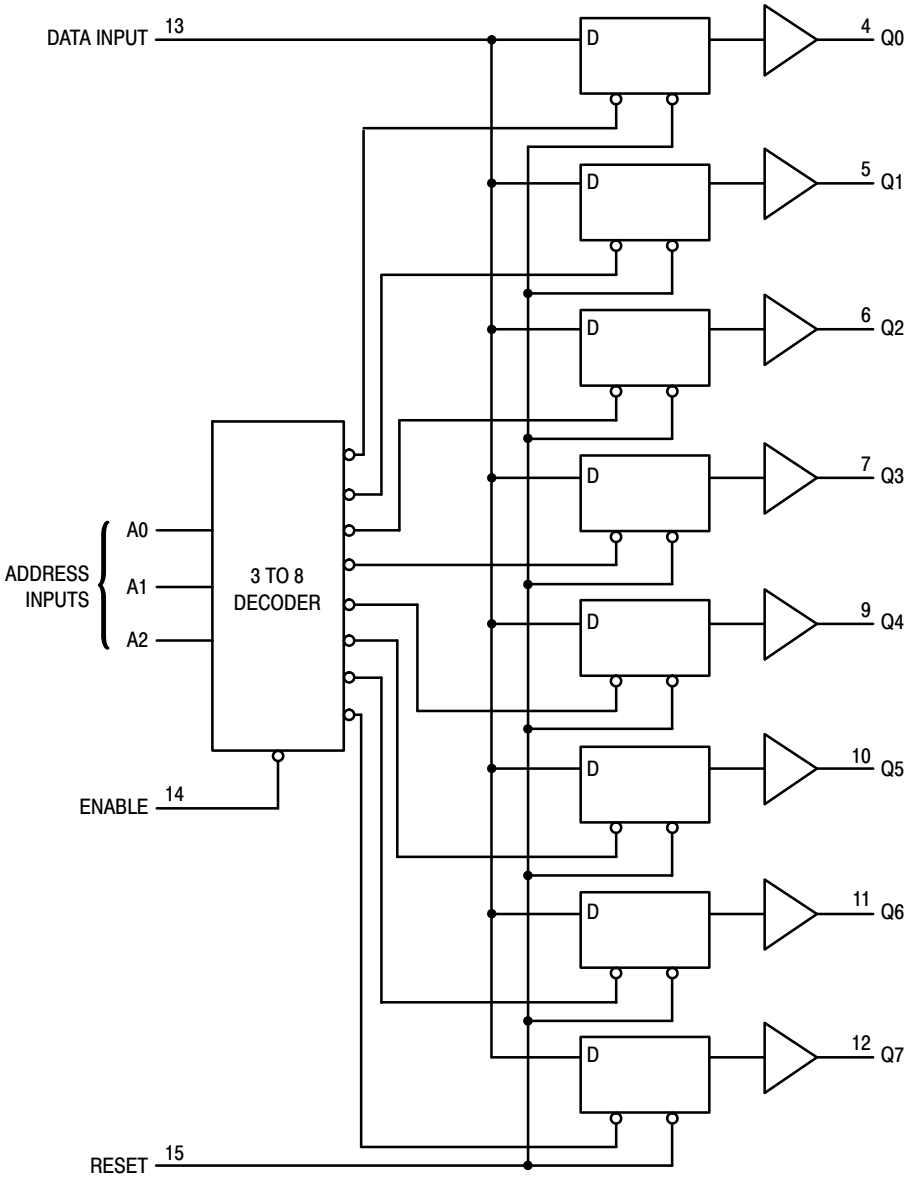

Figure 8. Expanded Logic Diagram

ORDERING INFORMATION

Device	Marking	Package	Shipping†
MC74HC259ADR2G	HC259AG	SOIC−16	2500 Units / Tape & Reel
MC74HC259ADR2G−Q*	HC259AG	SOIC−16	2500 Units / Tape & Reel
MC74HC259ADTR2G	HC 259A	TSSOP−16	2500 Units / Tape & Reel
MC74HC259ADTR2G−Q*	HC 259A	TSSOP−16	2500 Units / Tape & Reel
MC74HCT259ADR2G	HCT259AG	SOIC−16	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

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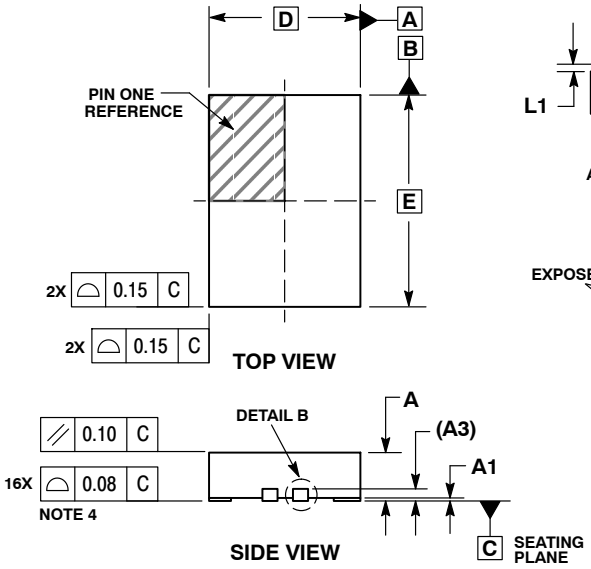
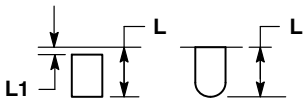
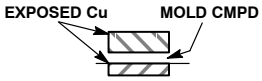
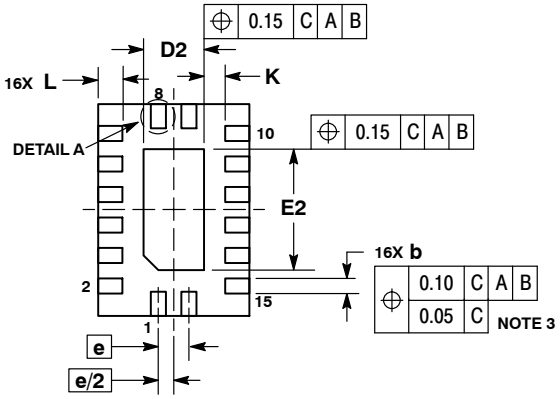
PACKAGE DIMENSIONS

QFN16, 2.5x3.5, 0.5P
CASE 485AW
ISSUE O





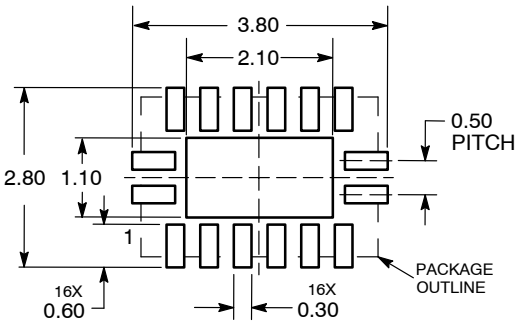




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.50 BSC	
D2	0.85	1.15
E	3.50 BSC	
E2	1.85	2.15
e	0.50 BSC	
K	0.20	---
L	0.35	0.45
L1	---	0.15

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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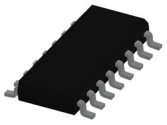
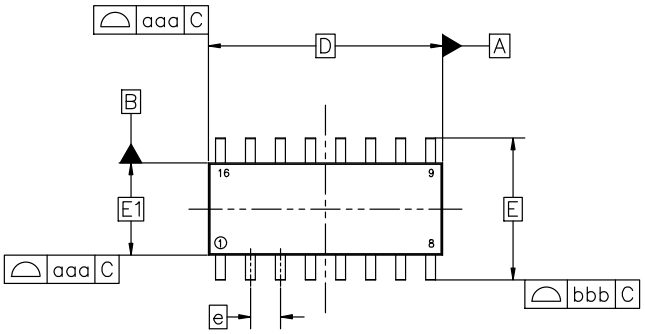


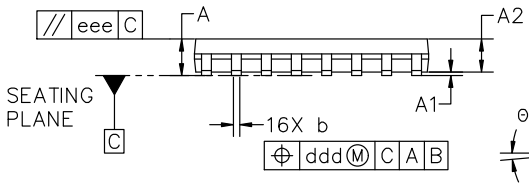
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

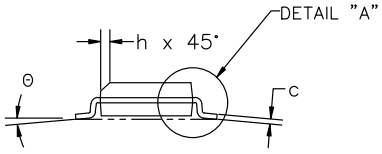
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



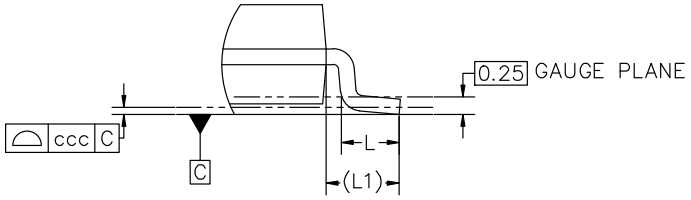
TOP VIEW



SIDE VIEW

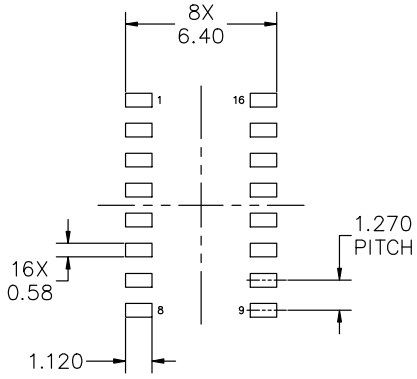


END VIEW



DETAIL "A"
Scale 3:1

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

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DESCRIPTION:	**SOIC−16 9.90X3.90X1.37 1.27P**		**PAGE 1 OF 2**

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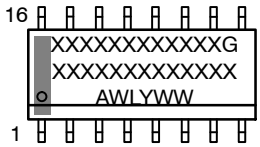
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN	
1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN	
1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN	
1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN	
1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

PIN	
1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

PIN	
1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

PIN	
1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH

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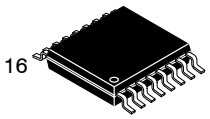
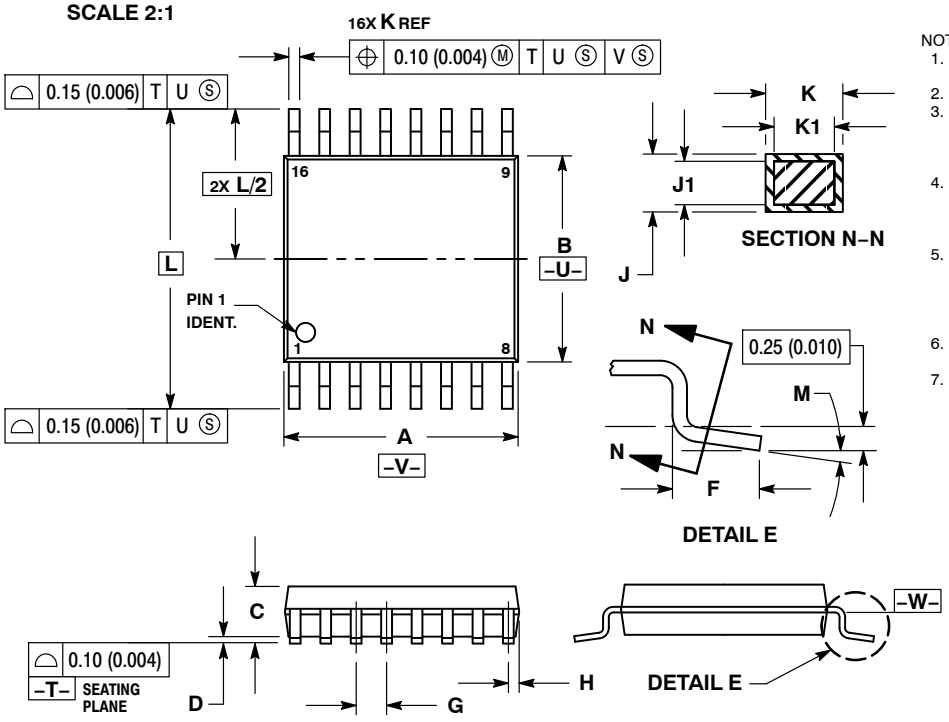


SCALE 2:1

TSSOP−16 WB
CASE 948F
ISSUE B

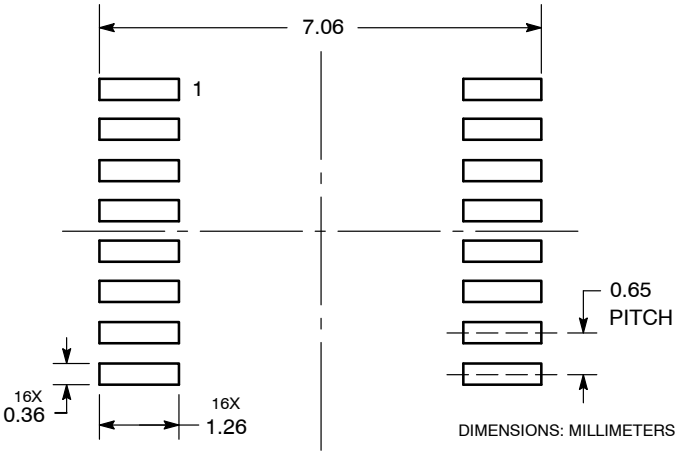
DATE 19 OCT 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

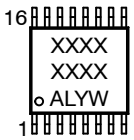
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP−16**		**PAGE 1 OF 1**

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