

Motion SPM[®] 5 Series

FSB50325A, FSB50325AT, FSB50325AS

General Description

The FSB50325A/AT/AS is an advanced Motion SPM 5 module providing a fully-featured, high-performance inverter output stage for AC Induction, BLDC and PMSM motors. These modules integrate optimized gate drive of the built-in MOSFETs (FRFET[®] technology) to minimize EMI and losses, while also providing multiple on-module protection features including under-voltage lockouts and thermal monitoring. The built-in high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's internal MOSFETs. Separate open-source MOSFET terminals are available for each phase to support the widest variety of control algorithms.

Features

- UL Certified No. E209204 (UL1557)
- 250 V $R_{DS(on)} = 1.7 \Omega$ (Max) FRFET MOSFET 3-Phase Inverter with Gate Drivers and Protection
- Built-in Bootstrap Diodes Simplify PCB Layout
- Separate Open-Source Pins from Low-Side MOSFETs for Three-Phase Current-Sensing
- Active-HIGH Interface, Works with 3.3 / 5 V Logic, Schmitt-trigger Input
- Optimized for Low Electromagnetic Interference
- HVIC Temperature-Sensing Built-in for Temperature Monitoring
- HVIC for Gate Driving and Under-Voltage Protection
- Isolation Rating: 1500 Vrms / 1 min.
- Moisture Sensitive Level (MSL) 3 – FSB50325AS
- These Devices are Pb-Free and are RoHS Compliant

Applications

- 3-Phase Inverter Driver for Small Power AC Motor Drives

Related Source

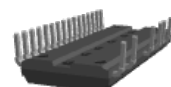
- RD-FSB50450A – Reference Design for Motion SPM 5 Series Ver.2
- [AN-9082](#) – Motion SPM5 Series Thermal Performance by Contact Pressure
- [AN-9080](#) – User's Guide for Motion SPM 5 Series V2



ON Semiconductor[®]

www.onsemi.com

**SPM5E – 023 / 23LD,
PDD STD, FULL PACK,
DIP TYPE
CASE MODEJ**



**SPM5G – 023 / 23LD,
PDD STD, FULL PACK,
DOUBLE DIP TYPE (BSH)
CASE MODEL**



**SPM5H – 023 / 23LD,
PDD STD, SPM23 – BD
(Ver1.5) SMD TYPE
CASE MODEM**



MARKING DIAGRAM

\$Y
FSB50325x
&Z&K&E&E&E&3

\$Y = ON Semiconductor Logo
FSB50325x = Specific Device Code
(x = A, AT, AS)
&Z = Assembly Plant Code
&K = 2-Digits Lot Run Traceability Code
&E = Designate Space
&3 = 3-Digits Data Code Format

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FSB50325A, FSB50325AT, FSB50325AS

ORDERING INFORMATION

Device	Device Marking	Package	Shipping†
FSB50325A	FSB50325A	SPM5E-023 (Pb-Free)	270 / Tube
FSB50325AT	FSB50325AT	SPM5G-023 (Pb-Free)	180 / Tube
FSB50325AS	FSB50325AS	SPM5H-023 (Pb-Free)	450 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Rating	Unit
--------	-----------	-------------	--------	------

INVERTER PART (each MOSFET unless otherwise specified.)

V_{DSS}	Drain-Source Voltage of Each MOSFET		250	V
$*I_{D25}$	Each MOSFET Drain Current, Continuous	$T_C = 25^\circ\text{C}$	1.7	A
$*I_{D80}$	Each MOSFET Drain Current, Continuous	$T_C = 80^\circ\text{C}$	1.3	A
$*I_{DP}$	Each MOSFET Drain Current, Peak	$T_C = 25^\circ\text{C}$, $PW < 100\text{ ms}$	4.4	A
$*I_{DRMS}$	Each MOSFET Drain Current, Rms	$T_C = 80^\circ\text{C}$, $F_{PWM} < 20\text{ kHz}$	0.9	A_{rms}
$*P_D$	Maximum Power Dissipation	$T_C = 25^\circ\text{C}$, For Each MOSFET	12.3	W

CONTROL PART (each HVIC unless otherwise specified.)

V_{CC}	Control Supply Voltage	Applied Between V_{CC} and COM	20	V
V_{BS}	High-side Bias Voltage	Applied Between V_B and V_S	20	V
V_{IN}	Input Signal Voltage	Applied Between IN and COM	$-0.3 \sim V_{CC} + 0.3$	V

BOOTSTRAP DIODE PART (each bootstrap diode unless otherwise specified.)

V_{RRMB}	Maximum Repetitive Reverse Voltage		250	V
$*I_{FB}$	Forward Current	$T_C = 25^\circ\text{C}$	0.5	A
$*I_{FPB}$	Forward Current (Peak)	$T_C = 25^\circ\text{C}$, Under 1 ms Pulse Width	1.5	A

THERMAL RESISTANCE

$R_{\theta JC}$	Junction to Case Thermal Resistance	Each MOSFET under Inverter Operating Condition (Note 1)	10.2	$^\circ\text{C/W}$
-----------------	-------------------------------------	---	------	--------------------

TOTAL SYSTEM

T_J	Operating Junction Temperature		$-40 \sim 150$	$^\circ\text{C}$
T_{STG}	Storage Temperature		$-40 \sim 125$	$^\circ\text{C}$
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, 1 Minute, Connect Pins to Heat Sink Plate	1500	V_{rms}

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- For the measurement point of case temperature T_C , please refer to Figure 4.
- Marking “*” is calculation value or design factor.

FSB50325A, FSB50325AT, FSB50325AS

PIN DESCRIPTION

Pin No.	Pin Name	Description
1	COM	IC Common Supply Ground
2	$V_{B(U)}$	Bias Voltage for U-Phase High-Side MOSFET Driving
3	$V_{CC(U)}$	Bias Voltage for U-Phase IC and Low-Side MOSFET Driving
4	$IN_{(UH)}$	Signal Input for U-Phase High-Side
5	$IN_{(UL)}$	Signal Input for U-Phase Low-Side
6	N.C	No Connection
7	$V_{B(V)}$	Bias Voltage for V-Phase High Side MOSFET Driving
8	$V_{CC(V)}$	Bias Voltage for V-Phase IC and Low Side MOSFET Driving
9	$IN_{(VH)}$	Signal Input for V-Phase High-Side
10	$IN_{(VL)}$	Signal Input for V-Phase Low-Side
11	V_{TS}	Output for HVIC Temperature Sensing
12	$V_{B(W)}$	Bias Voltage for W-Phase High-Side MOSFET Driving
13	$V_{CC(W)}$	Bias Voltage for W-Phase IC and Low-Side MOSFET Driving
14	$IN_{(WH)}$	Signal Input for W-Phase High-Side
15	$IN_{(WL)}$	Signal Input for W-Phase Low-Side
16	N.C	No Connection
17	P	Positive DC-Link Input
18	U, $V_{S(U)}$	Output for U-Phase & Bias Voltage Ground for High-Side MOSFET Driving
19	N_U	Negative DC-Link Input for U-Phase
20	N_V	Negative DC-Link Input for V-Phase
21	V, $V_{S(V)}$	Output for V-Phase & Bias Voltage Ground for High-Side MOSFET Driving
22	N_W	Negative DC-Link Input for W-Phase
23	W, $V_{S(W)}$	Output for W Phase & Bias Voltage Ground for High-Side MOSFET Driving

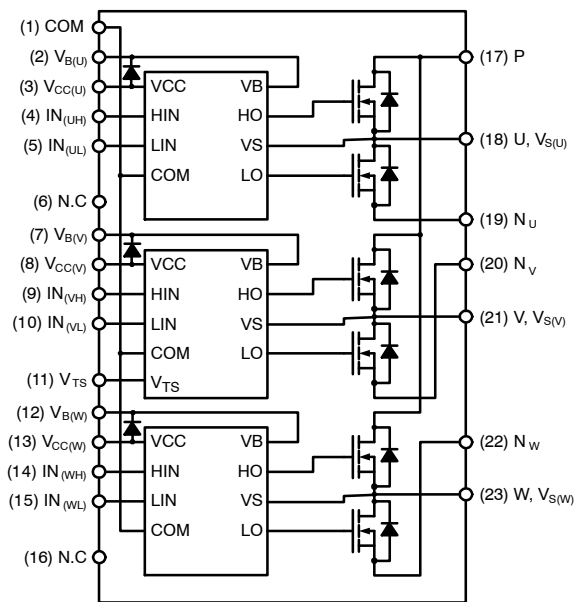


Figure 1. Pin Configuration and Internal Block Diagram (Bottom View)

NOTE:

- Source terminal of each low-side MOSFET is not connected to supply ground or bias voltage ground inside Motion SPM 5 product. External connections should be made as indicated in Figure 3.

FSB50325A, FSB50325AT, FSB50325AS

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, $V_{CC} = V_{BS} = 15\text{ V}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
INVERTER PART (each MOSFET unless otherwise specified.)						
BV_{DSS}	Drain – Source Breakdown Voltage	$V_{IN} = 0\text{ V}$, $I_D = 1\text{ mA}$ (Note 4)	250	–	–	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{IN} = 0\text{ V}$, $V_{DS} = 250\text{ V}$	–	–	1	mA
$R_{DS(on)}$	Static Drain – Source Turn-On Resistance	$V_{CC} = V_{BS} = 15\text{ V}$, $V_{IN} = 5\text{ V}$, $I_D = 1.0\text{ A}$	–	1.1	1.7	Ω
V_{SD}	Drain – Source Diode Forward Voltage	$V_{CC} = V_{BS} = 15\text{ V}$, $V_{IN} = 0\text{ V}$, $I_D = -1.0\text{ A}$	–	–	1.2	V
t_{ON}	Switching Times	$V_{PN} = 150\text{ V}$, $V_{CC} = V_{BS} = 15\text{ V}$, $I_D = 1.0\text{ A}$ $V_{IN} = 0\text{ V}$ e 5 V , Inductive Load $L = 3\text{ mH}$ High- and Low-Side MOSFET Switching (Note 5)	–	810	–	ns
t_{OFF}			–	600	–	ns
t_{rr}			–	140	–	ns
E_{ON}			–	40	–	mJ
E_{OFF}			–	10	–	mJ
RBSOA	Reverse Bias Safe Operating Area	$V_{PN} = 200\text{ V}$, $V_{CC} = V_{BS} = 15\text{ V}$, $I_D = I_{DP}$ $V_{DS} = BV_{DSS}$, $T_J = 150^\circ\text{C}$ High- and Low-Side MOSFET Switching (Note 6)	Full Square			

CONTROL PART (each HVIC unless otherwise specified.)

I_{QCC}	Quiescent V_{CC} Current	$V_{CC} = 15\text{ V}$, $V_{IN} = 0\text{ V}$	Applied Between V_{CC} and COM	–	–	200	A
I_{QBS}	Quiescent V_{BS} Current	$V_{BS} = 15\text{ V}$, $V_{IN} = 0\text{ V}$	Applied Between $V_{B(U)} - U$, $V_{B(V)} - V$, $V_{B(W)} - W$	–	–	100	μA
U_{VCCD}	Low-Side Under-Voltage Protection (Figure 8)	V_{CC} Under-Voltage Protection Detection Level		7.4	8.0	9.4	V
U_{VCCR}		V_{CC} Under-Voltage Protection Reset Level		8.0	8.9	9.8	V
U_{VBSD}	High-Side Under-Voltage Protection (Figure 9)	V_{BS} Under-Voltage Protection Detection Level		7.4	8.0	9.4	V
$U_{VB SR}$		V_{BS} Under-Voltage Protection Reset Level		8.0	8.9	9.8	V
V_{TS}	HVIC Temperature Sensing Voltage Output	$V_{CC} = 15\text{ V}$, $T_{HVIC} = 25^\circ\text{C}$ (Note 7)		600	790	980	mV
V_{IH}	ON Threshold Voltage	Logic HIGH Level	Applied between IN and COM	–	–	2.9	V
V_{IL}	OFF Threshold Voltage	Logic LOW Level		0.8	–	–	V

BOOTSTRAP DIODE PART (each bootstrap diode unless otherwise specified.)

V_{FB}	Forward Voltage	$I_F = 0.1\text{ A}$, $T_C = 25^\circ\text{C}$ (Note 8)	–	2.5	–	V
$trrB$	Reverse Recovery Time	$I_F = 0.1\text{ A}$, $T_C = 25^\circ\text{C}$	–	80	–	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- BV_{DSS} is the absolute maximum voltage rating between drain and source terminal of each MOSFET inside Motion SPM 5 product. V_{PN} should be sufficiently less than this value considering the effect of the stray inductance so that V_{PN} should not exceed BV_{DSS} in any case.
- t_{ON} and t_{OFF} include the propagation delay of the internal drive IC. Listed values are measured at the laboratory test condition, and they can be different according to the field applications due to the effect of different printed circuit boards and wirings. Please see Figure 6 for the switching time definition with the switching test circuit of Figure 7.
- The peak current and voltage of each MOSFET during the switching operation should be included in the Safe Operating Area (SOA). Please see Figure 7 for the RBSOA test circuit that is same as the switching test circuit.
- V_{TS} is only for sensing-temperature of module and cannot shutdown MOSFETs automatically.
- Built-in bootstrap diode includes around $15\ \Omega$ resistance characteristic. Please refer to Figure 2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PN}	Supply Voltage	Applied Between P and N		150	200	V
V_{CC}	Control Supply Voltage	Applied Between V_{CC} and COM	13.5	15.0	16.5	V
V_{BS}	High-Side Bias Voltage	Applied Between V_B and V_S	13.5	15.0	16.5	V
$V_{IN(ON)}$	Input ON Threshold Voltage	Applied Between IN and COM	3.0		V_{CC}	V
$V_{IN(OFF)}$	Input OFF Threshold Voltage		0		0.6	V
t_{dead}	Blanking Time for Preventing Arm-Short	$V_{CC} = V_{BS} = 13.5 \sim 16.5$ V, $T_J \leq 150^\circ\text{C}$	1.0			μs
f_{PWM}	PWM Switching Frequency	$T_J \leq 150^\circ\text{C}$		15		kHz

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

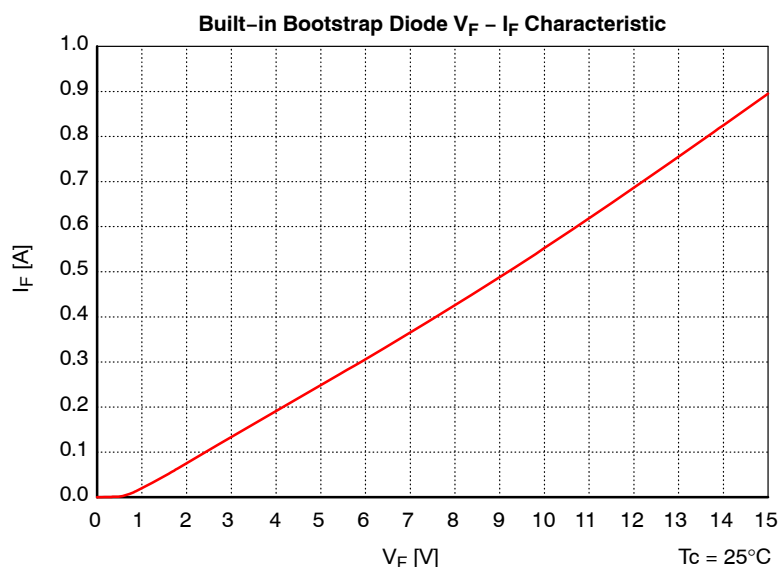


Figure 2. Built-in Bootstrap Diode Characteristics (Typical)

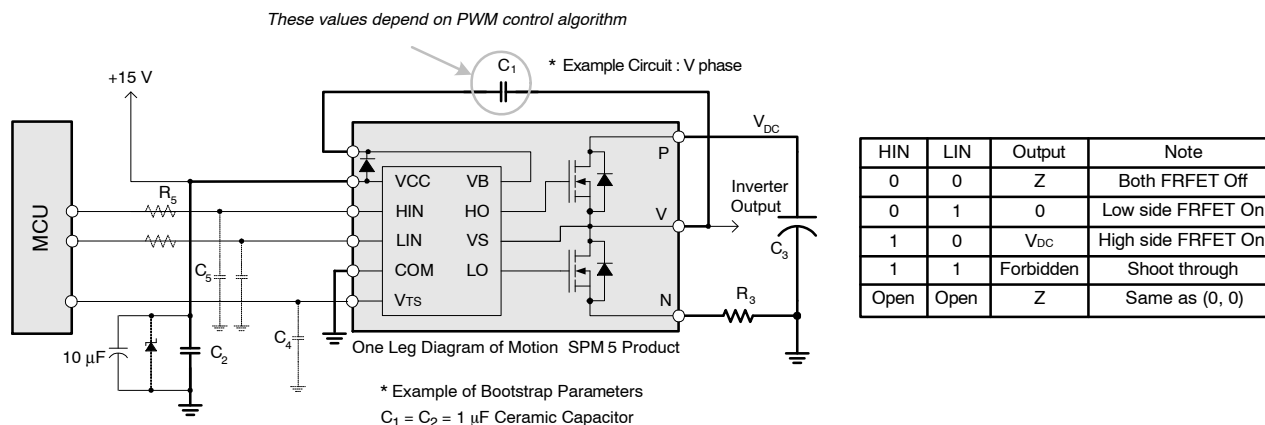


Figure 3. Recommended MCU Interface and Bootstrap Circuit with Parameters

NOTES:

- Parameters for bootstrap circuit elements are dependent on PWM algorithm. For 15 kHz of switching frequency, typical example of parameters is shown above.
- RC-coupling (R_5 and C_5) and C_4 at each input of Motion SPM 5 product and MCU (Indicated as Dotted Lines) may be used to prevent improper signal due to surge-noise.
- Bold lines should be short and thick in PCB pattern to have small stray inductance of circuit, which results in the reduction of surge-voltage. Bypass capacitors such as C_1 , C_2 and C_3 should have good high-frequency characteristics to absorb high-frequency ripple-current.

FSB50325A, FSB50325AT, FSB50325AS

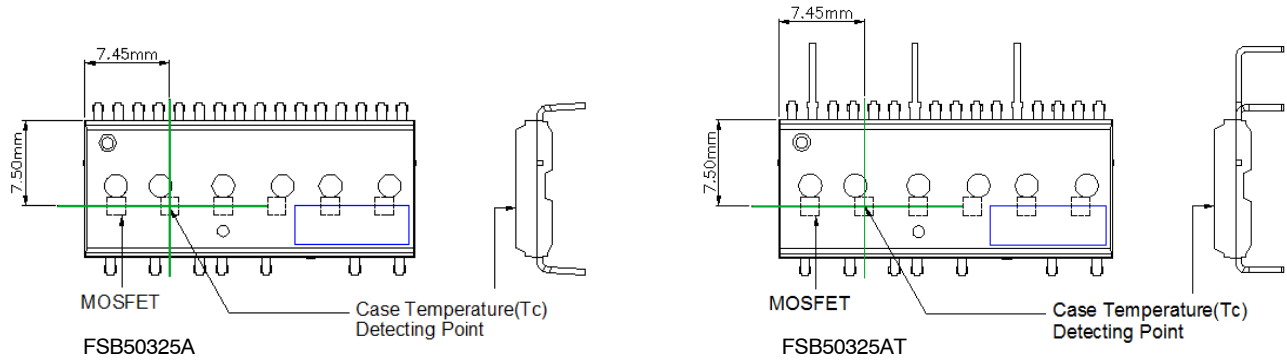


Figure 4. Case Temperature Measurement

NOTE:

12. Attach the thermocouple on top of the heat-sink of SPM 5 package (between SPM 5 package and heatsink if applied) to get the correct temperature measurement.

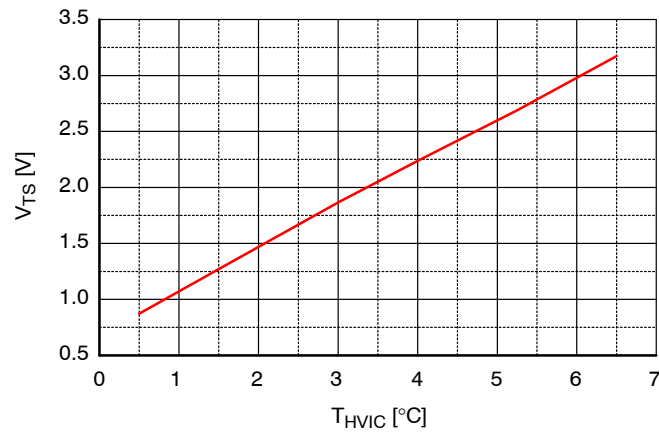


Figure 5. Temperature Profile of V_{TS} (Typical)

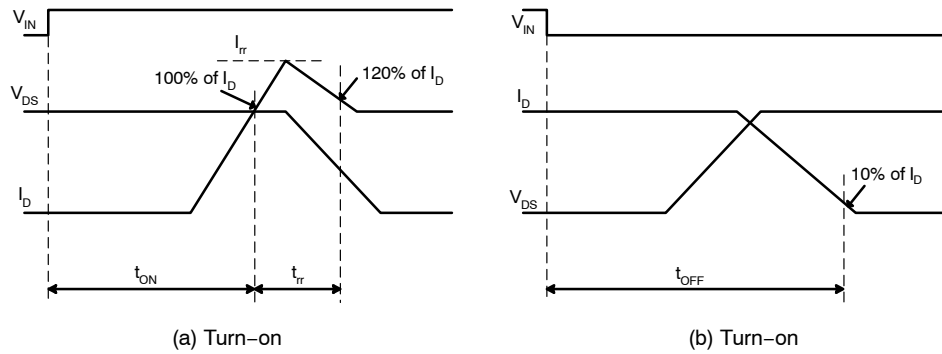


Figure 6. Switching Time Definitions

FSB50325A, FSB50325AT, FSB50325AS

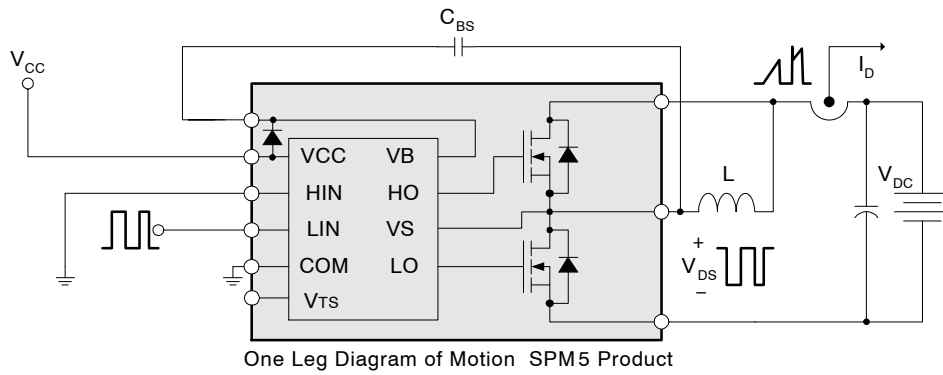


Figure 7. Switching and RBSOA (Single-pulse) Test Circuit (Low-side)

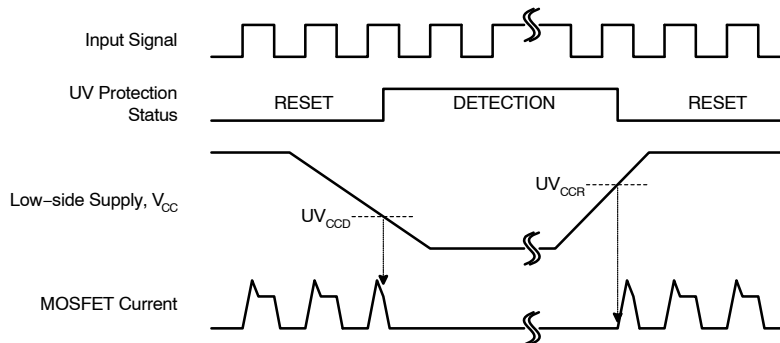


Figure 8. Under-Voltage Protection (Low-Side)

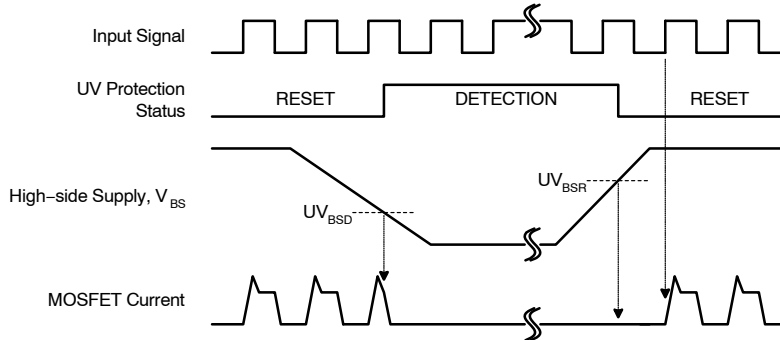


Figure 9. Under-Voltage Protection (High-Side)

FSB50325A, FSB50325AT, FSB50325AS

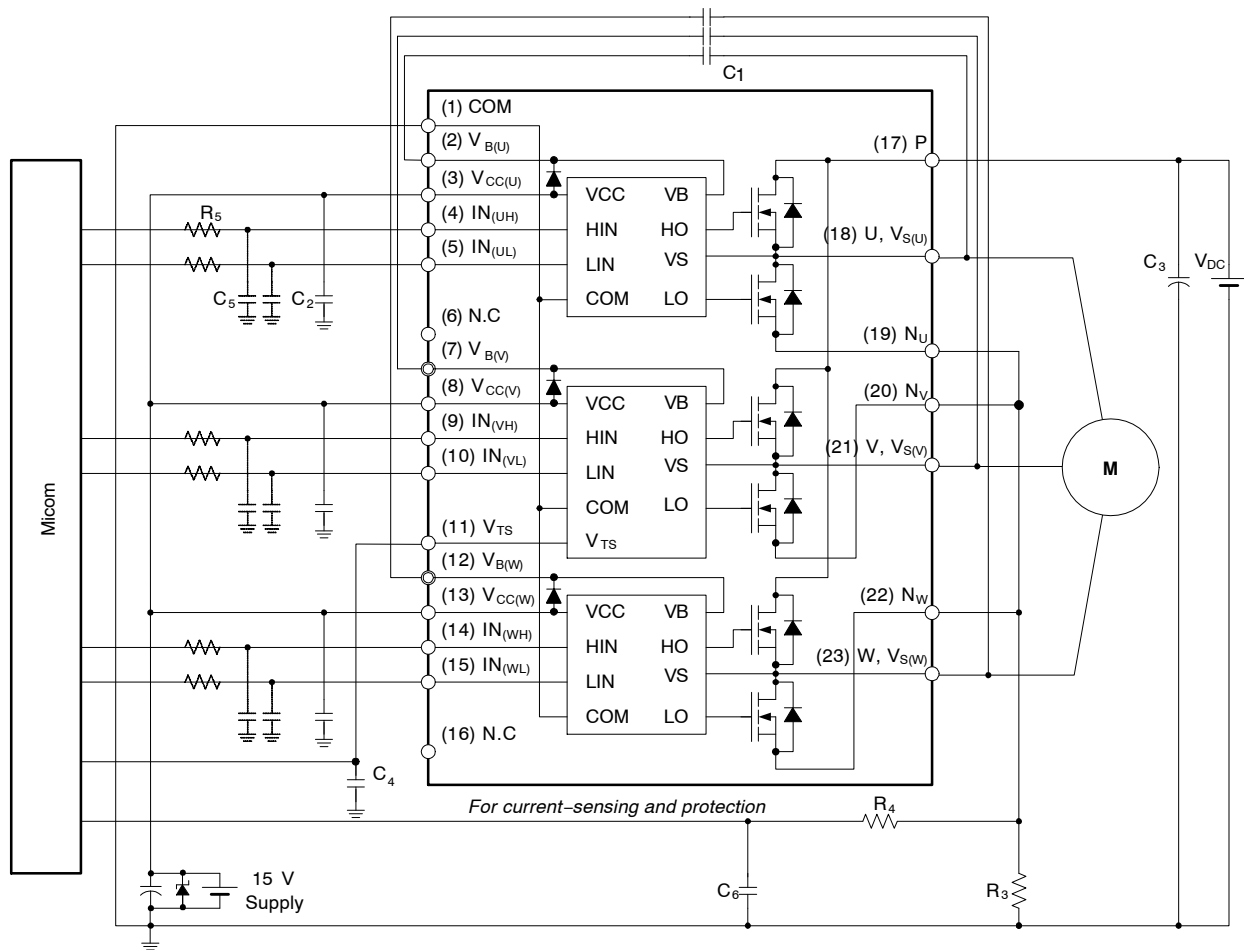


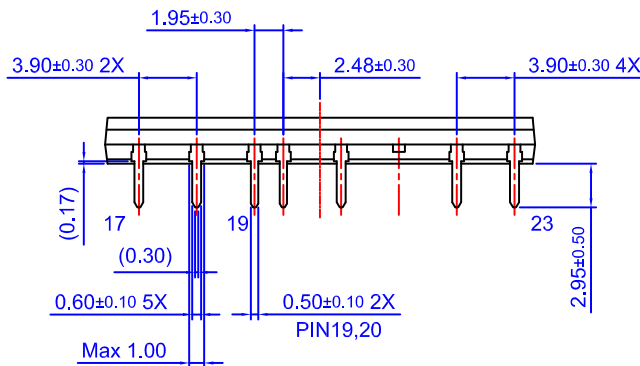
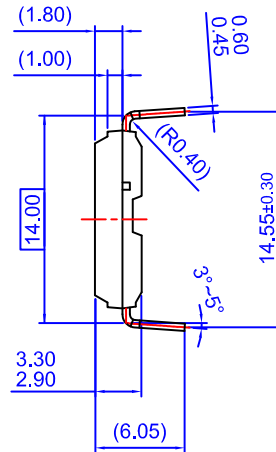
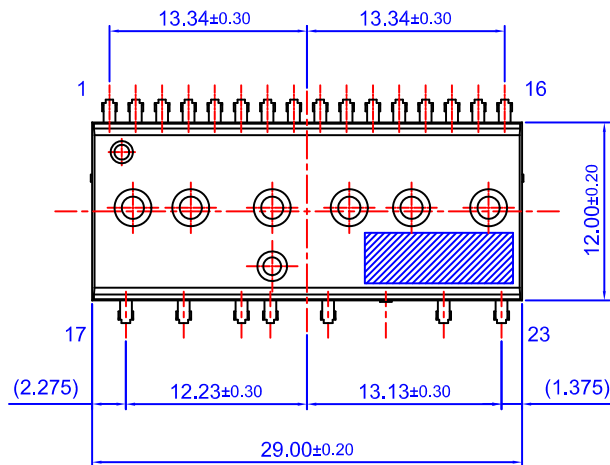
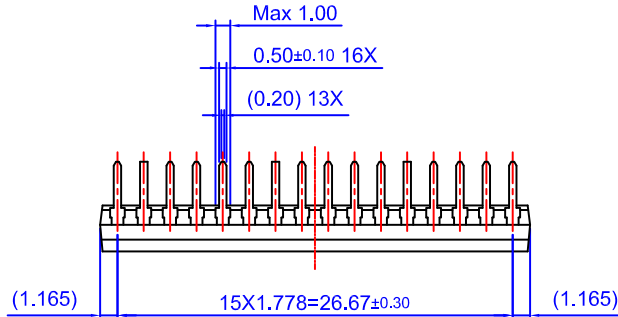
Figure 10. Example of Application Circuit

NOTES:

13. About pin position, refer to Figure 1.
14. RC-coupling (R_5 and C_5 , R_4 and C_6) and C_4 at each input of Motion SPM 5 product and MCU are useful to prevent improper input signal caused by surge-noise.
15. The voltage-drop across R_3 affects the low-side switching performance and the bootstrap characteristics since it is placed between COM and the source terminal of the low-side MOSFET. For this reason, the voltage-drop across R_3 should be less than 1 V in the steady-state.
16. Ground-wires and output terminals, should be thick and short in order to avoid surge-voltage and malfunction of HVIC.
17. All the filter capacitors should be connected close to Motion SPM 5 product, and they should have good characteristics for rejecting high-frequency ripple current.

SPM5E-023 / 23LD, PDD STD, FULL PACK, DIP TYPE
CASE MODEJ
ISSUE O

DATE 31 JAN 2017



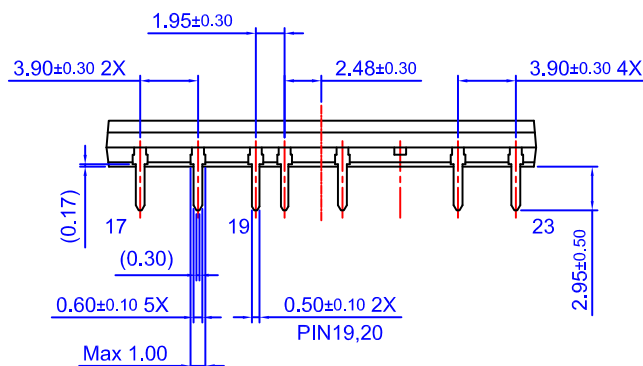
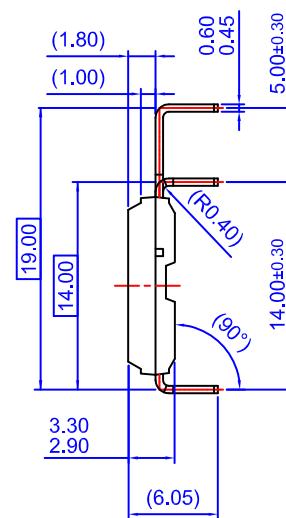
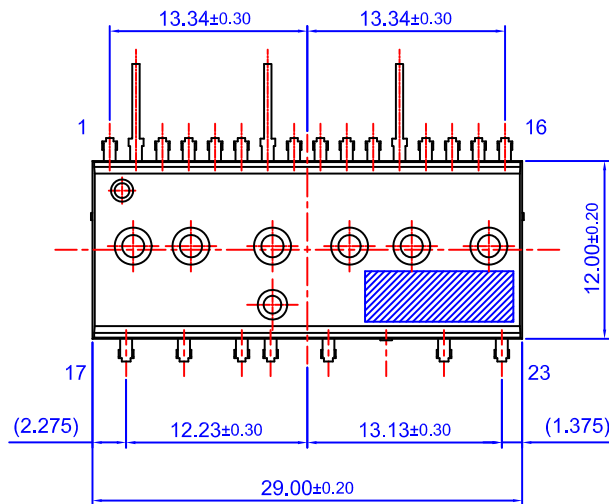
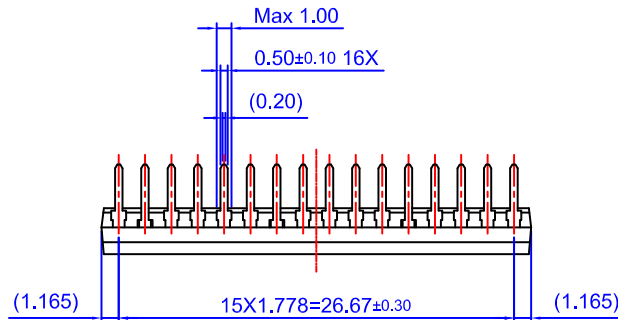
NOTES: UNLESS OTHERWISE SPECIFIED
 A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
 B) ALL DIMENSIONS ARE IN MILLIMETERS
 C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
 D) () IS REFERENCE

DOCUMENT NUMBER:	98AON13543G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SPM5E-023 / 23LD, PDD STD, FULL PACK, DIP TYPE	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SPM5G-023 / 23LD, PDD STD, FULL PACK, DOUBLE DIP TYPE (BSH)
CASE MODEL
ISSUE O

DATE 31 JAN 2017



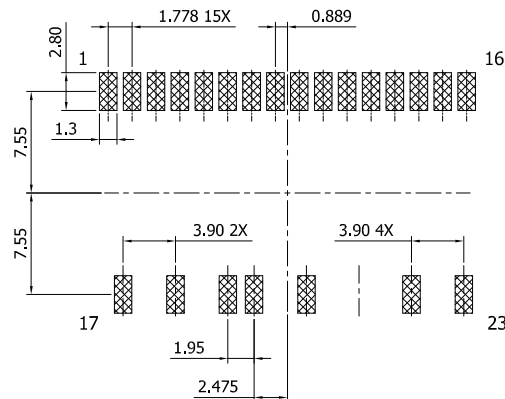
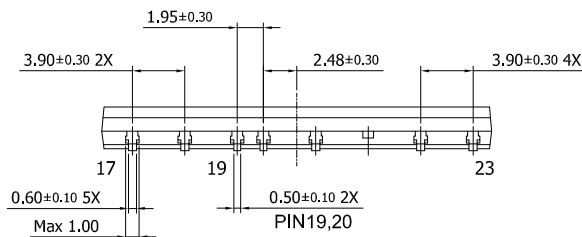
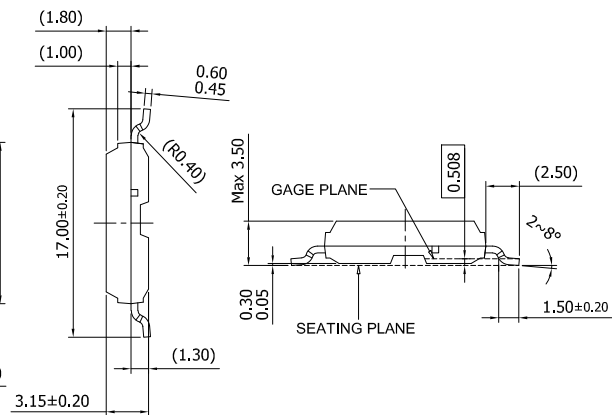
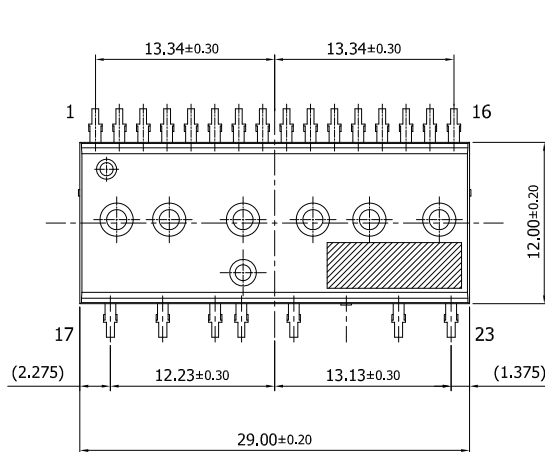
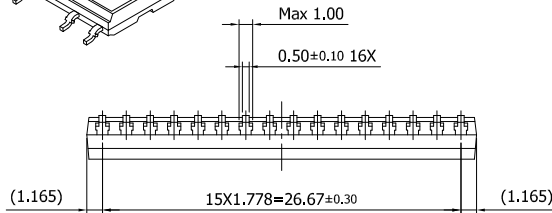
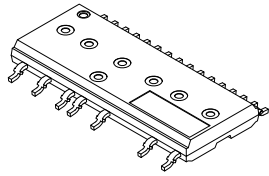
NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
B) ALL DIMENSIONS ARE IN MILLIMETERS
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D) () IS REFERENCE

DOCUMENT NUMBER:	98AON13545G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SPM5G-023 / 23LD, PDD STD, FULL PACK, DOUBLE DIP TYPE (BSH)	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SPM5H-023 / 23LD MODULE, SPM23-BD (Ver1.5) SMD TYPE
CASE MODEM
ISSUE A

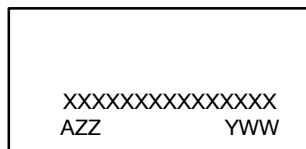
DATE 28 MAR 2025



- NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
B) ALL DIMENSIONS ARE IN MILLIMETERS
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D) () IS REFERENCE

LAND PATTERN RECOMMENDATIONS

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
ZZ = Assembly Lot Code
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON13546G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SPM5H-023 / 23LD MODULE, SPM23-BD (Ver1.5) SMD TYPE	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales