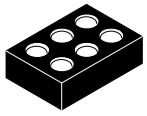
IntelliMAX™ 3 A-Capable, Slew-Rate-Controlled Load Switch with True Reverse Current Blocking

FPF1048



WLCSP6
CASE 567RM

MARKING DIAGRAM

RA = Device Code
K = 2−Digits Lot Run Traceability Code
&. = Pin One Dot
&2 = 2−Digit Date Code
&Z = Assembly Plant Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

Description

The FPF1048 advanced load management switch targets applications requiring a highly integrated solution. It disconnects loads powered from the DC power rail (<6 V) with stringent off−state current targets and high load capacitances (up to 100 μF). The FPF1048 consists of slew−rate controlled lowimpedance MOSFET switch (23 mΩ typical) and integrated analog features. The slew−rate controlled turn−on characteristic prevents inrush current and the resulting excessive voltage droop on power rails.

The FPF1048 has a True Reverse Current Blocking (TRCB) function that obstructs unwanted reverse current from V_{OUT} to V_{IN} during both ON and OFF states. The exceptionally low off−state current drain (<1 μA maximum) facilitates compliance with standby power requirements. The input voltage range operates from 1.5 V to 5.5 V_{DC} to support a wide range of applications in consumer, optical, medical, storage, portable, and industrial−device power management. Switch control is managed by a logic input (active HIGH) capable of interfacing directly with low−voltage control signal / General−Purpose Input / Output (GPIO) without an external pull−down resistor.

The device is packaged in advanced, fully “green” compliant, 1.0 mm x 1.5 mm, Wafer−Level Chip−Scale Package (WLCSP) with backside lamination.

Features

- Input Voltage Operating Range: 1.5 V to 5.5 V
- Typical $R_{DS(ON)}$:
  - 21 mΩ at V_{IN} = 5.5 V
  - 23 mΩ at V_{IN} = 4.5 V
  - 41 mΩ at V_{IN} = 1.8 V
  - 90 mΩ at V_{IN} = 1.5 V
- Slew Rate/Inrush Control with t_R: 2.7 ms (Typ.)
- 3 A Maximum Continuous Current Capability
- Low Off Switch Current: <1 μA
- True Reverse Current Blocking (TRCB)
- Logic CMOS IO Meets JESD76 Standard for GPIO Interface and Related Power Supply Requirements
- ESD Protected:
  - Human Body Model: >8 kV
  - Charged Device Model: >1.5 kV
  - IEC 61000−4−2 Air Discharge: >15 kV
  - IEC 61000−4−2 Contact Discharge: >8 kV
- This is a Pb−Free Device

Applications

- Smart Phones, Tablet PCs
- Storage, DSLR, and Portable Devices

Application Diagram

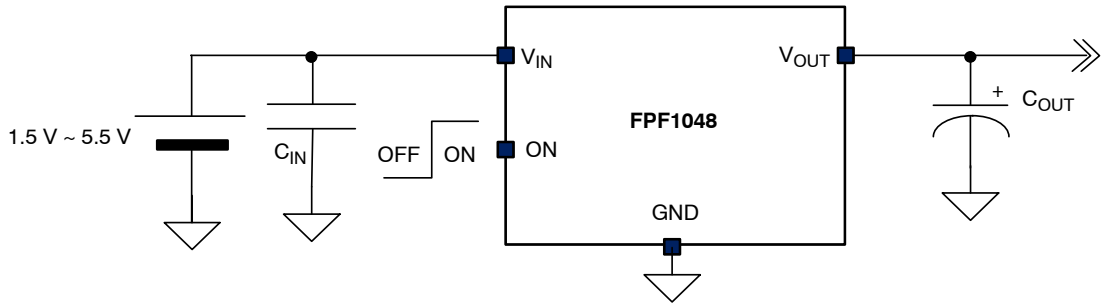


Figure 1. General Application

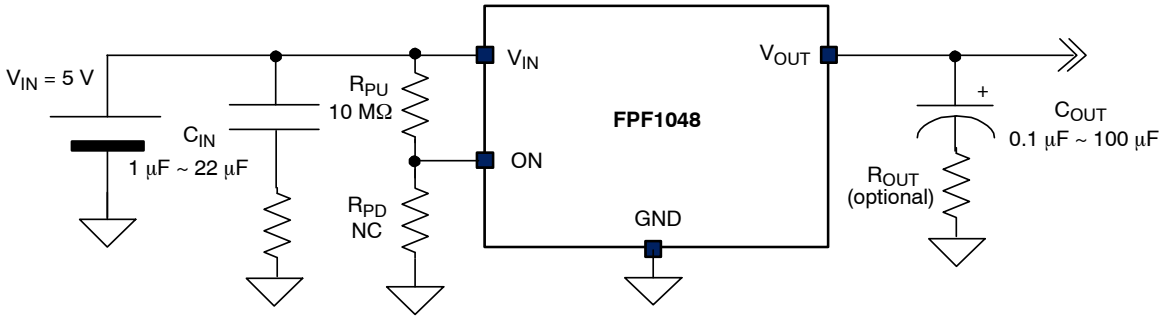


Figure 2. Specific Application with 10 MΩ Pull−Up Resistor at ON Pin

NOTES:
1. Turn−on operation with a 10 MΩ pull−up resistor at ON pin is acceptable.
2. V_{IN} should be high enough to generate V_{ON} greater than V_{IH} at the ON pin.
3. NC means no connection.
4. R_{IN} and R_{OUT} can be added to reduce transient peak voltage. 1 Ω ~ 10 Ω is recommended.

Functional Block Diagram

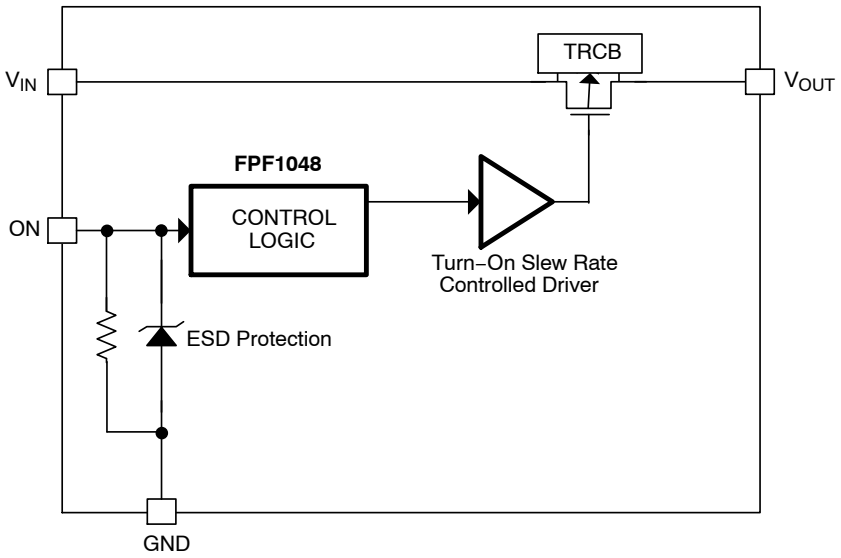


Figure 3. Functional Block Diagram

Pin Configurations

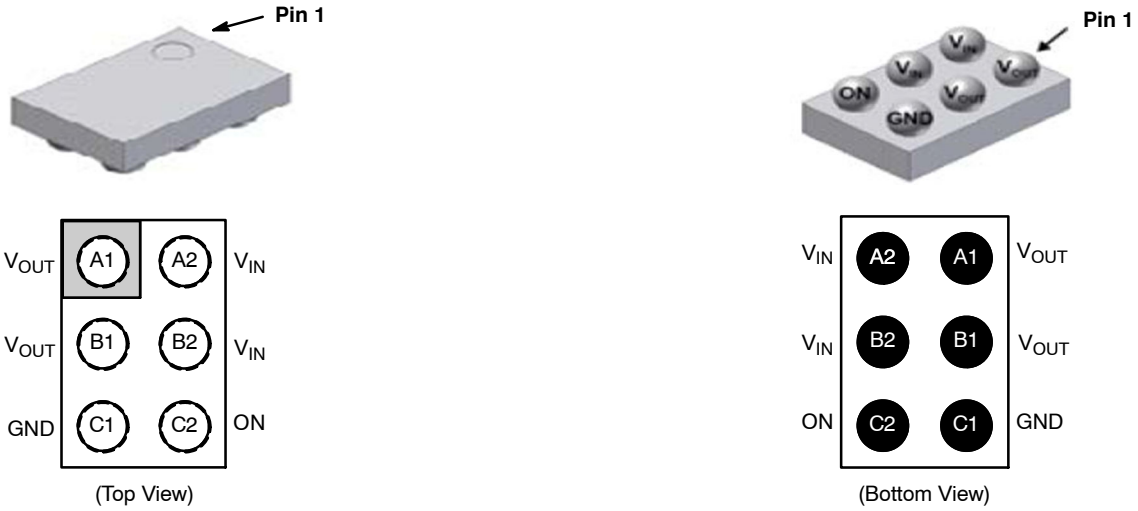


Figure 4. Pin Assignments

PIN DESCRIPTIONS

Pin #	Name	Description
A1, B1	V_{OUT}	Switch Output
A2, B2	V_{IN}	Supply Input: Input to the Power Switch
C1	GND	Ground
C2	ON	ON/OFF Control, Active High, GPIO Compatible

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter			Min	Max	Unit
V_{IN}	V_{IN}, V_{OUT}, V_{ON} to GND			−0.3	6.0	V
I_{SW}	Maximum Continuous Switch Current			–	3.0	A
P_D	Power Dissipation at T_A = 25°C			–	1.2	W
T_{STG}	Storage Junction Temperature			−65	+150	°C
T_A	Operating Temperature Range			−40	+85	°C
θ_{JA}	Thermal Resistance, Junction to Ambient			–	85 (Note 5)	°C/W
				–	110 (Note 6)	
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22−A114		8.0	–	kV
		Charged Device Model, JESD22−C101		1.5	–	
		IEC61000−4−2 System Level	Air Discharge (V_{IN}, V_{ON}, V_{OUT} to GND)	15.0	–	
			Contact Discharge (V_{IN}, V_{ON}, V_{OUT} to GND)	8.0	–	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

5. Measured using 2S2P JEDEC std. PCB.
6. Measured using 2S2P JEDEC PCB cold plate method.

RECOMMENDED OPERATING RANGE

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Input Voltage	1.5	–	5.5	V
T_A	Ambient Operating Temperature	−40	–	+85	°C
I_{SW}	Continuous Switch Current	–	2.5	3	A

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{IN} = 1.5 V to 5.5 V, T_A = −40 to +85°C, typical values are at V_{IN} = 4.5 V and T_A = 25°C.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
BASIC OPERATION						
V_{IN}	Input Voltage		1.5	–	5.5	V
$I_{Q(OFF)}$	Off Supply Current	V_{ON} = GND, V_{OUT} = Open	–	–	1	μA
I_{SD}	Shutdown Current	V_{ON} = GND, V_{OUT} = GND, T_A = −40 to +85°C	–	0.2	4.0	μA
I_Q	Quiescent Current	I_{OUT} = 0 mA	–	–	11	μA
R_{ON}	On−Resistance	V_{IN} = 5.5 V, I_{OUT} = 3 A (Note 7)	–	22.0	–	mΩ
		V_{IN} = 5.5 V, I_{OUT} = 2 A (Note 7)	–	21.5	–	
		V_{IN} = 5.5 V, I_{OUT} = 1 A, T_A = 25°C	–	21.0	28.0	
		V_{IN} = 4.5 V, I_{OUT} = 3 A (Note 7)	–	24.0	–	
		V_{IN} = 4.5 V, I_{OUT} = 2 A (Note 7)	–	23.5	–	
		V_{IN} = 4.5 V, I_{OUT} = 1 A, T_A = 25°C	–	23.0	30.0	
		V_{IN} = 3.3 V, I_{OUT} = 500 mA, T_A = 25°C	–	26.0	–	
		V_{IN} = 2.5 V, I_{OUT} = 500 mA, T_A = 25°C	–	30.0	–	
		V_{IN} = 1.8 V, I_{OUT} = 250 mA, T_A = 25°C	–	41.0	–	
		V_{IN} = 1.5 V, I_{OUT} = 250 mA, T_A = 25°C	–	90.0	110.0	
V_{IH}	ON Input Logic High Voltage	V_{IN} = 1.5 V to 5.5 V	1.15	–	–	V
V_{IL}	ON Input Logic Low Voltage	V_{IN} = 1.8 V to 5.5 V	–	–	0.65	V
		V_{IN} = 1.5 V to 1.8 V	–	–	0.60	
I_{ON}	ON Input Leakage	V_{ON} = V_{IN} or GND	–	–	1.0	μA
R_{ON_PD}	Pull−Down Resistance at ON Pin	V_{IN} = V_{ON} = 1.5 V to 5.5 V, T_A = −40°C − +85°C	6.38	7.65	8.86	MΩ
TRUE REVERSE CURRENT BLOCKING						
V_{T_RCB}	RCB Protection Trip Point	V_{OUT}−V_{IN}	–	45	–	mV
V_{R_RCB}	RCB Protection Release Trip Point	V_{IN}−V_{OUT}	–	25	–	mV
	RCB Hysteresis		–	70	–	mV
I_{SD_OUT}	V_{OUT} Shutdown Current	V_{ON} = 0, V_{OUT} = 4.5 V, V_{IN} = Short to GND	–	–	2	μA
t_{RCB_ON}	RCB Response Time, Device ON	V_{OUT} − V_{IN} = 100 mV, V_{ON} = HIGH	–	4	–	μs
t_{RCB_OFF}	RCB Response Time, Device OFF	V_{OUT} − V_{IN} = 100 mV, V_{ON} = LOW	–	2.5	–	μs
DYNAMIC CHARACTERISTICS						
t_{DON}	Turn−On Delay (Notes 8, 9)	V_{IN} = 4.5 V, R_L = 5 Ω, C_L = 100 μF, T_A = 25°C	–	1.7	–	ms
t_R	V_{OUT} Rise Time (Notes 8, 9)		–	2.7	–	ms
t_{ON}	Turn−On Time (Notes 8, 9)		–	4.4	–	ms
t_{DON}	Turn−On Delay (Notes 8, 9)	V_{IN} = 4.5 V, R_L = 150 Ω, C_L = 100 μF, T_A = 25°C	–	1.7	–	ms
t_R	V_{OUT} Rise Time (Notes 8, 9)		–	1.5	–	ms
t_{ON}	Turn−On Time (Notes 8, 9)		–	3.2	–	ms
t_{DOFF}	Turn−Off Delay (Notes 8, 10)	V_{IN} = 4.5 V, R_L = 150 Ω, C_L = 100 μF, T_A = 25°C	–	1.8	–	ms
t_F	V_{OUT} Fall Time (Notes 8, 10)		–	34	–	ms
t_{OFF}	Turn−Off Time (Notes 8, 10)		–	35	–	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. This parameter is guaranteed by design and characterization; not production tested.
8. t_{DON}/t_{DOFF}/t_R/t_F are defined in Figure 21.
9. t_{ON} = t_R + t_{DON}.
10. t_{OFF} = t_F + t_{DOFF}

TYPICAL CHARACTERISTICS

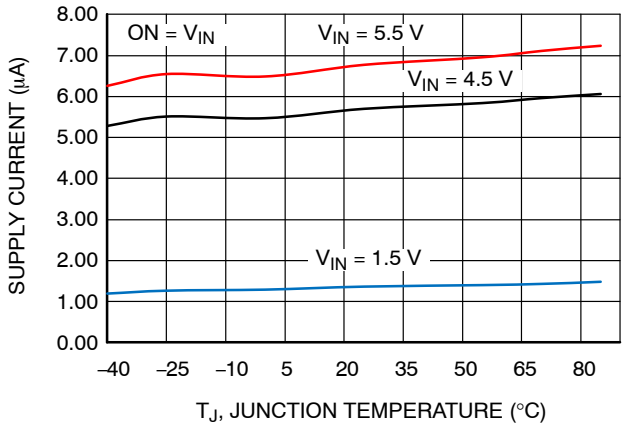


Figure 5. Supply Current vs. Temperature

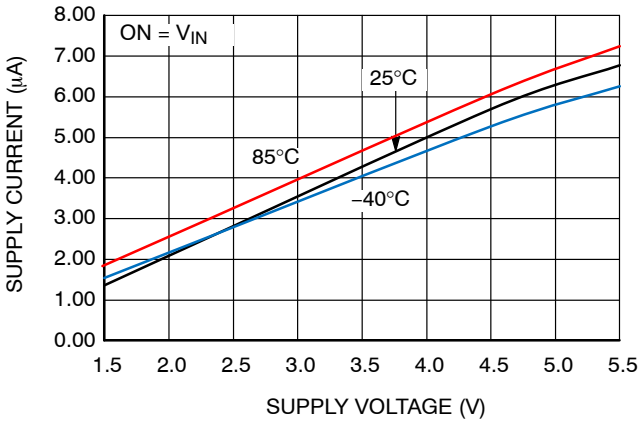


Figure 6. Supply Current vs. Supply Voltage

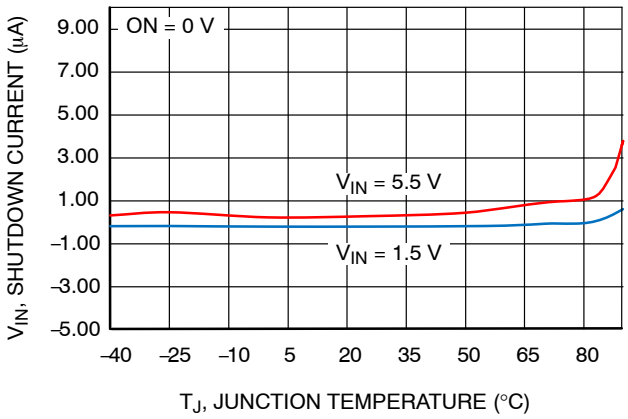


Figure 7. Shutdown Current vs. Temperature

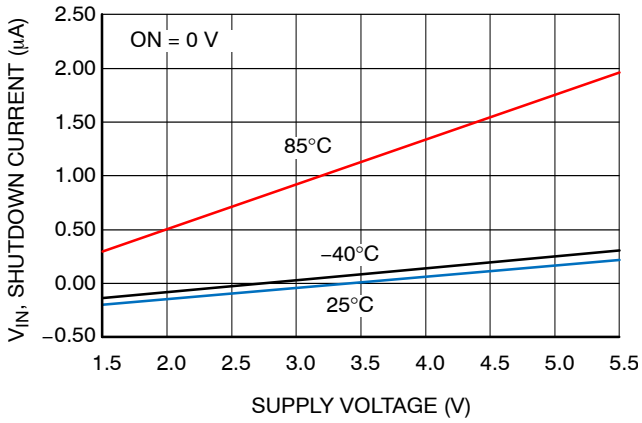


Figure 8. Shutdown Current vs. Supply Voltage

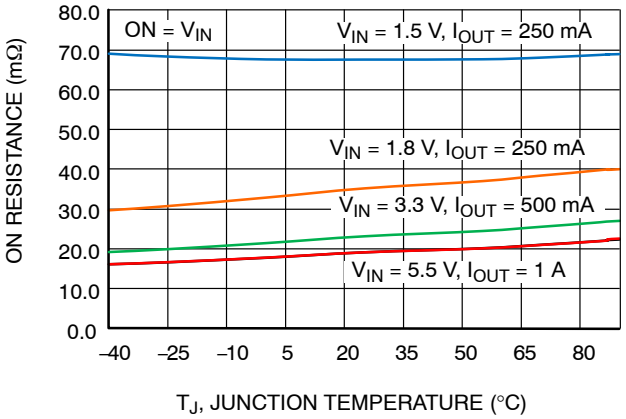


Figure 9. R_{ON} vs. Temperature

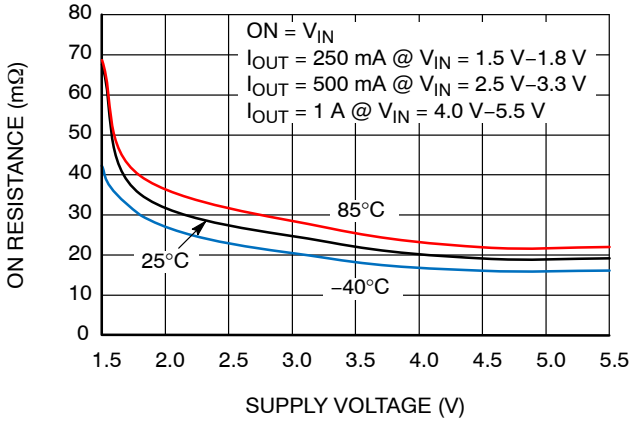


Figure 10. R_{ON} vs. Supply Voltage

TYPICAL CHARACTERISTICS (continued)

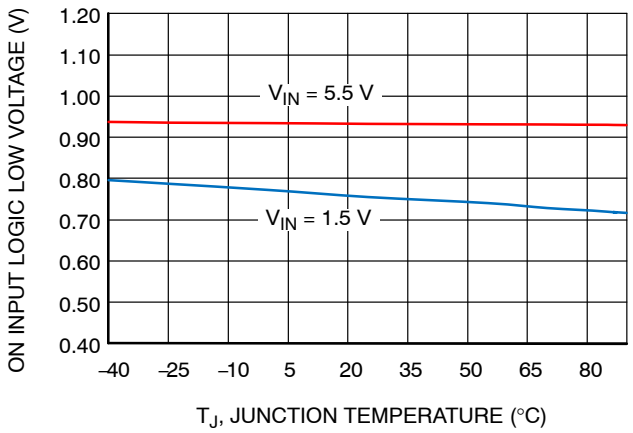


Figure 11. V_{IL} vs. Temperature

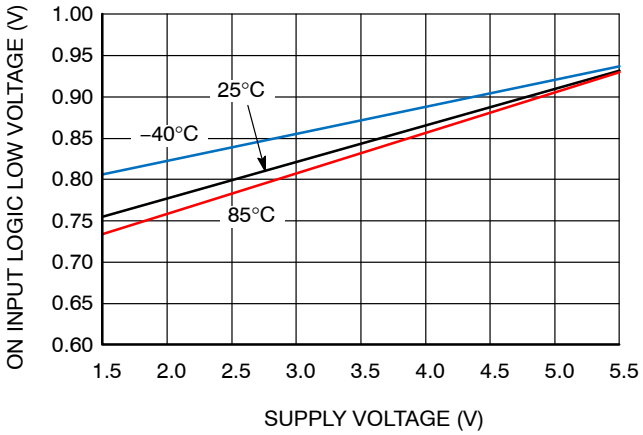


Figure 12. V_{IL} vs. Supply Voltage

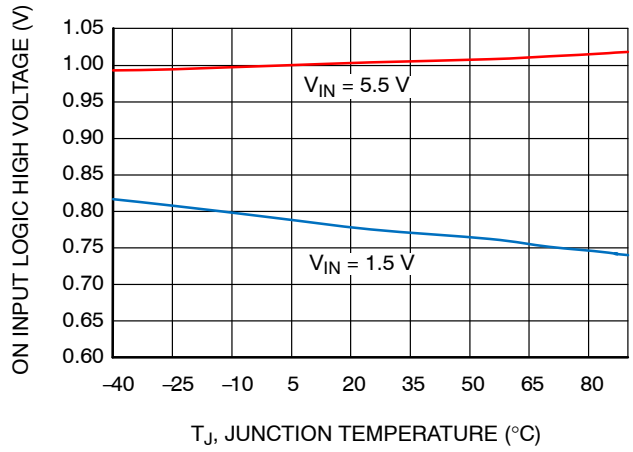


Figure 13. V_{IH} vs. Temperature

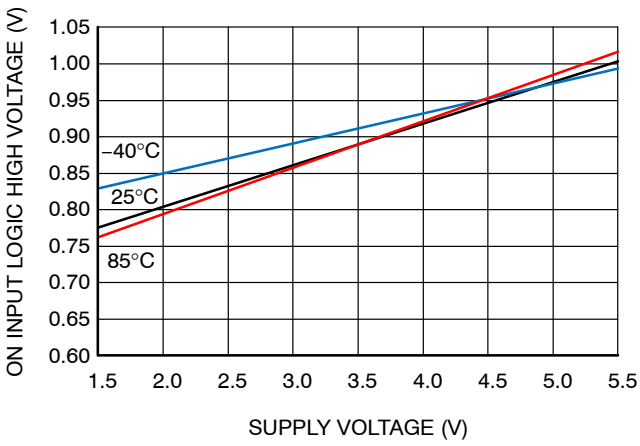


Figure 14. V_{IH} vs. Supply Voltage

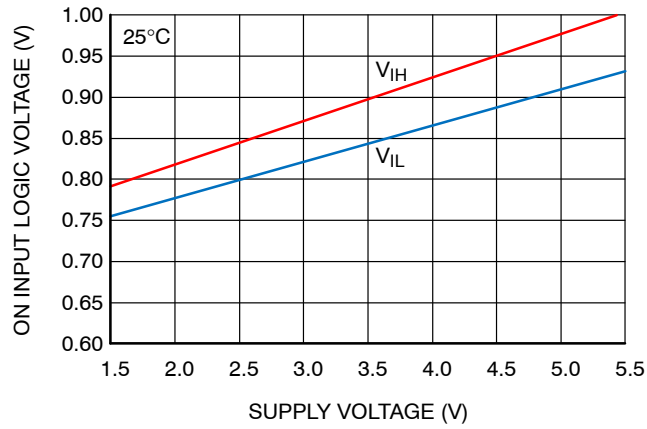


Figure 15. On Pin Threshold vs. Supply Voltage

TYPICAL CHARACTERISTICS (continued)

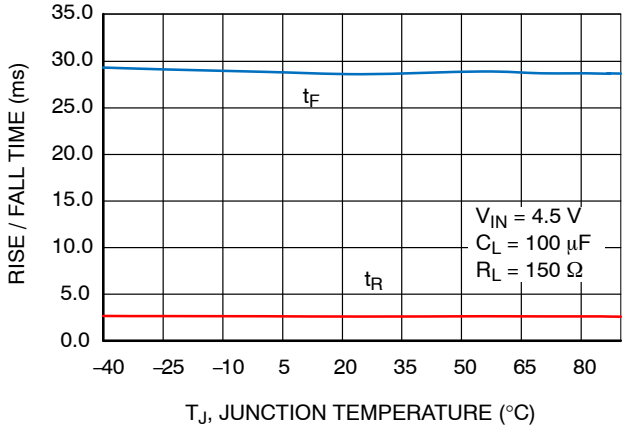


Figure 16. t_R / t_F vs. Temperature

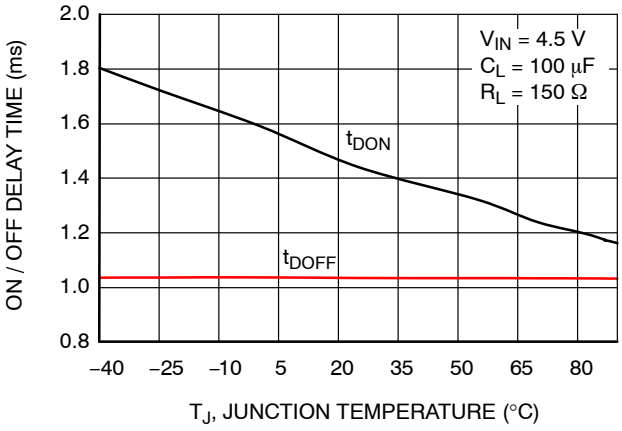


Figure 17. t_{DON} vs. Temperature

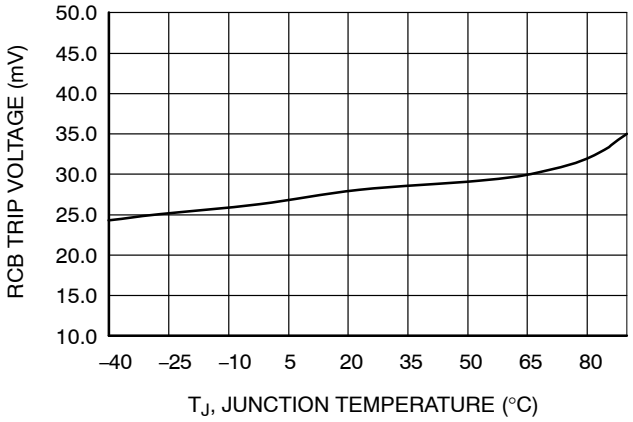


Figure 18. RCB Trip vs. Temperature

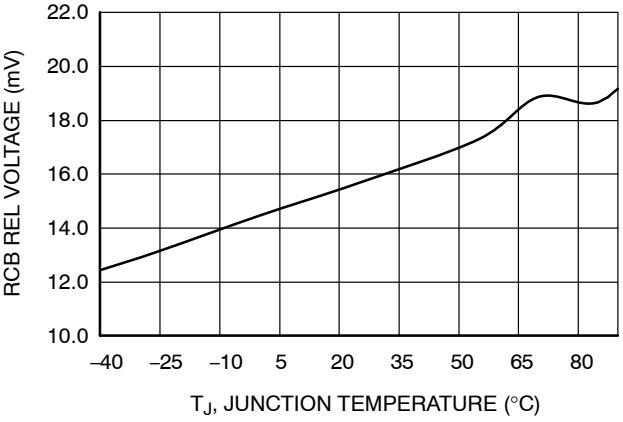


Figure 19. RCB Release vs. Temperature

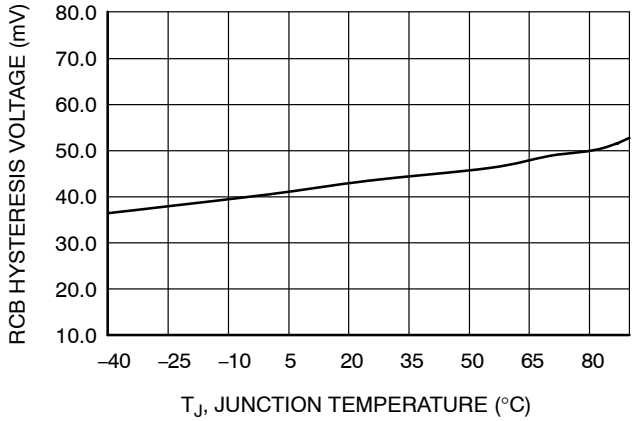


Figure 20. RCB Hysteresis vs. Temperature

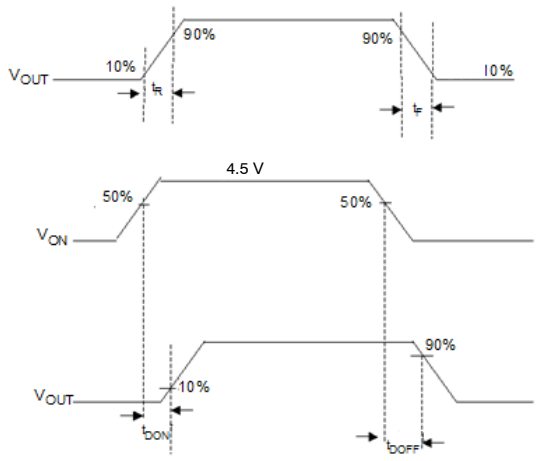


Figure 21. Timing Diagram

TYPICAL CHARACTERISTICS (continued)

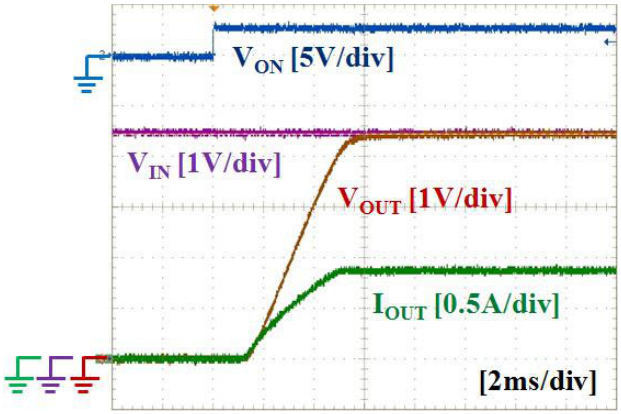


Figure 22. Turn−On Response
(V_{IN} = 4.5 V, C_{IN} = 10 μF, C_{OUT} = 100 μF, R_L = 5 Ω)

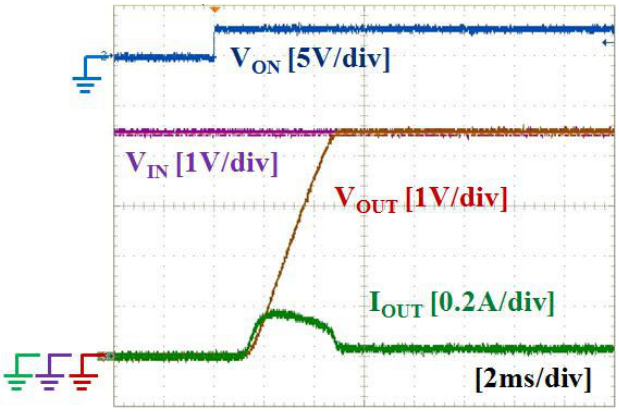


Figure 23. Turn−On Response
(V_{IN} = 4.5 V, C_{IN} = 10 μF, C_{OUT} = 100 μF, R_L = 150 Ω)

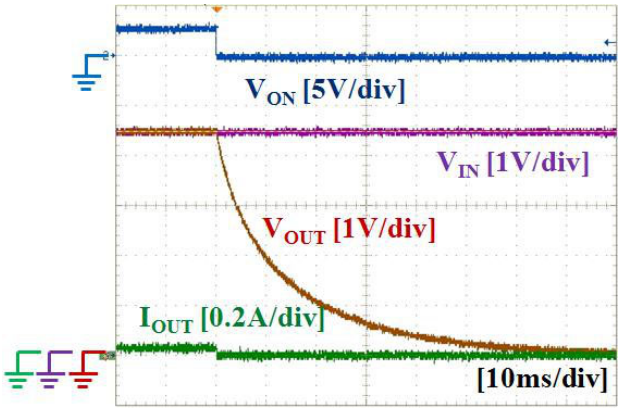


Figure 24. Turn−Off Response
(V_{IN} = 4.5 V, C_{IN} = 10 μF, C_{OUT} = 100 μF, R_L = 150 Ω)

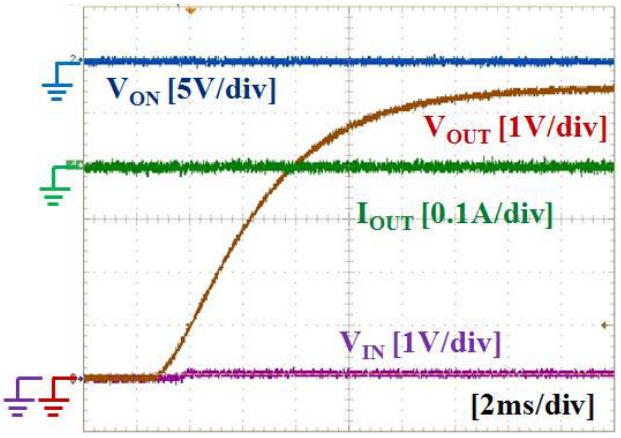


Figure 25. RCB Response During Off
(V_{IN} = Open, V_{ON} = GND, V_{OUT} = 5.5 V, C_{IN} = 10 μF, C_{OUT} = 100 μF)

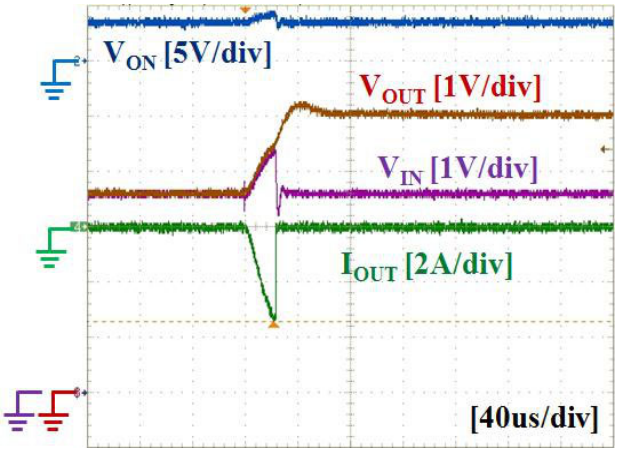


Figure 26. RCB Response During On
(V_{IN} = V_{ON} = 3.6 V, V_{OUT} = 5 V, C_{IN} = 10 μF, C_{OUT} = 100 μF)

Operation and Application Description

The FPF1048 is a low−R_{ON} P−channel load switch with controlled turn−on and True Reverse Current Blocking (TRCB). The core is a 23 mΩ P−channel MOSFET and controller capable of functioning over a wide input operating range of 1.5 V to 5.5 V. The ON pin, an active−HIGH, GPIO/CMOS−compatible input; controls the state of the switch. TRCB functionality blocks unwanted reverse current during both ON and OFF states when higher V_{OUT} than V_{IN} is applied.

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into a discharged load capacitor; a capacitor must be placed between the V_{IN} and GND pins. At least 1 μF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. Higher−value C_{IN} can be used to reduce the voltage drop in higher−current applications.

Inrush Current

Inrush current occurs when the device is turned on. Inrush current is dependent on output capacitance and slew rate control capability, as expressed by:

$$I_{INRUSH} = C_{OUT} \times \frac{V_{IN} - V_{INITIAL}}{t_R} + I_{LOAD} \qquad \text{(eq. 1)}$$

Where:

C_{OUT}	Ouput capacitance;
tR	Slew rate or rise time at V_{OUT};
V_{IN}	Input voltage;
$V_{INITIAL}$	Initial voltage at C_{OUT}, usually GND; and
I_{LOAD}	Load current.

Higher inrush current causes higher input voltage drop, depending on the distributed input resistance and input capacitance. High inrush current can cause problems.

FPF1048 has a 2.7 ms of slew rate capability under 4.5 V_{IN} at 1000 μF of C_{OUT} and 5 Ω of RL so inrush current can be minimized and no input voltage drop appears. Table 1 and Figure 27 show the values and actual waveforms with C_{IN} = 10 μF, C_{OUT} = 100 μF, and no load current.

Table 1. INRUSH CURRENT BY INPUT VOLTAGE

V_{IN} [V]	t_R [ms]	Inrush Current [mA]	
		Measured	Calculated with 2.7 ms t_R
1.5	1.62	76	56
3.3	2.03	140	122
5.0	2.33	196	185

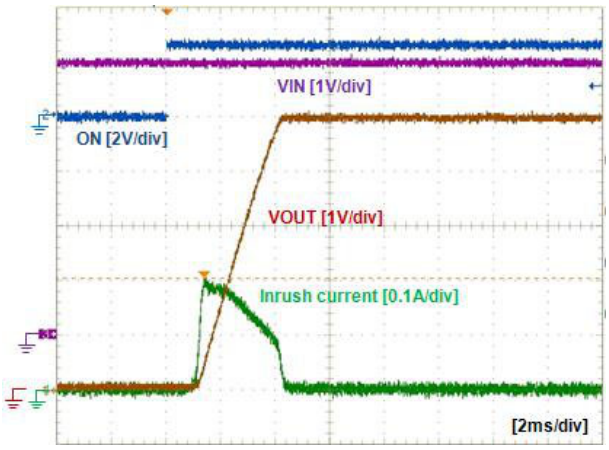


Figure 27. Inrush Current Waveform, Under 5 V_{IN}, C_{OUT} = 100 μF, no Load

Output Capacitor

At least 0.1 μF capacitor, C_{OUT}, should be placed between the V_{OUT} and GND pins. This capacitor prevents parasitic board inductance from forcing V_{OUT} below GND when the switch is on.

True Reverse Current Blocking

The true reverse current blocking feature protects the input source against current flow from output to input regardless of whether the load switch is on or off.

Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effect that parasitic trace inductance on normal and short−circuit operation. Using wide traces or large copper planes for all pins (V_{IN}, V_{OUT}, ON, and GND) minimizes the parasitic electrical effects and the case−to−ambient thermal impedance.

ORDERING INFORMATION

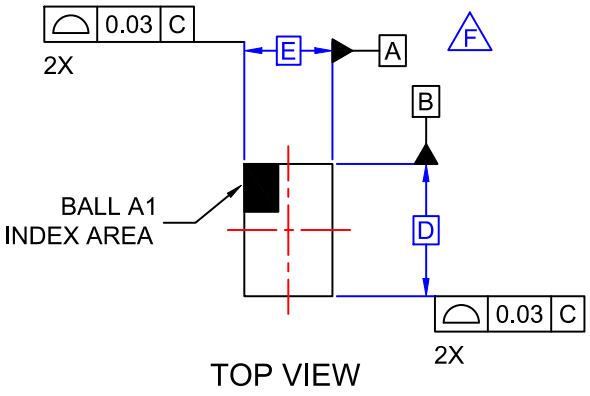
Part Number	Top Mark	Switch R_{ON} (Typical) at 4.5 V_{IN}	Input Buffer	Output Discharge	ON Pin Activity	t_R	Package
FPF1048BUCX	RA	23 mΩ	CMOS	NA	Active HIGH	2.7 ms	6−Ball, WLCSP with Backside Laminate, 2 x 3 Array, 0.5 mm Pitch, 300 μm Balls

PRODUCT−SPECIFIC DIMENSIONS

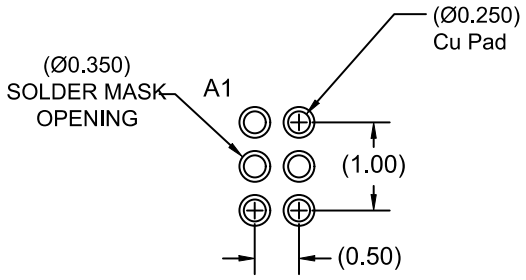
Product	D	E	X	Y
FPF1048BUCX	1460 μm ±30 μm	960 μm ±30 μm	230 μm	230 μm

WLCSP6 1.46x0.96x0.582
CASE 567RM
ISSUE O

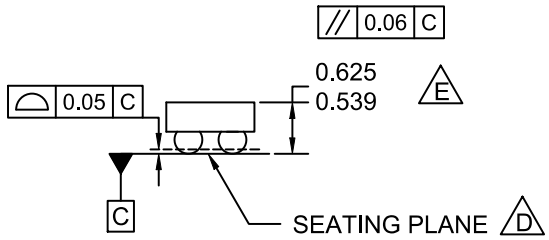
DATE 30 NOV 2016

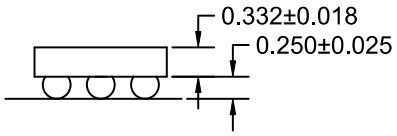


TOP VIEW

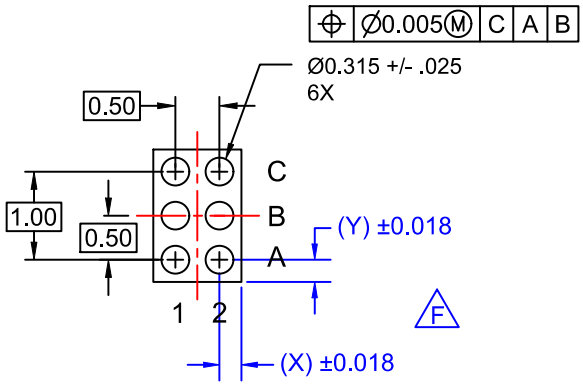


RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 582 MICRONS ±43 MICRONS (539-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

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DESCRIPTION:	**WLCSP6 1.46x0.96x0.582**	**PAGE 1 OF 1**

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