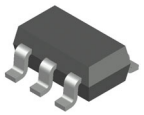
LVDS 1-Bit, High-Speed Differential Reciever

FIN1002



SOT−23, 5 Lead
CASE 527AH

Description

This single receiver is designed for high−speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The receiver translates LVDS levels, with a typical differential input threshold of 100 mV, to LVTTL signal levels. LVDS provides low EMI at ultra low power dissipation even at high frequencies. This device is ideal for high−speed transfer of clock or data. The FIN1002 can be paired with its companion driver, the FIN1001, or with any other LVDS driver.

Features

- Greater than 400 Mbs Data Rate
- 3.3 V Power Supply Operation
- 0.4 ns Maximum Pulse Skew
- 2.5 ns Maximum Propagation Delay
- Bus Pin ESD (HBM) Protection Exceeds 10 kV
- Power−Off, Over−voltage Tolerant Input and Output
- Fail−safe Protection for open−circuit and Non−driven, Shorted, or Terminated Conditions
- High−impedance Output at V_{CC} < 1.5 V
- Meets or exceeds TIA/EIA−644 LVDS Standard
- 5−Lead SOT23 Package Saves Space

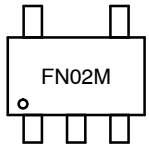
PIN DEFINITIONS

Pin No.	Function	Description
1	V_{CC}	Power Supply
2	GND	Ground for the IC
3	R_{IN+}	Non−inverting Driver Input
4	$R_{IN−}$	Inverting Driver Input
5	R_{OUT}	LVTTL Data Output

FUNCTION TABLE

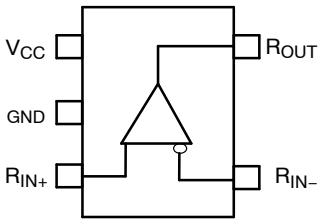
Inputs		Outputs
R_{IN+}	R_{IN-}	R_{OUT}
LOW	HIGH	LOW
HIGH	LOW	HIGH
Fail−Safe Condition (Open, Shorted, Terminated)		HIGH

MARKING DIAGRAM



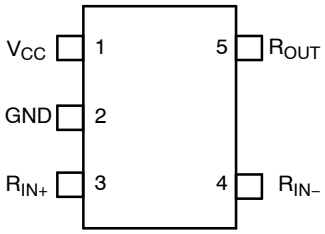
FN02 = Specific Device Code
M = Date Code

CONNECTION DIAGRAM



(Top View)

PIN CONFIGURATION



ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter			Min.	Max.	Unit
V_{CC}	Supply Voltage			−0.5	4.6	V
R_{IN+} / R_{IN-}	Input Voltage			−0.5	4.6	V
D_{OUT}	DC Output Voltage			−0.5	6.0	V
I_O	Output Current				16	mA
T_{STG}	Storage Temperature Range			−65	+150	°C
T_J	Maximum Junction Temperature				+150	°C
T_L	Lead Temperature, Soldering, 10 Seconds				+260	°C
ESD	Electrostatic Discharge	Human Body Model	All Pins		8	kV
			LVDS Pins to GND		10	
		Machine Model			400	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING RANGES

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.6	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_{ID}	Magnitude of Differential Voltage	100	V_{CC}	mV
V_{IC}	Common−mode Input Voltage	$0 + \|V_{ID}\| / 2$	$2.4 - \|V_{ID}\| / 2$	V
T_A	Operating Temperature	−40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Note 1)

All min. and max. values are guaranteed at T_A = −40 to +125°C. All typical values are at T_A = 25°C and with V_{CC} = 3.3 V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{TH}	Differential Input Threshold HIGH	V_{IC} = +0.05 V, 1.2 V, or 2.35 V (Figure 1)			100	mV
V_{TL}	Differential Input Threshold LOW	V_{IC} = +0.05 V, 1.2 V, or 2.35 V (Figure 1)	−100			mV
I_{IN}	Input Current	V_{IN} = 0 V or V_{CC}			±20	μA
$I_{I(OFF)}$	Power−OFF Input Current	V_{CC} = 0 V, V_{IN} = 0 V or 3.6 V			±20	μA
V_{OH}	Output HIGH Voltage	I_{OH} = −100 μA	V_{CC} − 0.2	3.3		V
		I_{OH} = −8 mA	2.4	3.1		
V_{OL}	Output LOW Voltage	I_{OH} = 100 μA		0	0.2	V
		I_{OL} = 8 mA		0.16	0.50	
V_{IK}	Input Clamp Voltage	I_{IK} = −18 mA	−1.5	0.8		V
I_{CC}	Power Supply Current	(R_{IN+} = 1 V and R_{IN-} = 1.4 V) or (R_{IN+} = 1.4 V and R_{IN-} = 1 V)		4	7	mA
C_{IN}	Input Capacitance	V_{CC} = 3.3 V		2.3		pF
C_{OUT}	Output Capacitance	V_{CC} = 0 V		2.8		pF

1. Not production tested across the full temperature range.

AC ELECTRICAL CHARACTERISTICS

All min. and max. values are guaranteed at T_A = −40 to +85°C. All typical values are at T_A = 25°C and with V_{CC} = 3.3 V, unless otherwise specified.

$|V_{ID}|$ = 400 mV, C_L = 10 pF. See Figure 1 and Figure 2.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay	LOW to HIGH	0.9	1.5	2.5	ns
t_{PHL}	Propagation Delay	HIGH to LOW	0.9	1.5	2.5	ns
t_{TLH}	Output Rise Time	20% to 80%		0.6		ns
t_{THL}	Output Fall Time	80% to 20%		0.5		ns
$t_{SK(p)}$	Pulse Skew	$\|t_{PLH} - t_{PHL}\|$		0.02	0.4	ns
$t_{SK(PP)}$	Part−to−Part Skew (Note 2)				1.0	ns

2. $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW−to−HIGH or HIGH−to−LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.

TEST DIAGRAMS

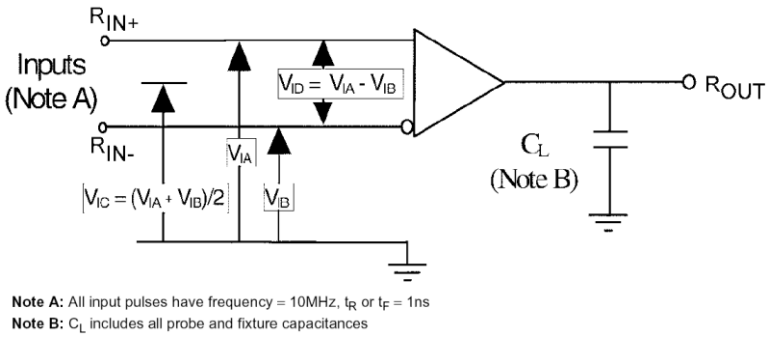


Figure 1. Differential Receiver Voltage Definitions and Propagation Delay and Transition Time Test Circuit

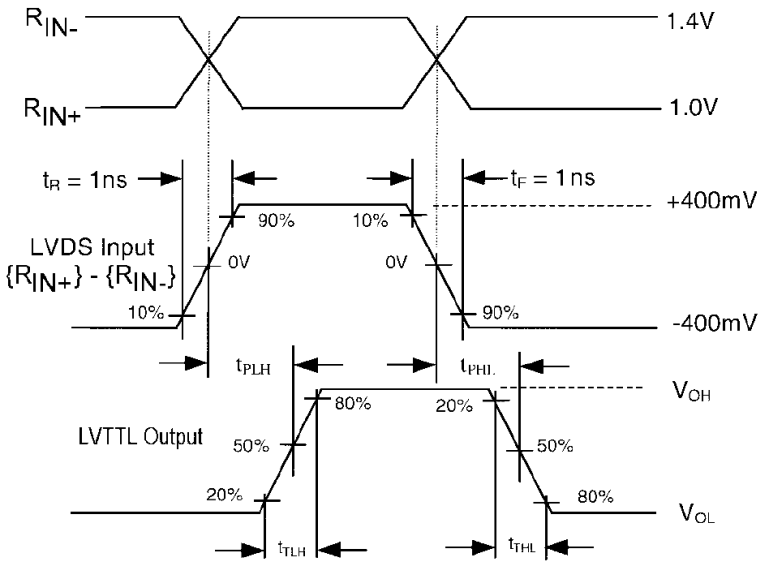


Figure 2. LVDS Input to LVTTL Output AC Waveforms

TYPICAL CHARACTERISTICS

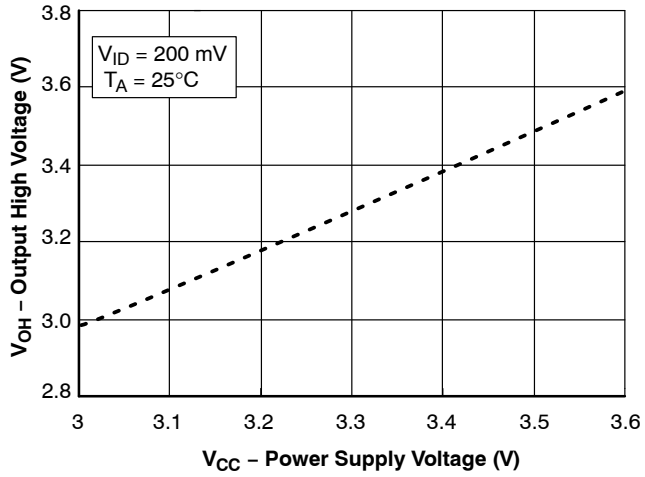


Figure 3. Output High Voltage vs. Power Supply Voltage

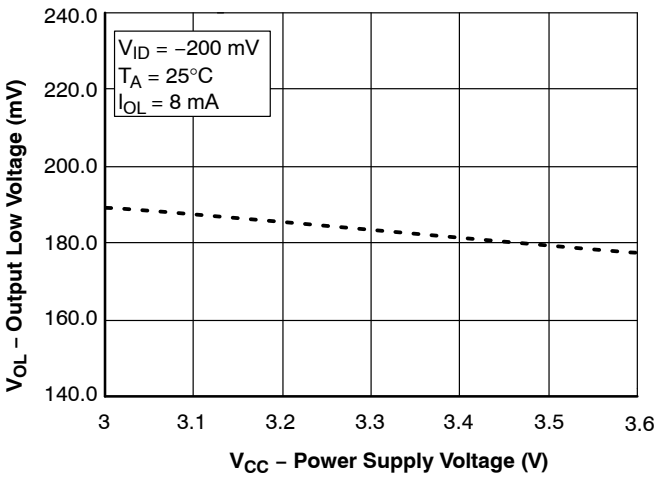


Figure 4. Output Low Voltage vs. Power Supply Voltage

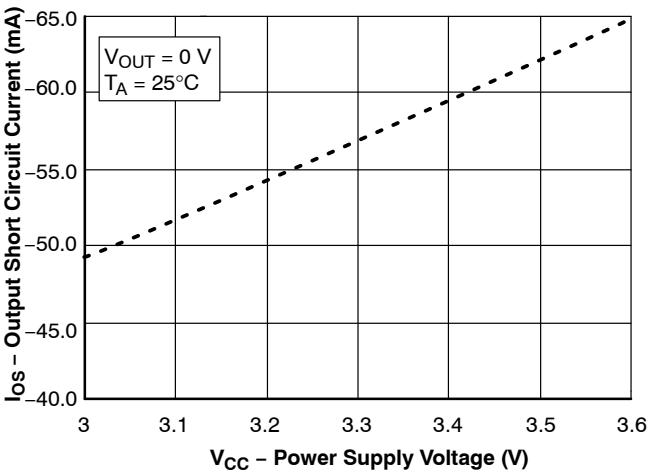


Figure 5. Output Short Circuit Current vs. Power Supply Voltage

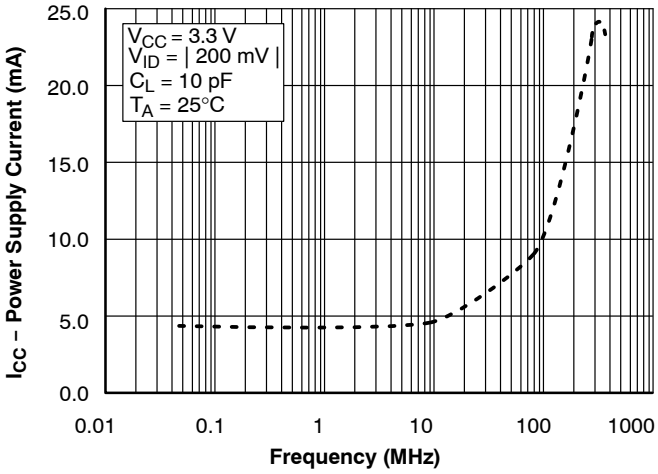


Figure 6. Power Supply Current vs. Frequency

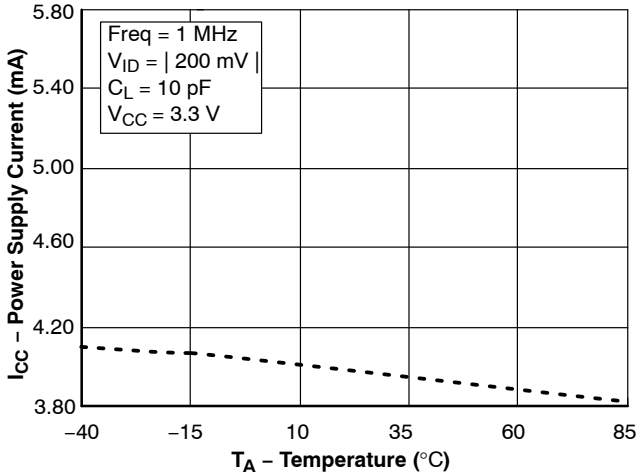


Figure 7. Power Supply Current vs. Ambient Temperature

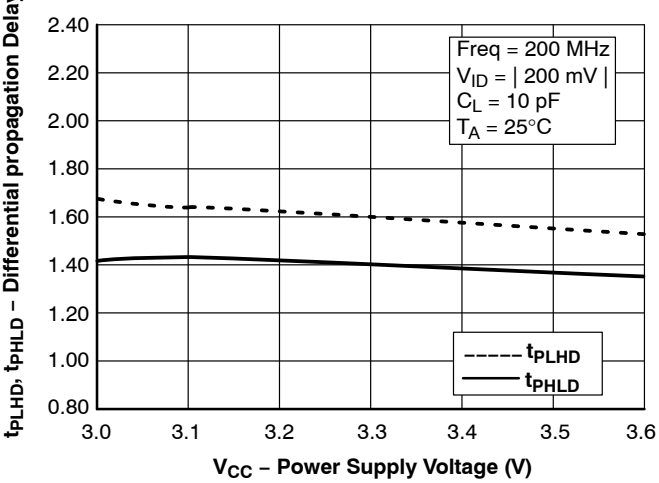


Figure 8. Differential Propagation Delay Power Supply Voltage

TYPICAL CHARACTERISTICS (continued)

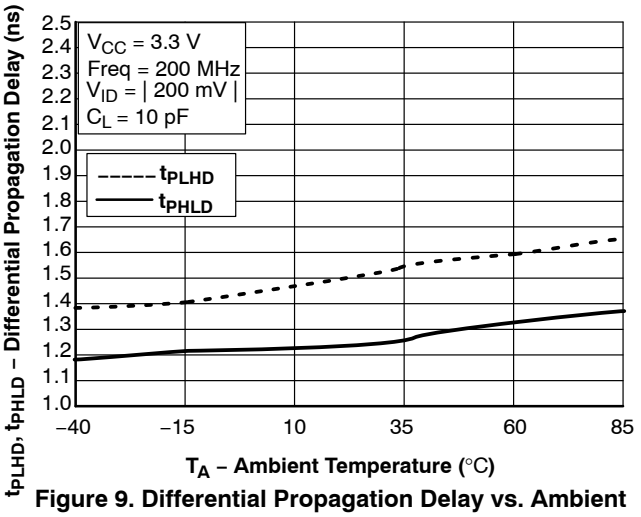


Figure 9. Differential Propagation Delay vs. Ambient Temperature

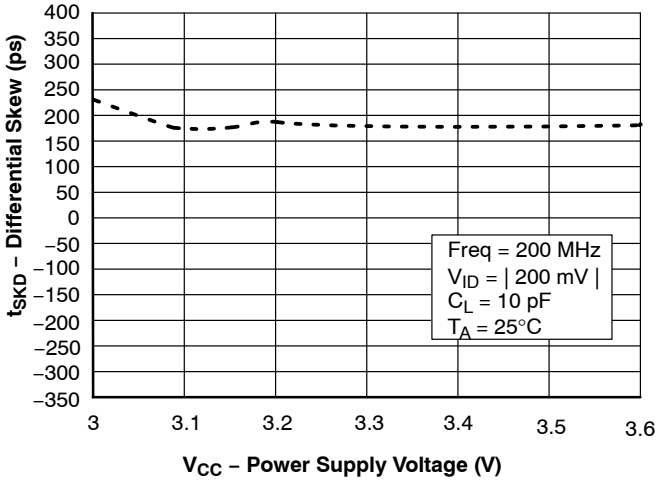


Figure 10. Differential Skew vs. Power Supply Voltage

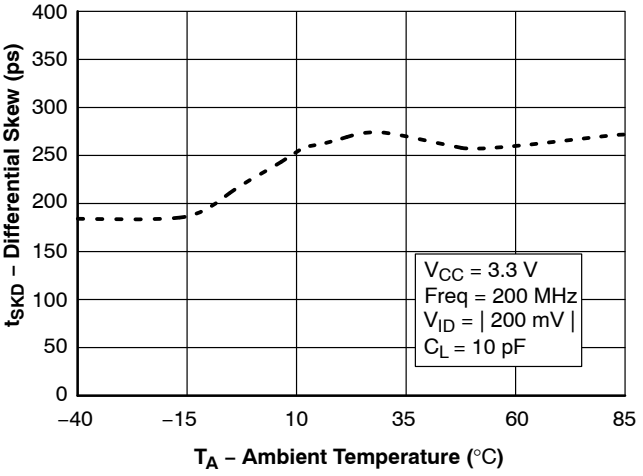


Figure 11. Differential Skew vs. Ambient Temperature

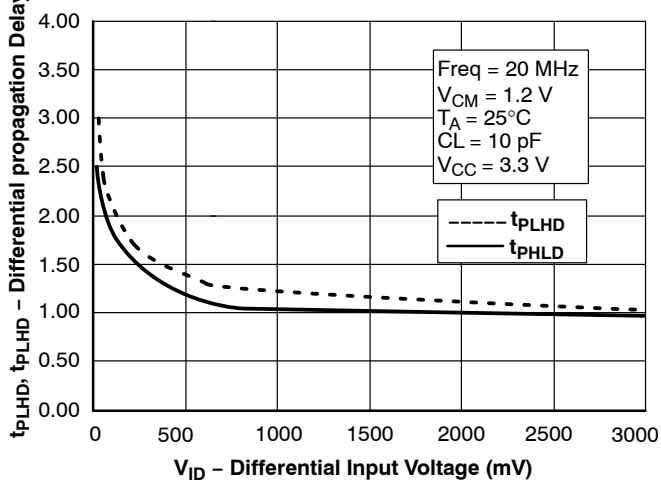


Figure 12. Differential Propagation Delay vs. Differential Input Voltage

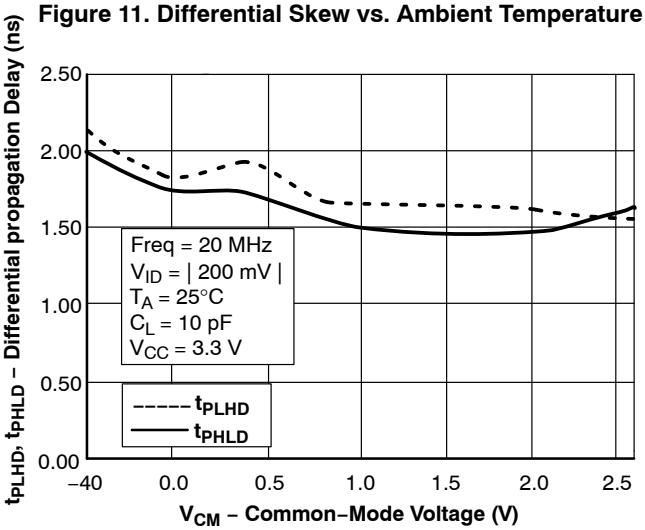


Figure 13. Differential Propagation Delay vs. Common–Mode Voltage

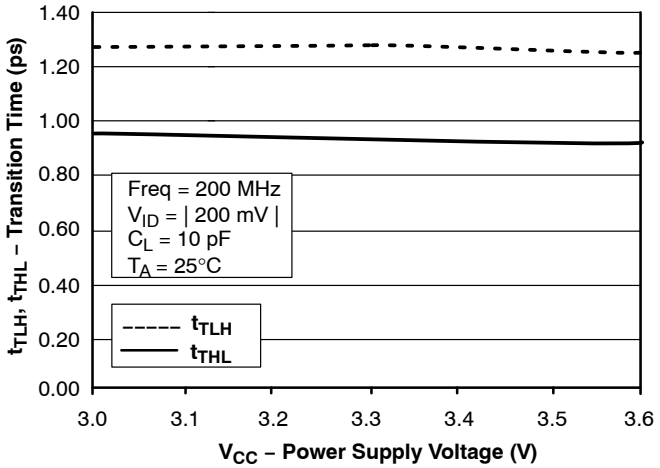


Figure 14. Transition Time vs. Power Supply Voltage

TYPICAL CHARACTERISTICS (continued)

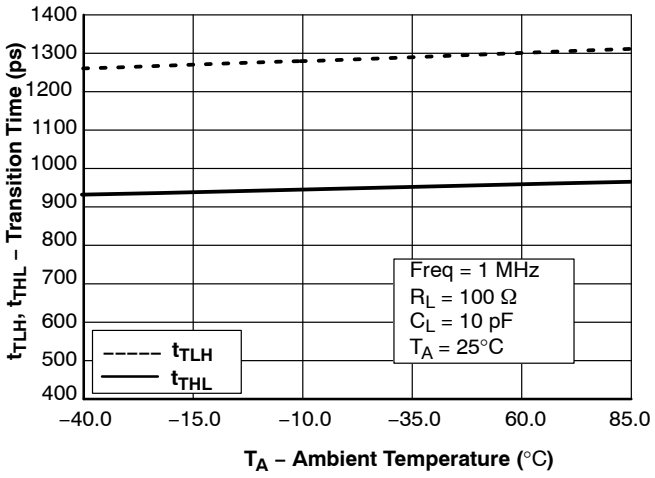


Figure 15. Transition Time vs. Ambient Temperature

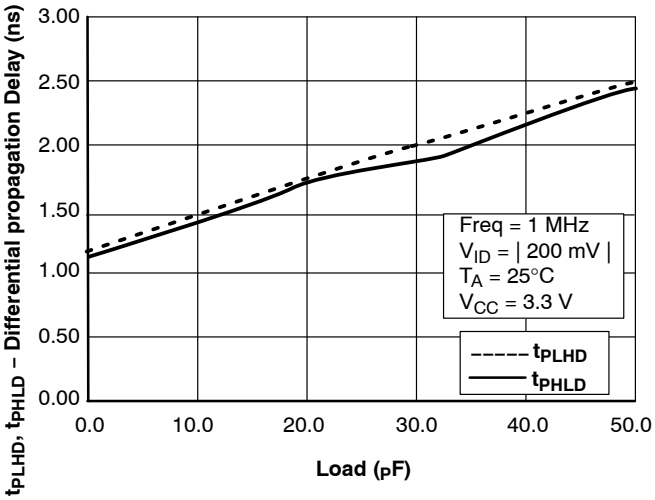


Figure 16. Differential Propagation Delay vs. Load

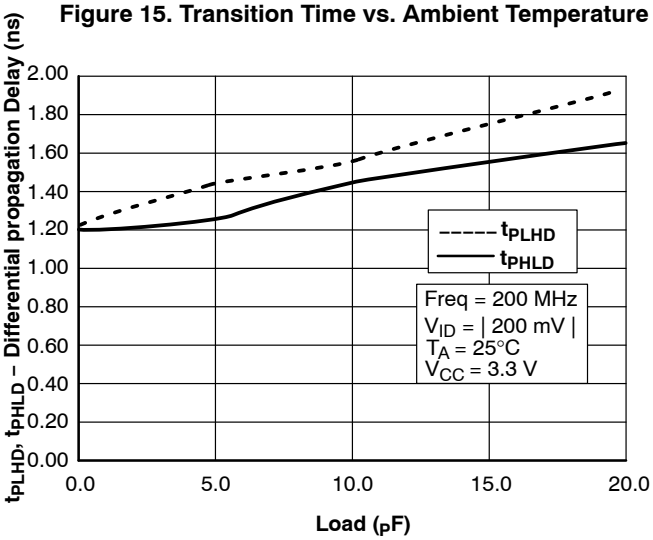


Figure 17. Differential Propagation Delay vs. Load

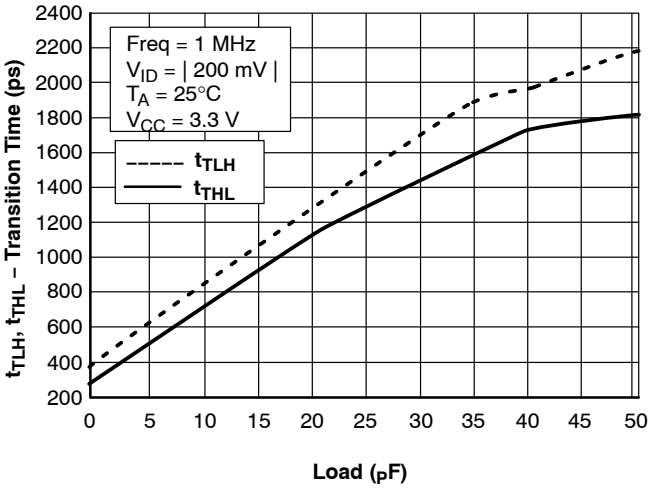


Figure 18. Transition Time vs. Load

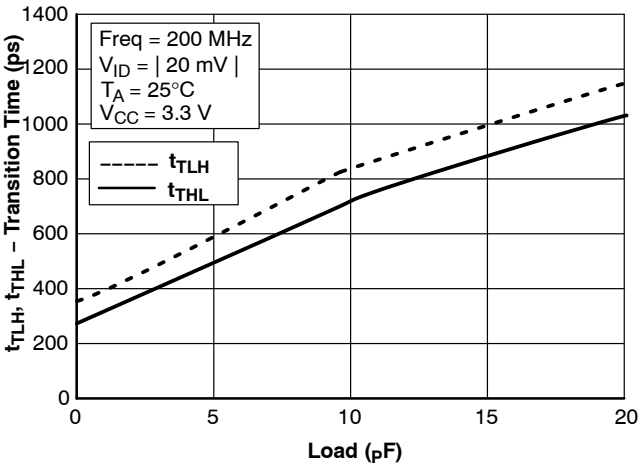


Figure 19. Transition Time vs. Load

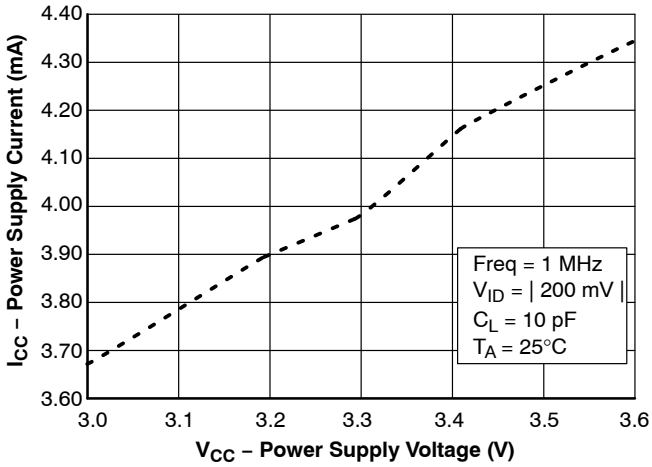
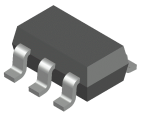


Figure 20. Power Supply Current vs. Power Supply Voltage

ORDERING INFORMATION

Product Number	Package	Shipping†
FIN1002M5X	5 Lead SOT23, JEDEC MO−178, 1.6 mm (Pb−Free)	3000 / Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



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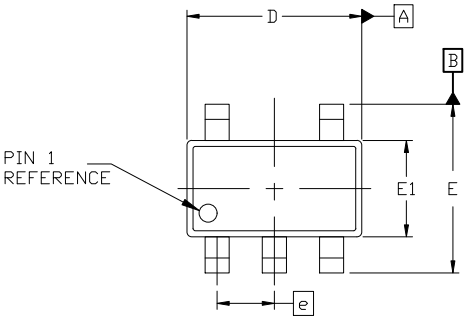
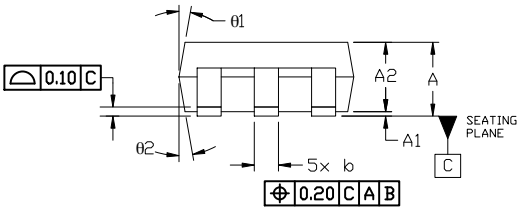
CASE 527AH
ISSUE A

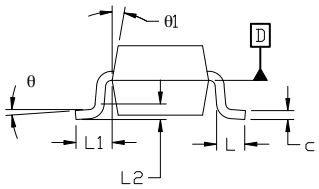
DATE 09 JUN 2021



TOP VIEW



SIDE VIEW

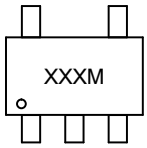


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 19894
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM D.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.

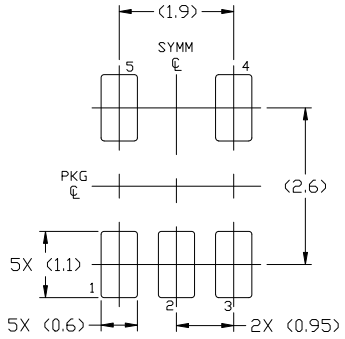
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	—	1.45
A1	0.00	—	0.15
A2	0.90	1.15	1.30
b	0.30	—	0.50
c	0.08	—	0.22
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 REF		
θ	0°	4°	8°
θ1	0°	10°	15°
θ2	0°	10°	15°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON34320E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOT−23, 5 LEAD**		**PAGE 1 OF 1**

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