

MOSFET – P-Channel POWERTRENC[®]

-12 V, -8 A, 22 mΩ

FDME905PT

General Description

This device is designed specifically for battery charging or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on-state resistance.

The MicroFET[™] 1.6x1.6 Thin package offers exceptional thermal performance for its physical size and is well suited to switching and linear mode applications.

Features

- Max $R_{DS(on)}$ = 22 mΩ at $V_{GS} = -4.5$ V, $I_D = -8$ A
- Max $R_{DS(on)}$ = 26 mΩ at $V_{GS} = -2.5$ V, $I_D = -7.3$ A
- Max $R_{DS(on)}$ = 97 mΩ at $V_{GS} = -1.8$ V, $I_D = -3.8$ A
- Low Profile: 0.55 mm Maximum in the New Package MicroFET 1.6x1.6 Thin
- Free from Halogenated Compounds and Antimony Oxides
- These Devices are Pb-Free and are RoHS Compliant

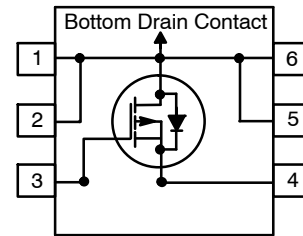
MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, Unless otherwise specified)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	-12	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	Drain Current Continuous ($T_A = 25^\circ\text{C}$) (Note 1a) Pulsed	-8 -30	A
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) (Note 1a) ($T_A = 25^\circ\text{C}$) (Note 1b)	2.1 0.7	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

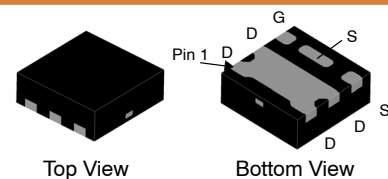
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

V_{DS}	I_D MAX	$R_{DS(on)}$ MAX
-12 V	-8 A	22 mΩ

ELECTRICAL CONNECTION

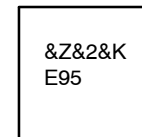


P-Channel MOSFET



MicroFET
(UDFN6)
CASE 517DV

MARKING DIAGRAM



- &Z = Assembly Plant Code
- &2 = 2-Digit Date Code (YW)
- &K = 2-Digit Lot Traceability Code
- E95 = Specific Device Code

ORDERING INFORMATION

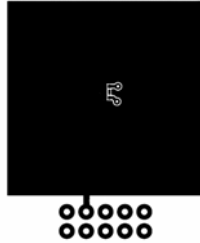
See detailed ordering and shipping information on page 2 of this data sheet.

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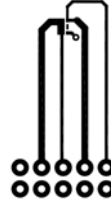
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.5	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	175	$^{\circ}\text{C/W}$

1. Repetitive rating: pulse-width limited by maximum junction temperature.



a) 60 $^{\circ}\text{C/W}$ when mounted on
a 1 in² pad of 2 oz copper



b). 175 $^{\circ}\text{C/W}$ when mounted on
a minimum pad of 2 oz copper

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size [†]	Tape Width	Quantity
E95	FDME905PT	MicroFET 1.6x1.6 Thin (Pb-Free / Halide Free)	7"	8 mm	5,000 Units

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250 \mu\text{A}$, $V_{GS} = 0 \text{ V}$	-12	-	-	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$, referenced to 25°C	-	-8.7	-	mV/ $^{\circ}\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -9.6 \text{ V}$, $V_{GS} = 0 \text{ V}$	-	-	-1	μA
I_{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = \pm 8 \text{ V}$, $V_{DS} = 0 \text{ V}$	-	-	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250 \mu\text{A}$	-0.4	-0.7	-1.0	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$, referenced to 25°C	-	2.5	-	mV/ $^{\circ}\text{C}$
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = -4.5 \text{ V}$, $I_D = -8 \text{ A}$ $V_{GS} = -2.5 \text{ V}$, $I_D = -7.3 \text{ A}$ $V_{GS} = -1.8 \text{ V}$, $I_D = -3.8 \text{ A}$, $V_{GS} = -4.5 \text{ V}$, $I_D = -8 \text{ A}$, $T_J = 125^{\circ}\text{C}$	-	18 22 28 23	22 26 97 32	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = -5 \text{ V}$, $I_D = -8 \text{ A}$	-	38	-	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = -6 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	-	1740	2315	pF
C_{oss}	Output Capacitance		-	350	525	pF
C_{rss}	Reverse Transfer Capacitance		-	311	465	pF

FDME905PT

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -6\text{ V}$, $I_D = -8\text{ A}$, $V_{GS} = -4.5\text{ V}$, $R_{GEN} = 6\ \Omega$	–	9.5	19	ns
t_r	Rise Time		–	8	16	ns
$t_{d(off)}$	Turn-Off Delay Time		–	90	144	ns
t_f	Fall Time		–	42	67	ns
Q_g	Total Gate Charge	$V_{DD} = -6\text{ V}$, $I_D = -8\text{ A}$, $V_{GS} = -4.5\text{ V}$	–	14	20	nC
Q_{gs}	Gate to Source Gate Charge		–	2.4	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	3	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = -8\text{ A}$ (Note 2)	–	–0.8	–1.2	V
		$V_{GS} = 0\text{ V}$, $I_S = -1.8\text{ A}$ (Note 2)	–	–0.7	–1.2	V
t_{rr}	Reverse Recovery Time	$I_F = -8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	–	17	31	ns
Q_{rr}	Reverse Recovery Charge		–	4.5	10	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS
($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

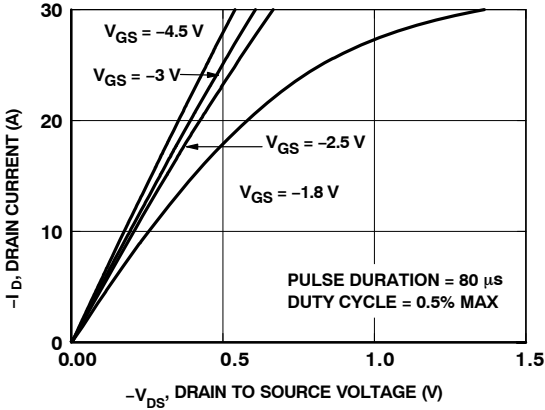


Figure 1. On-Region Characteristics

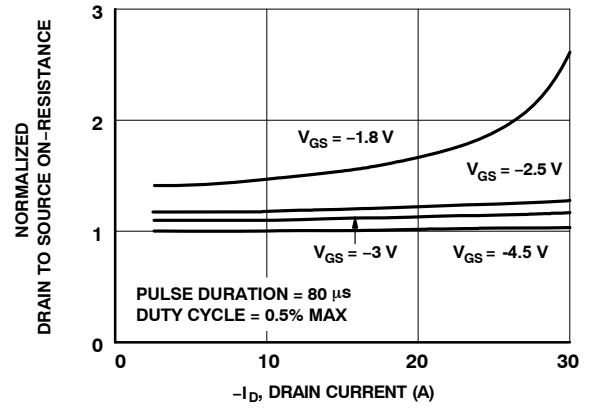


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

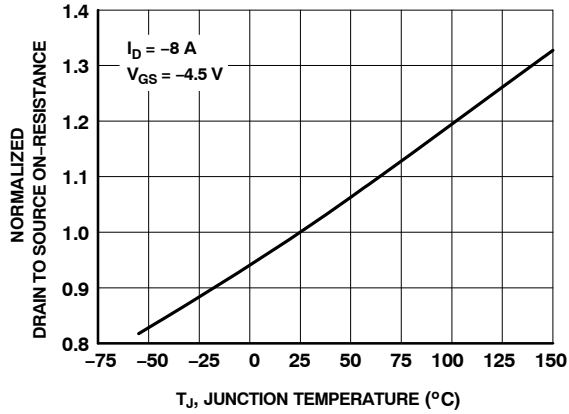


Figure 3. Normalized On-Resistance vs. Junction Temperature

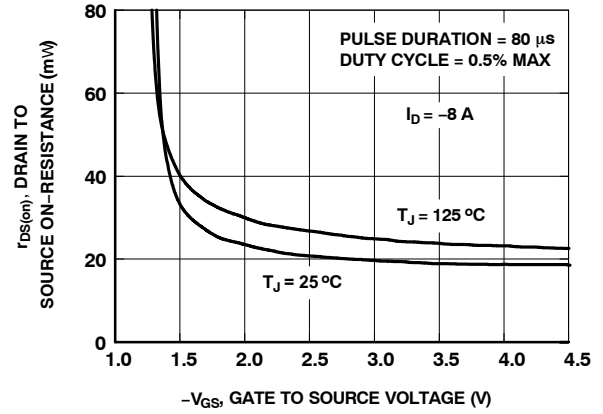


Figure 4. On-Resistance vs. Gate to Source Voltage

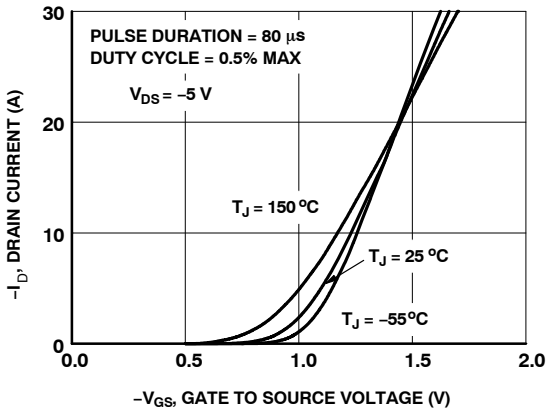


Figure 5. Transfer Characteristics

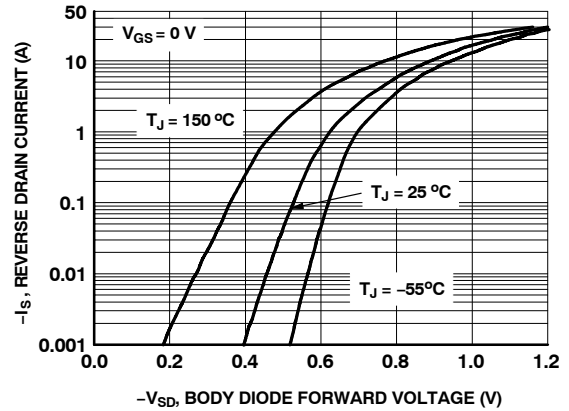


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

FDME905PT

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

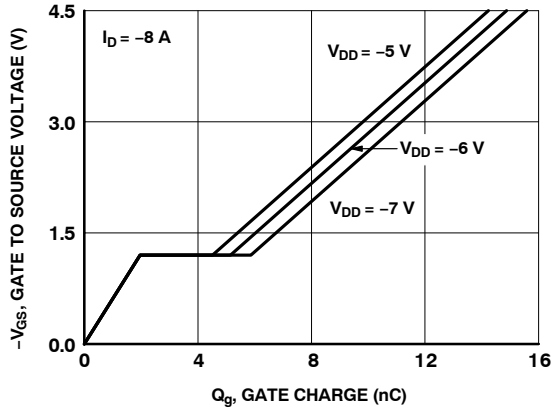


Figure 7. Gate Charge Characteristics

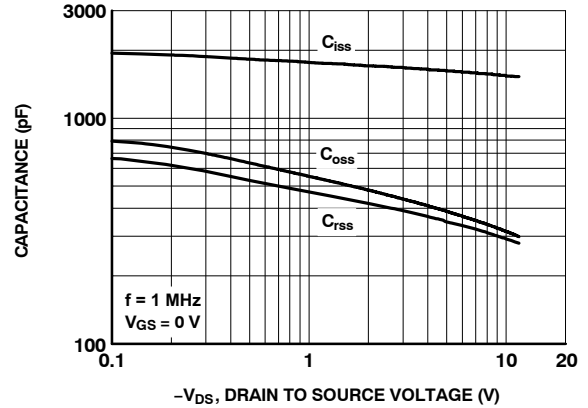


Figure 8. Capacitance vs. Drain to Source Voltage

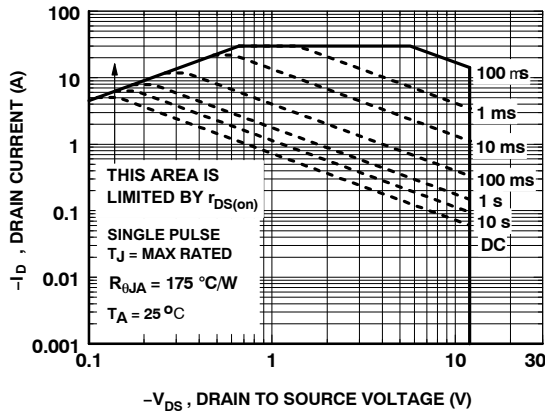


Figure 9. Forward Bias Safe Operating Area

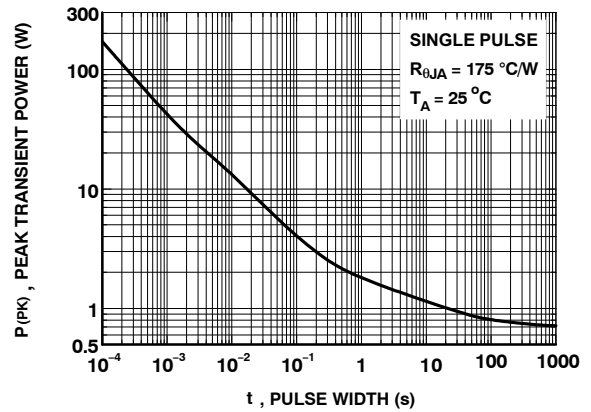


Figure 10. Single Pulse Maximum Power Dissipation

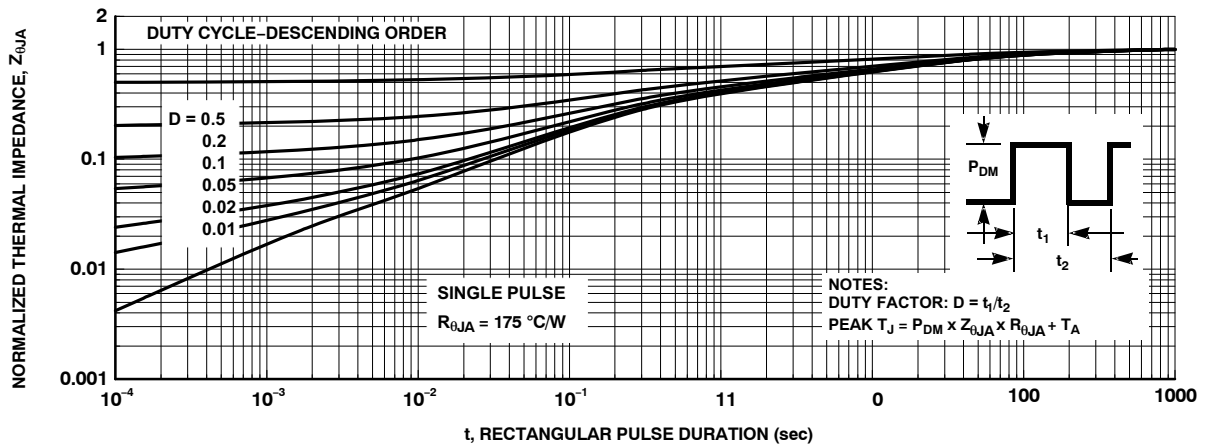
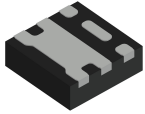


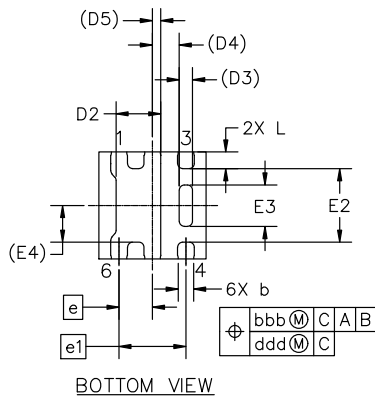
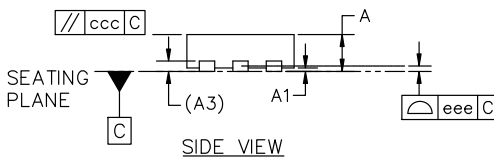
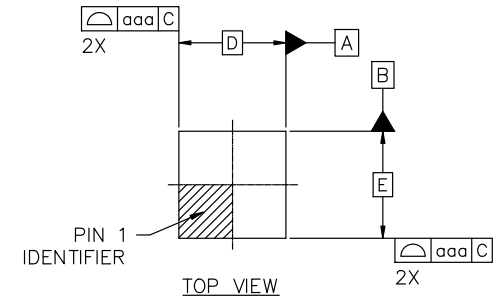
Figure 11. Junction-to-Ambient Transient Thermal Response Curve

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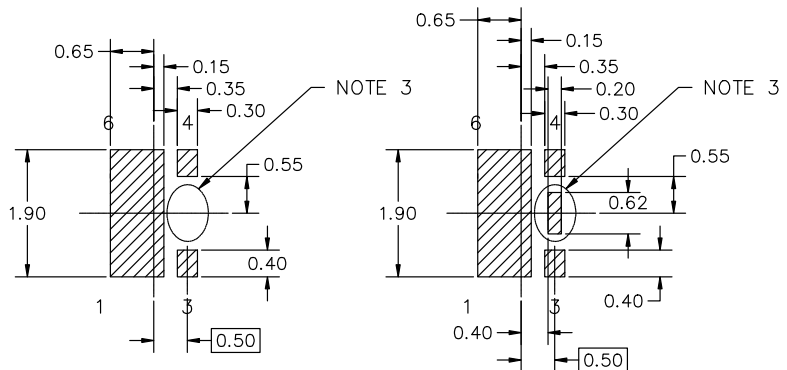
UDFN6 1.60x1.60x0.50, 0.50P
CASE 517DV
ISSUE A

DATE 31 OCT 2024



MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
A3	0.15 REF		
D	1.60 BSC		
D2	0.62	0.67	0.72
D3	0.20 REF		
D4	0.40 REF		
D5	0.125 REF		
E	1.60 BSC		
E2	1.05	1.10	1.15
E3	0.57	0.62	0.67
E4	0.55 REF		
b	0.20	0.25	0.30
e	0.50 BSC		
e1	1.00 BSC		
L	0.20	0.25	0.30

TOLERANCE FORM AND POSITION	
aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.05
eee	0.08



Option 1

Option 2

NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASMEY14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. NO VIAS OR TRACES ALLOWED IN THE AREA

RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference manual. SOLDERM/D.

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DESCRIPTION:	UDFN6 1.60x1.60x0.50, 0.50P	PAGE 1 OF 1

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