

MOSFET – N-Channel, UltraFET Trench

200 V, 9.5 A, 200 mΩ

FDMC2610

General Description

This N-Channel MOSFET is a rugged gate version of onsemi's advanced POWER trench[®] process. It has been optimized for power management applications.

Features

- Max $R_{DS(on)}$ = 200 mΩ at V_{GS} = 10 V, I_D = 2.2 A
- Max $R_{DS(on)}$ = 215 mΩ at V_{GS} = 6 V, I_D = 1.5 A
- Low Profile – 1 mm Max in a Power 33
- Pb-Free, Halide Free and RoHS Compliant

Applications

- DC-DC Conversion

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

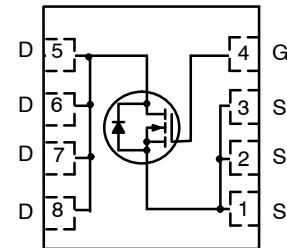
Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	200	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current: Continuous (Silicon limited) Continuous (Note 1a) Pulsed	$T_C = 25^\circ\text{C}$ 9.5 $T_A = 25^\circ\text{C}$ 2.2 15	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	6	mJ
P_D	Power Dissipation: $T_C = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$ (Note 1a)	42 2.1	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

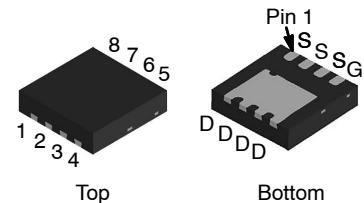
THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60	

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
200 V	200 mΩ @ 10 V	9.5 A
	215 mΩ @ 6 V	

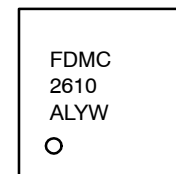


N-CHANNEL MOSFET



WDFN8 3.3 × 3.3, 0.65P
CASE 511DH

MARKING DIAGRAM



FDMC2610 = Specific Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

ORDERING INFORMATION

Device	Package	Shipping [†]
FDMC2610	WDFN8 (Pb-Free, Halide Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

FDMC2610

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	200	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C	–	199	–	$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 160\ \text{V}$, $V_{GS} = 0\ \text{V}$	–	–	1	μA
		$V_{DS} = 160\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 125^\circ\text{C}$	–	–	100	
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	2	3.2	4	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C	–	–9.9	–	$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 2.2\ \text{A}$	–	175	200	$\text{m}\Omega$
		$V_{GS} = 6\ \text{V}$, $I_D = 1.5\ \text{A}$	–	188	215	
		$V_{GS} = 10\ \text{V}$, $I_D = 2.2\ \text{A}$, $T_J = 125^\circ\text{C}$	–	347	397	
g_{FS}	Forward Transconductance	$V_{DS} = 5\ \text{V}$, $I_D = 2.2\ \text{A}$	–	7	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 100\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	–	720	960	pF
C_{oss}	Output Capacitance		–	41	55	pF
C_{rss}	Reverse Transfer Capacitance		–	12	20	pF
R_g	Gate Resistance	$f = 1\ \text{MHz}$	–	0.7	–	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100\ \text{V}$, $I_D = 2.2\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_{GEN} = 24\ \Omega$	–	17	31	ns
t_r	Rise Time		–	13	24	ns
$t_{d(off)}$	Turn-Off Delay Time		–	29	47	ns
t_f	Fall Time		–	16	29	ns
$Q_{g(TOT)}$	Total Gate Charge at 10 V	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$, $V_{DD} = 100\ \text{V}$, $I_D = 2.2\ \text{A}$	–	12.3	18	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 100\ \text{V}$, $I_D = 2.2\ \text{A}$	–	3	–	nC
Q_{gd}	Gate to Drain "Miller" Charge	$V_{DD} = 100\ \text{V}$, $I_D = 2.2\ \text{A}$	–	3.6	–	nC

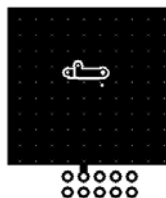
DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = 2.2\ \text{A}$ (Note 2)	–	0.8	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 2.2\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$	–	69	104	ns
Q_{rr}	Reverse Recovery Charge		–	114	171	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a $1\ \text{in}^2$ oz copper pad on a $1.5 \times 1.5\ \text{in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



- a) $60^\circ\text{C}/\text{W}$ when mounted on a $1\ \text{in}^2$ pad of 2 oz copper.



- b) $135^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width $< 300\ \mu\text{s}$, Duty cycle $< 2.0\%$.
- Starting $T_J = 25^\circ\text{C}$; N-ch: $L = 3\ \text{mH}$, $I_{AS} = 2\ \text{A}$, $V_{DD} = 200\ \text{V}$, $V_{GS} = 10\ \text{V}$.

TYPICAL CHARACTERISTICS

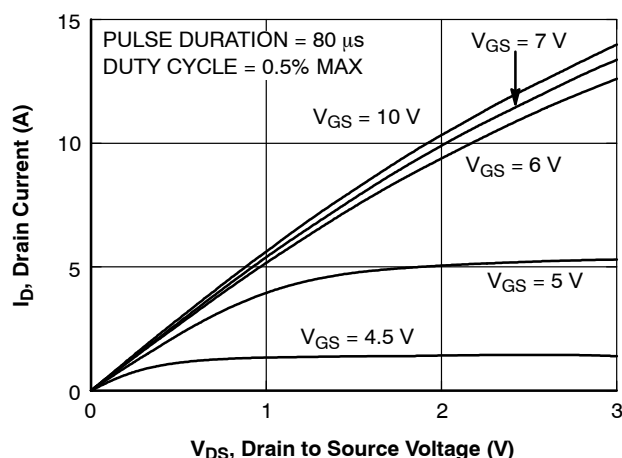
(T_J = 25°C unless otherwise noted)

Figure 1. On-Region Characteristics

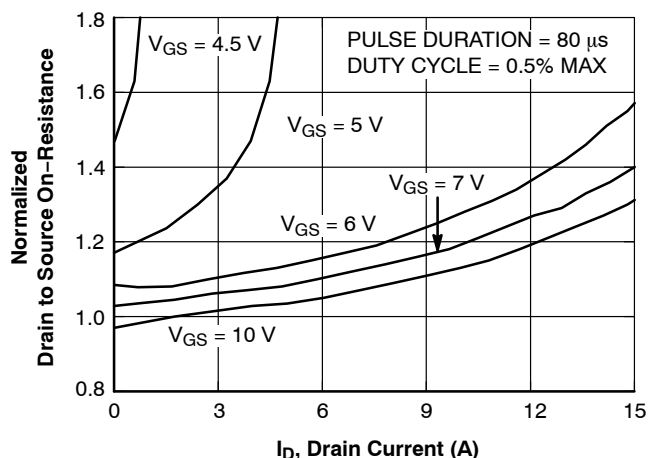


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

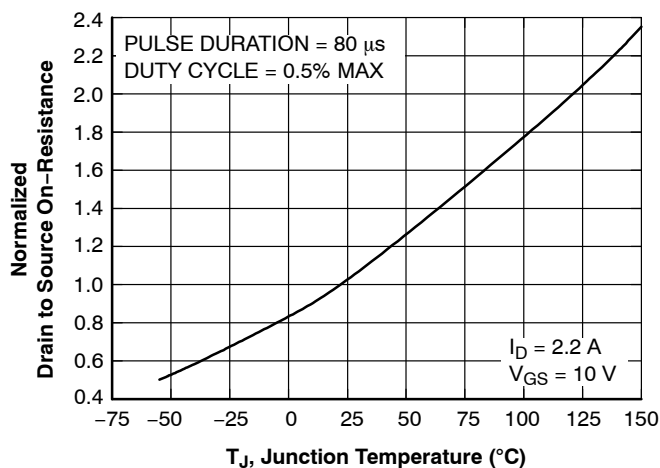


Figure 3. Normalized On-Resistance vs. Junction Temperature

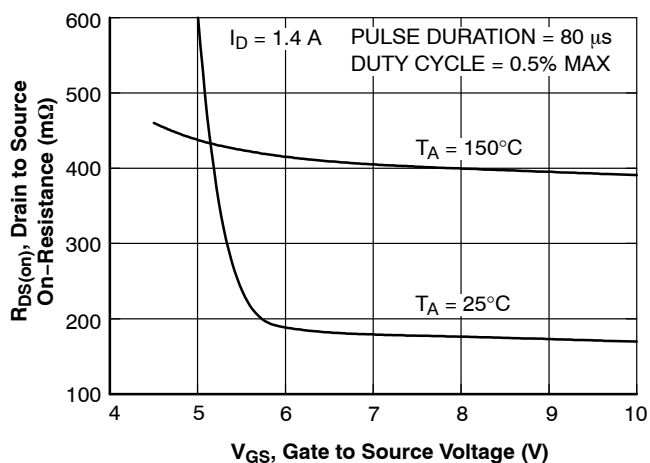


Figure 4. On-Resistance vs. Gate to Source Voltage

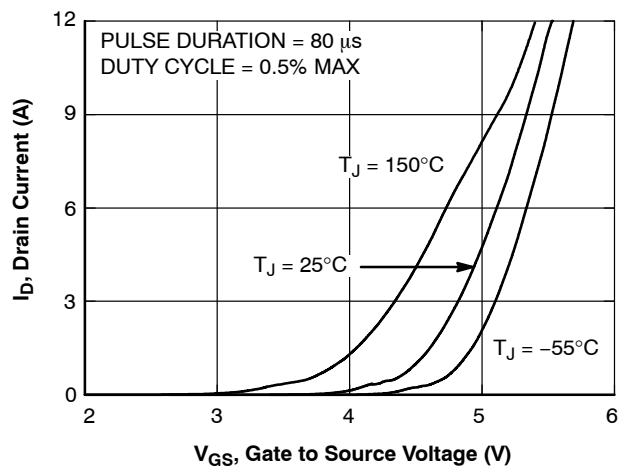


Figure 5. Transfer Characteristics

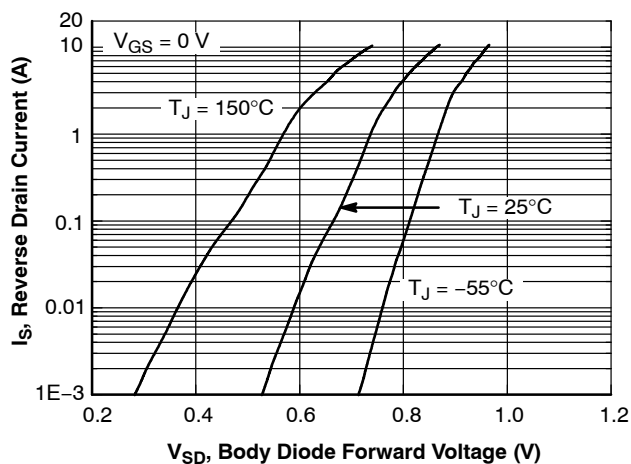


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

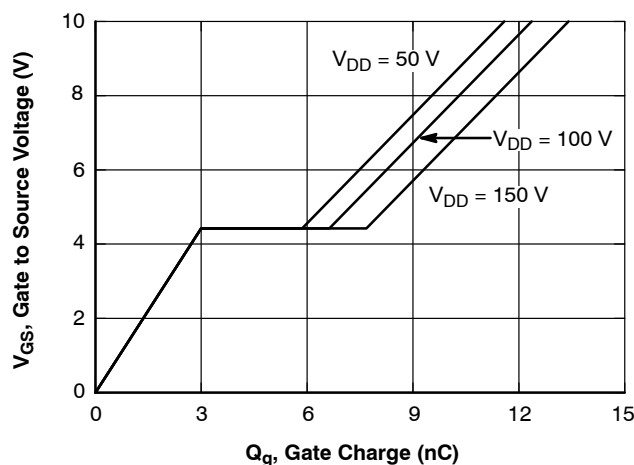


Figure 7. Gate Charge Characteristics

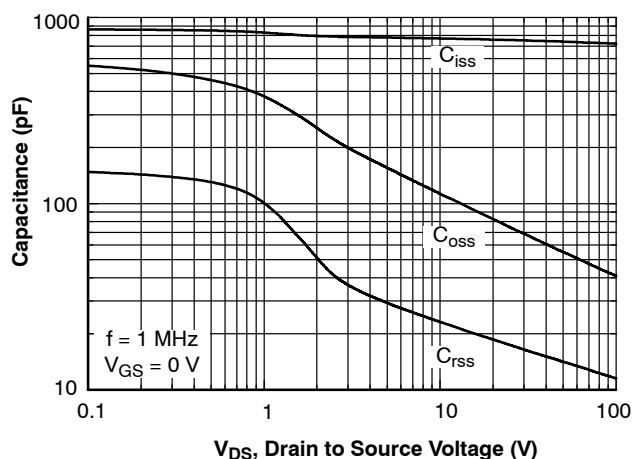


Figure 8. Capacitance vs. Drain to Source Voltage

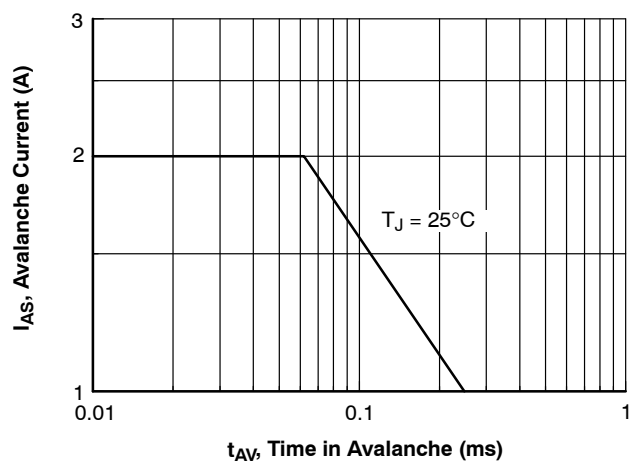


Figure 9. Unclamped Inductive Switching Capability

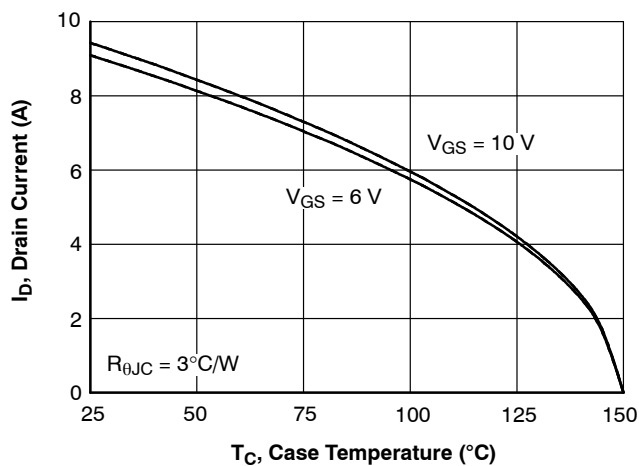


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

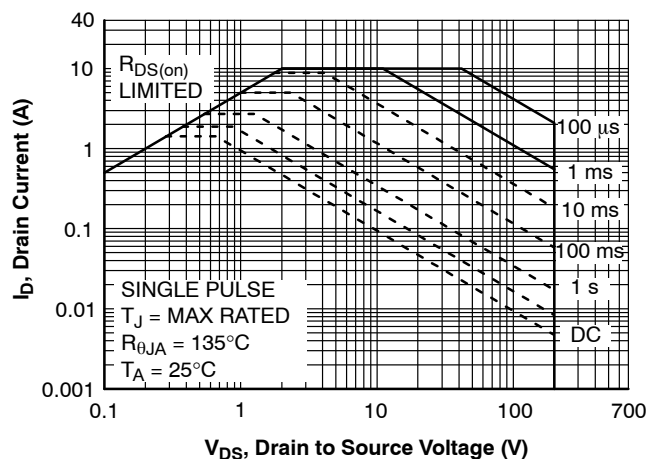


Figure 11. Forward Bias Safe Operating Area

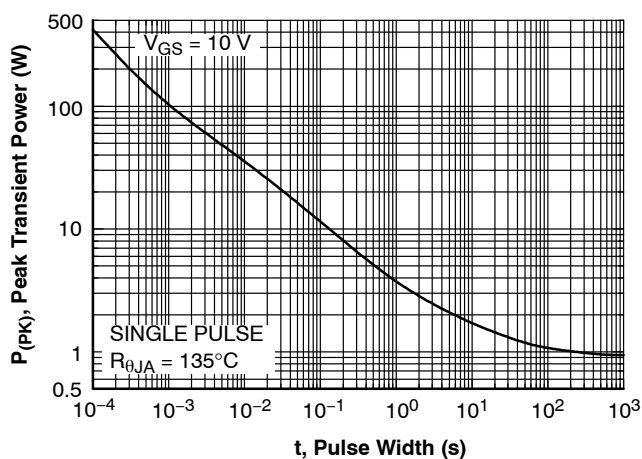


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

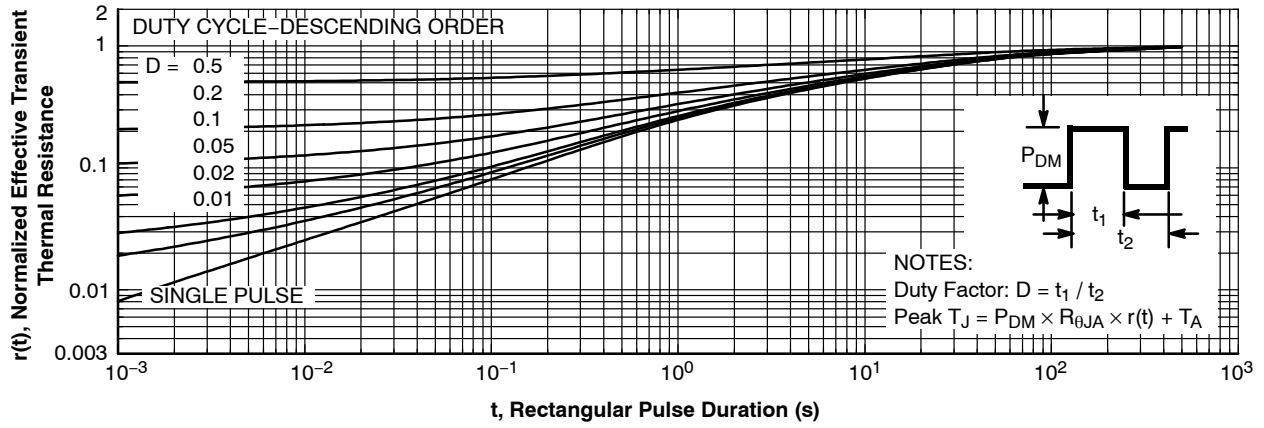
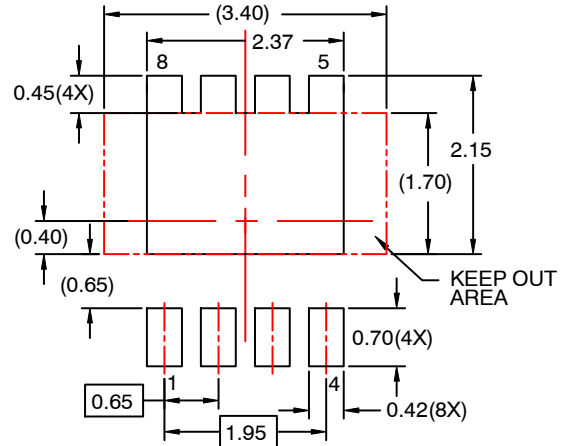
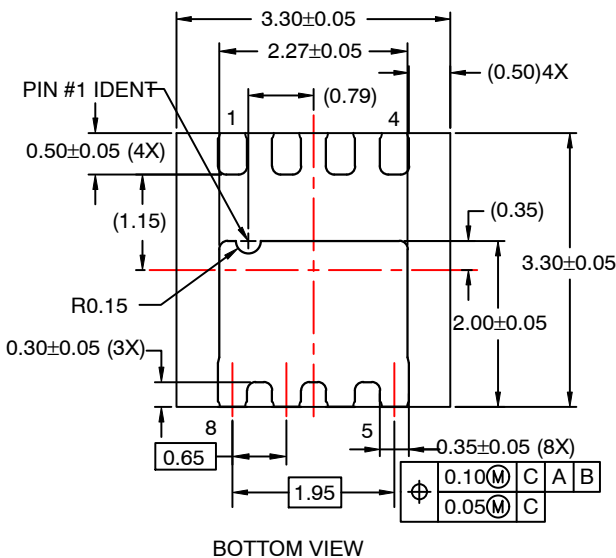
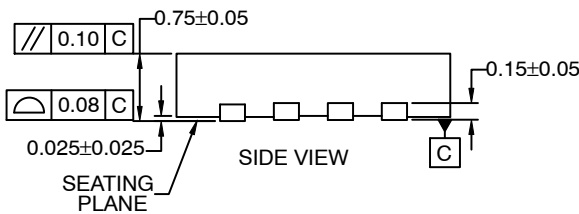
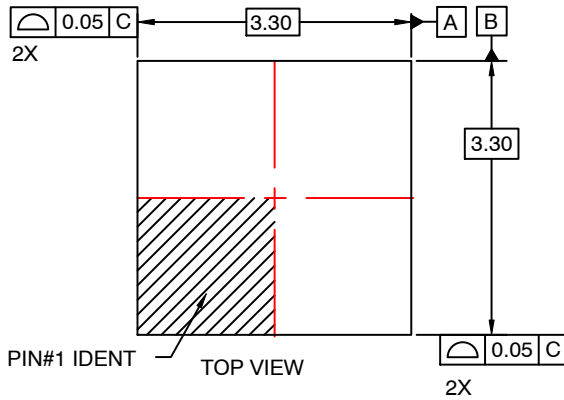


Figure 13. Transient Thermal Response Curve

WDFN8 3.3x3.3, 0.65P
CASE 511DH
ISSUE O

DATE 31 JUL 2016



RECOMMENDED LAND PATTERN

NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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