

MOSFET - N-Channel, SUPERFET® II, FRFET® 650 V, 41 mΩ, 76 A

FCH041N65F-F085

Description

SuperFET II Mosfet is onsemi's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very well suited for the Soft switching and Hard Switching topologies like High Voltage Full Bridge and Half Bridge DC-DC, Interleaved Boost PFC, Boost PFC for HEV-EV automotive.

SuperFET II FRFET MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.

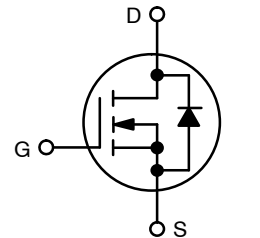
Features

- Typ. $R_{DS(on)}$ = 34 mΩ at V_{GS} = 10 V, I_D = 38 A
- Typ. $Q_{g(tot)}$ = 234 nC at V_{GS} = 10 V, I_D = 38 A
- UIS Capability
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

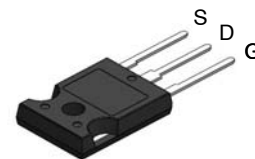
Applications

- Automotive On Board Charger
- Automotive DC/DC Converter for HEV

V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
650 V	41 mΩ @ 10 V	76 A

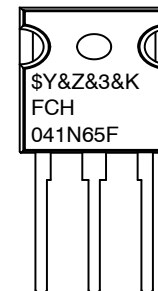


N-CHANNEL MOSFET



TO-247-3LD
CASE 340CK

MARKING DIAGRAM



\$Y	= onsemi Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FCH041N65F	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FCH041N65F–F085

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		Value	Unit
V _{DSS}	Drain-to-Source Voltage		650	V
V _{GSS}	Gate-to-Source Voltage		±20	V
I _D	Drain Current – Continuous (V _{GS} = 10) (Note 1)	T _C = 25°C	76	A
		T _C = 100°C	48	A
	Pulsed Drain Current		See Fig. 4	A
E _{AS}	Single Pulsed Avalanche Rating (Note 2)		2025	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		50	
P _D	Power Dissipation		595	W
	Derate Above 25°C		4.76	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 15 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 38 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 380 V, starting T_J = 25°C.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCH041N65F	FCH041N65F–F085	TO-247–3	–	–	30 Units

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction-to-Case, Max.	0.21	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient, Max. (Note 4)	40	

4. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2 oz copper.

FCH041N65F–F085

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain-to-Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	650	–	–	V
I _{DSS}	Drain-to-Source Leakage Current	V _{DS} = 650 V, V _{GS} = 0 V, T _J = 25°C	–	–	10	μA
		V _{DS} = 650 V, V _{GS} = 0 V, T _J = 150°C (Note 5)	–	–	1	mA
I _{GSS}	Gate-to-Source Leakage Current	V _{GS} = ±20 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	3	–	5	V
R _{DS(on)}	Drain-to-Source On Resistance	I _D = 38 A, V _{GS} = 10 V, T _J = 25°C	–	34	41	mΩ
		I _D = 38 A, V _{GS} = 10 V, T _J = 150°C (Note 5)	–	80	96	

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	–	10200	13566	pF
C _{oss}	Output Capacitance		–	10529	14004	
C _{rss}	Reverse Transfer Capacitance		–	227	–	
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 520 V, V _{GS} = 0 V	–	843	–	pF
R _g	Gate Resistance	f = 1 MHz	–	0.5	–	Ω
Q _{g(tot)}	Total Gate Charge	V _{DD} = 380 V, I _D = 38 A, V _{GS} = 10 V	–	234	304	nC
Q _{g(th)}	Threshold Gate Charge		–	17	22	
Q _{gs}	Gate-to-Source Gate Charge		–	50	–	
Q _{gd}	Gate-to-Drain “Miller” Charge		–	90	–	

SWITCHING CHARACTERISTICS

t _{on}	Turn-On Time	V _{DD} = 380 V, I _D = 38 A, V _{GS} = 10 V, R _G = 4.7 Ω	–	94	207	ns
t _{d(on)}	Turn-On Delay Time		–	55	–	
t _r	Turn-On Rise Time		–	39	–	
t _{d(off)}	Turn-Off Delay Time		–	183	–	
t _f	Turn-Off Fall Time		–	8	–	
t _{off}	Turn-Off Time		–	191	402	

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source-to-Drain Diode Voltage	V _{GS} = 0 V, I _{SD} = 38 A	–	–	1.2	V
t _{rr}	Reverse Recovery Time	V _{DD} = 480 V, I _F = 38 A, di _{SD} /dt = 100 A/μs	–	235	–	ns
Q _{rr}	Reverse Recovery Charge		–	2	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. The maximum value is specified by design at T_J = 150°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

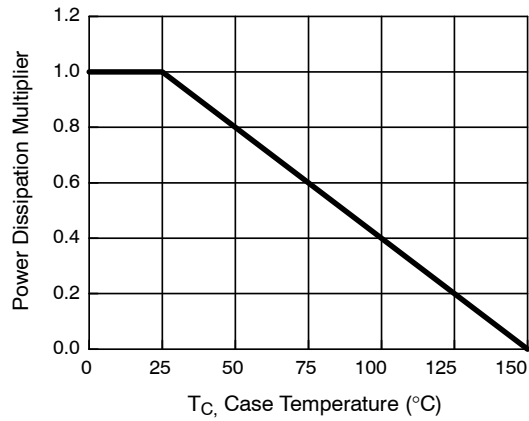


Figure 1. Normalized Power Dissipation vs. Case Temperature

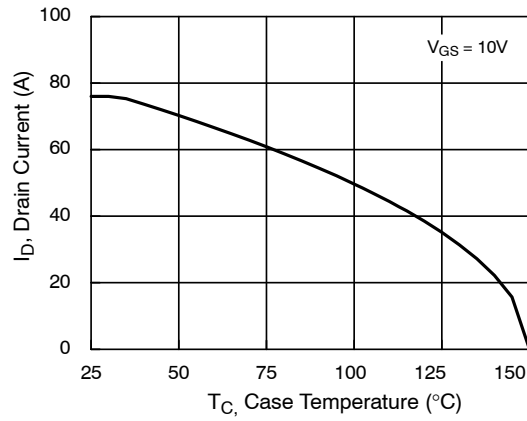


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

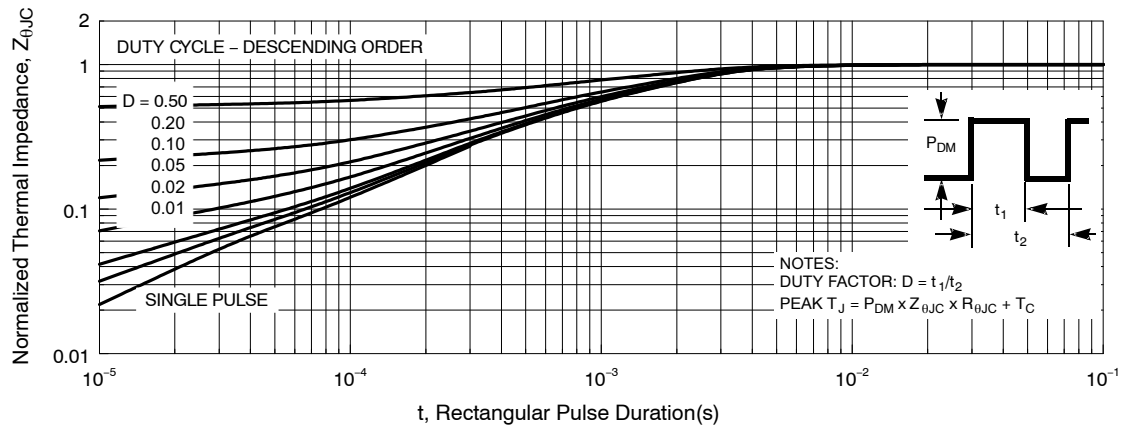


Figure 3. Normalized Maximum Transient Thermal Impedance

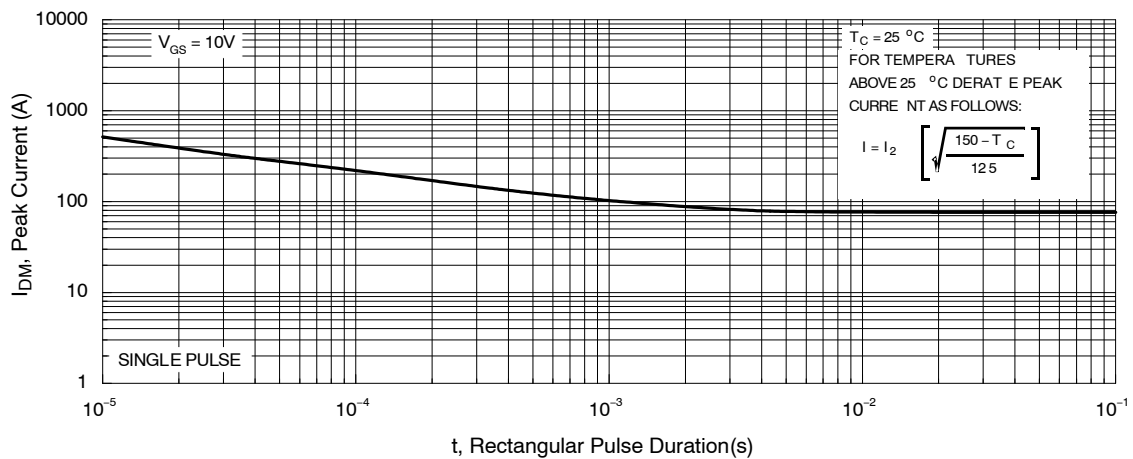


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

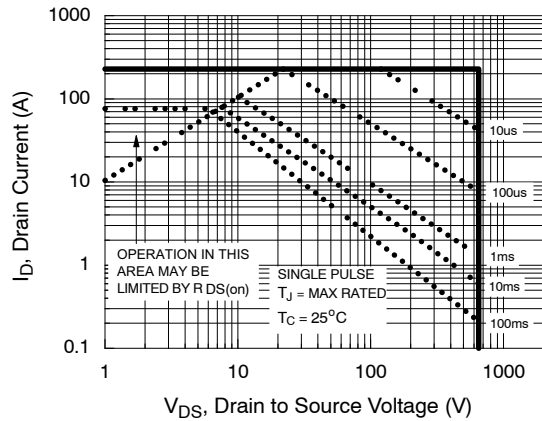


Figure 5. Forward Bias Safe Operating Area

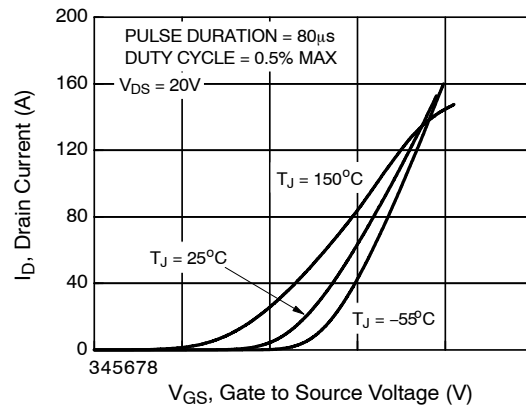


Figure 6. Transfer Characteristics

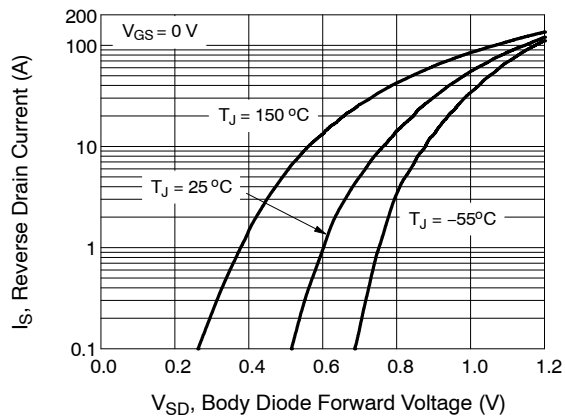


Figure 7. Forward Diode Characteristics

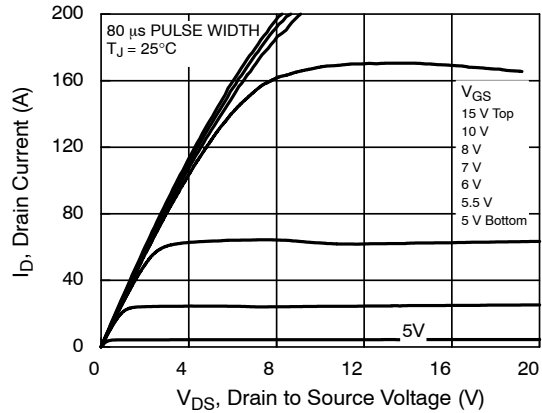


Figure 8. Saturation Characteristics

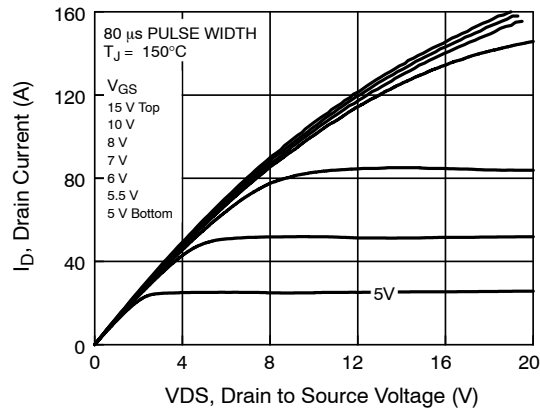
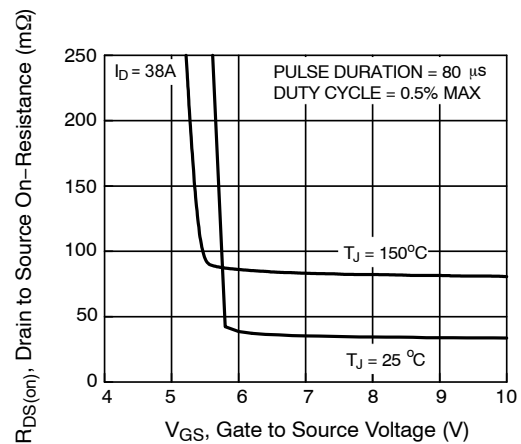


Figure 9. Saturation Characteristics

Figure 10. $R_{DS(on)}$ vs. Gate Voltage

TYPICAL CHARACTERISTICS

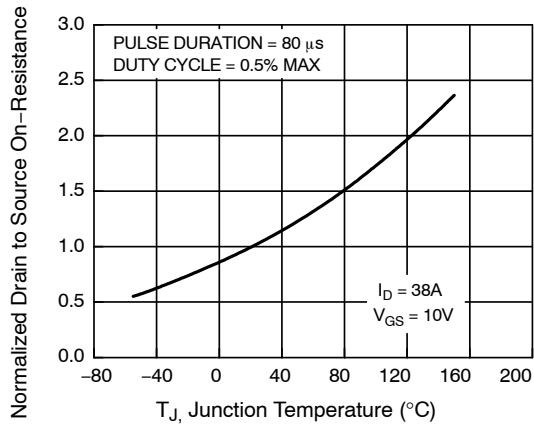
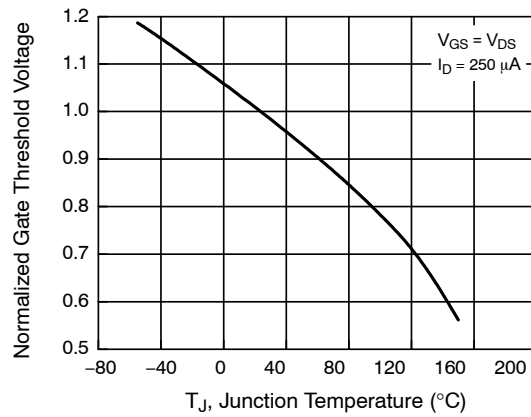
Figure 11. Normalized $R_{DS(on)}$ vs. Junction Temperature

Figure 12. Normalized Gate Threshold Voltage vs. Temperature

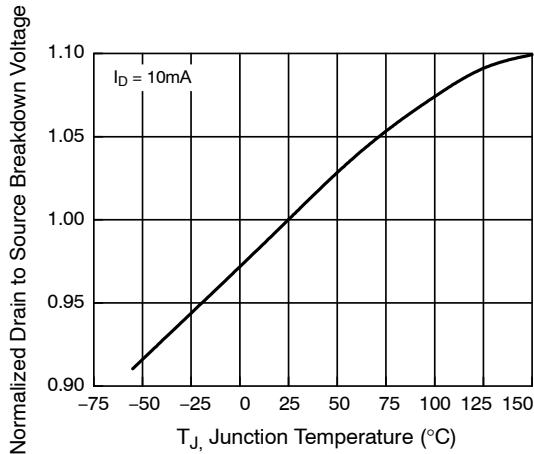


Figure 13. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

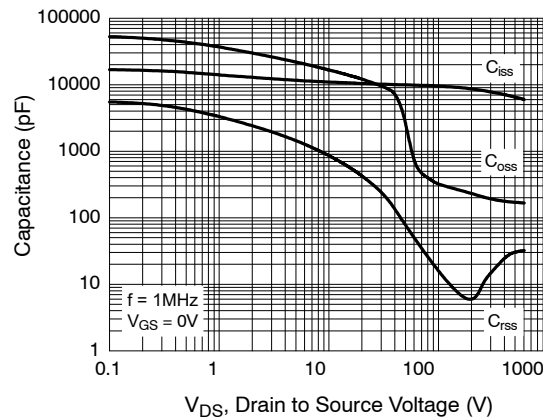


Figure 14. Capacitance vs. Drain to Source Voltage

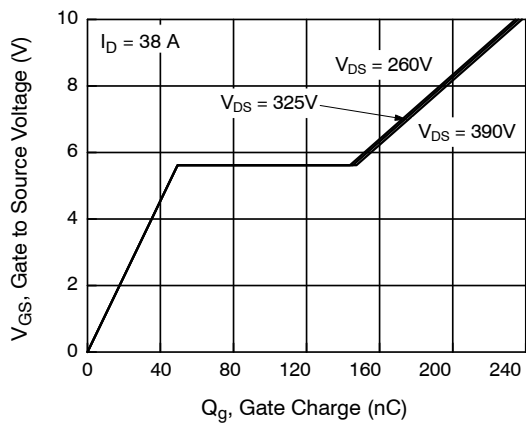
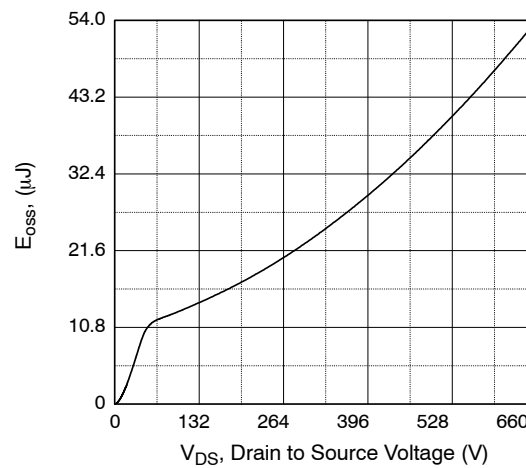


Figure 15. Gate Charge vs. Gate to Source Voltage

Figure 16. E_{oss} vs. Drain to Source Voltage

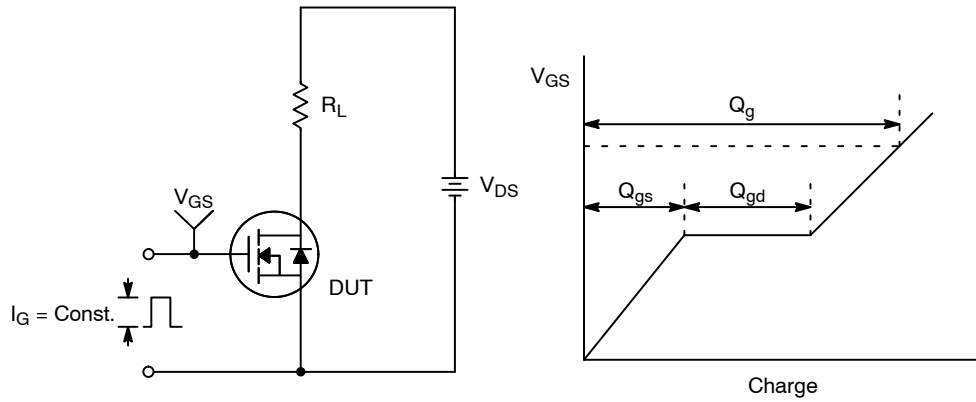


Figure 17. Gate Charge Test Circuit & Waveform

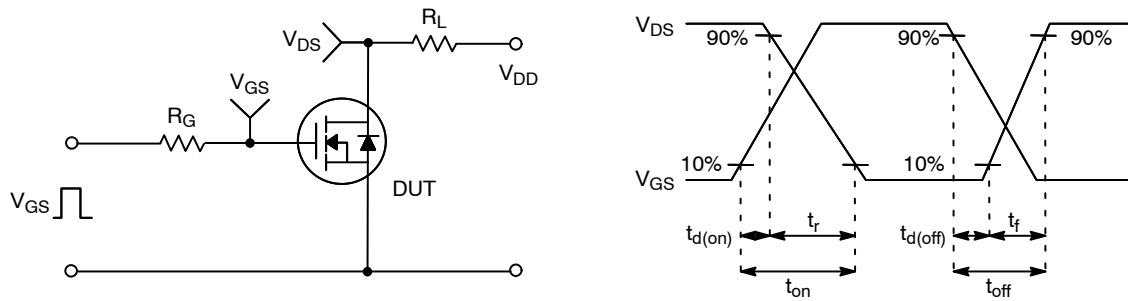


Figure 18. Resistive Switching Test Circuit & Waveforms

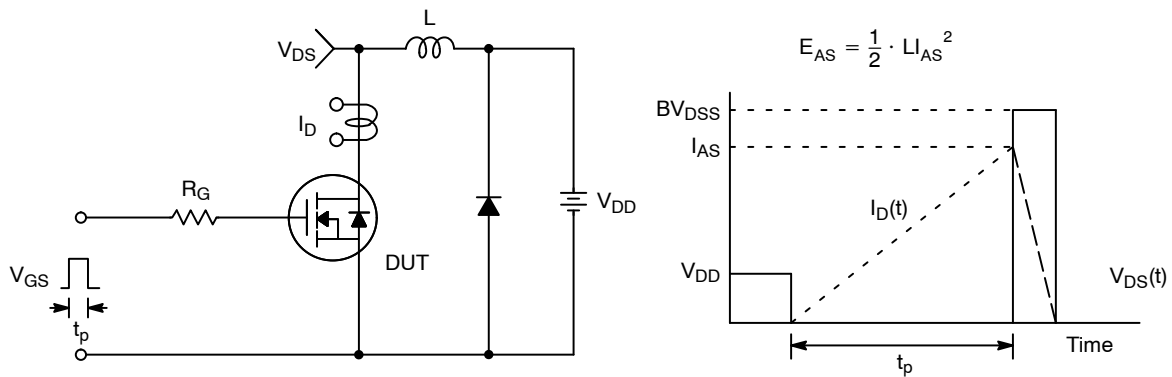


Figure 19. Unclamped Inductive Switching Test Circuit & Waveforms

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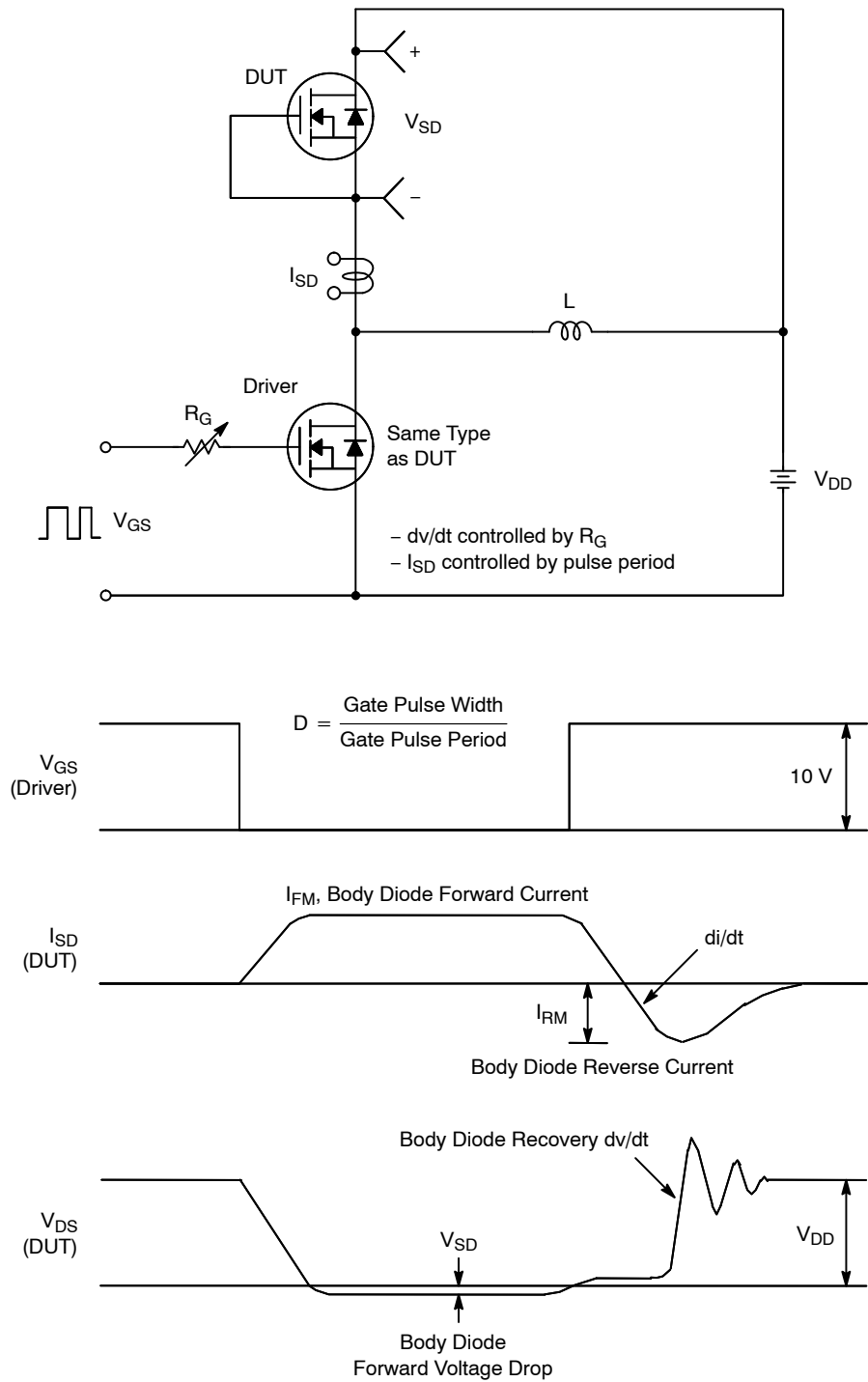


Figure 20. Peak Diode Recovery dv/dt Test Circuit & Waveforms

TO-247-3LD SHORT LEAD
CASE 340CK
ISSUE A

DATE 31 JAN 2019



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC
MARKING DIAGRAM*


XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ϕP	3.51	3.58	3.65
$\phi P1$	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

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