NB3N1900K Evaluation Board User's Manual

NB3N1900KMNGEVB

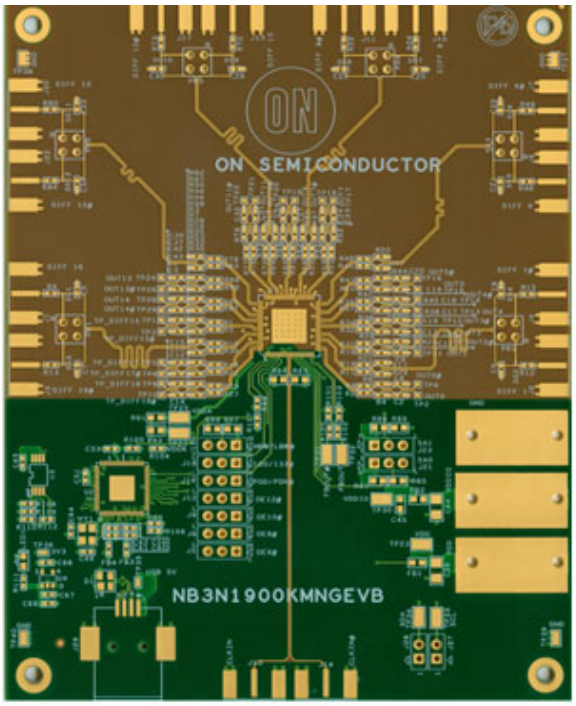
Introduction

The NB3N1900KMNGEVB evaluation boards were developed for the NB3N1900K (HCSL) devices. This evaluation board was designed to provide a flexible and convenient platform to quickly evaluate, characterize and verify the operation of the NB3N1900K devices.

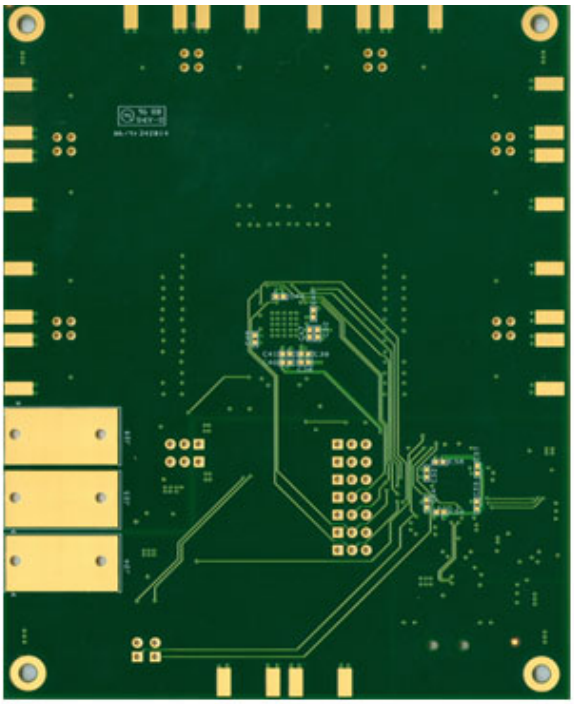
This evaluation board manual contains:

- Information on the NB3N1900K Evaluation Board
- Assembly Instructions
- Test and Measurement Setup Procedures
- Board Schematic and Bill of Materials

This manual should be used in conjunction with the device datasheet which contains full technical details on the device specifications and operation.



(Top View)



(Bottom View)

Figure 1. NB3N1900KMNGEVB Evaluation Board

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BOARD FEATURES

Single Board Design/Layout

- Accommodates the Electrical Characterization of the NB3N1900K (HCSL Outputs)
- Incorporates On-board I²C/SMBus Interface Circuitry Powered from a USB Connection, Minimizing Cabling
- Convenient and Compact Board Layout
- 3.3 V Power Supply Device Operation
- Differential Inputs/Outputs Signals are Accessed via SMA Connectors or High Impedance Probes

Other Board Features

There are no vias on the high-speed differential I/O metal traces so as to eliminate via impedance and stub affects. Board stand-offs are installed.

Board Layout

The NB3N1900K QFN−72 Evaluation Board provides a high bandwidth, 50-Ω controlled trace impedance environment (100-Ω line-to-line differential) and is implemented in four layers.

- All Layers are Constructed with FR4 Dielectric Material
- The First Layer is the Primary Signal Layer, Including All of the Differential Inputs and Outputs
- The Second Layer is the Ground Plane. It is Dedicated for the DUT Ground/SMA Ground Plane
- The Third Layer is Dedicated as the Power Plane. A Portion of this 3rd Layer is Designated for the Device VDD and VDDIO Power Planes
- The Fourth Layer Contains Control Lines, Power Supply Banana Jacks and Device Power Pin By-pass Capacitors

Layer Stack

- L1 (Top) Signal
- L2 Device Ground and SMA Ground
- L3 VDD, VDDIO (Separate Device Power Supplies)
- L4 (Bottom), Power Supply By-pass Capacitors, Control Pin Traces and Banana Jacks

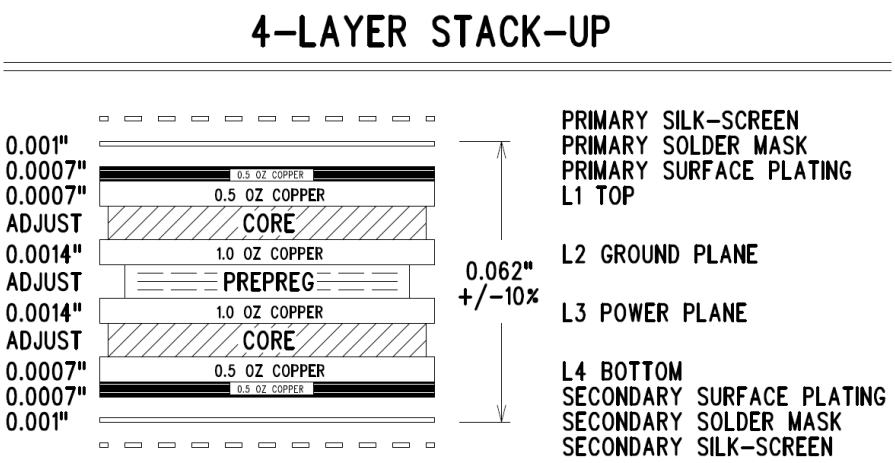


Figure 2. NB3N1900KMNGEVB Evaluation Board Layer Stack-Up

Power Supplies

Each VDD, VDDIO and GND power supply has a separate side-launch banana jack located on bottom side.

This board is capable of measuring device IDD & IDDIO separately.

Board Layer #2 = SMA Ground = Device GND = 0 V.

GND Banana Jack = negative power supply for DUTGND and SMAGND.

Exposed Pad (EP): The exposed pad footprint on the board is soldered to the exposed pad of the QFN−72 package, and is electrically connected to GND power supply.

Board Layer #3 = VDD and VDDIO Power Supplies

VDD = positive power supply for core and inputs; VDD/VDDA/VDDR (pins #1, 8)

VDDIO = positive power supply for outputs; VDDIO (pins #21, 31, 45, 58, 68)

VDD & VDDIO have the power supply filtering per datasheet by the banana jacks.

All VDD/VDDA/VDDR/VDDIO device pins have a 0.1 μF bypass capacitor installed on top side next to package pins.

Control Pins

Each control pin can be managed manually with a H/L jumper header; H = VDD, L = GND.

Tri-Level Input Pins – HBW_BYP_LBW#, SA_0 and SA_1

The three tri-level input pins, HBW_BYPASS_LBW#, SA0 and SA1, have selectable (with jumper) 4.7 kΩ pull-up to VDD and 4.7 kΩ pull-down to GND resistors; No jumper defaults to open/float.

- For a HIGH Level – Put Jumper to High
- For a LOW Level – Put Jumper to Low
- For a MID Level – Put Jumper to both High and Low; this will Enable both Pull-up and Pull-down Resistors

HBW_BYP_LBW#

At J16 header, there is a 4.7 kΩ pull-up to VDD and a 4.7 kΩ pull-down resistor to GND for manual control.

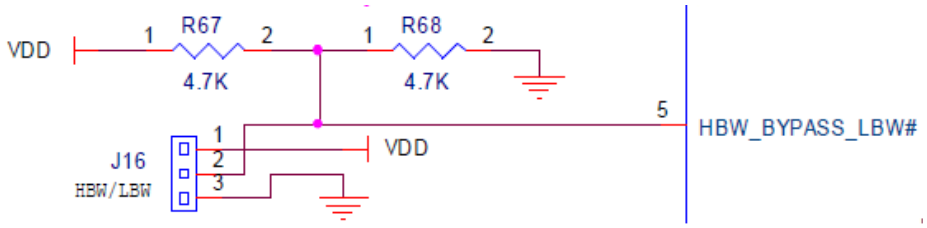


Figure 3. HBW_BYP_LBW# Schematic Configuration

SA_0 & SA_1

At J21 and J23 headers, there are 4.7 kΩ pull-ups to VDD and 4.7 kΩ pull-down resistors to GND for manual control.

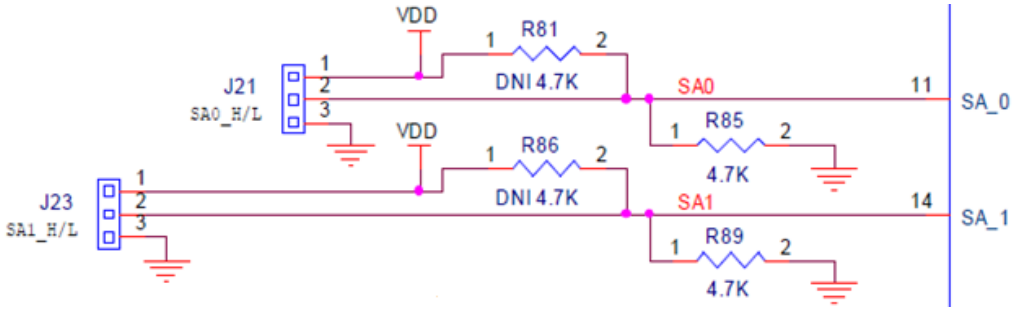


Figure 4. SA_0 & SA_1 Schematic Configuration

OE_n# Pins (Output Enable/Disable Function)

Four of the eight differential outputs can be controlled manually using the convenient High/Low OE_n# jumpers. See Figure 5.

All eight of the OE_n#s can be controlled individually/automatically by using the software GUI. GUI control is accomplished via the USB. See Figure 5.

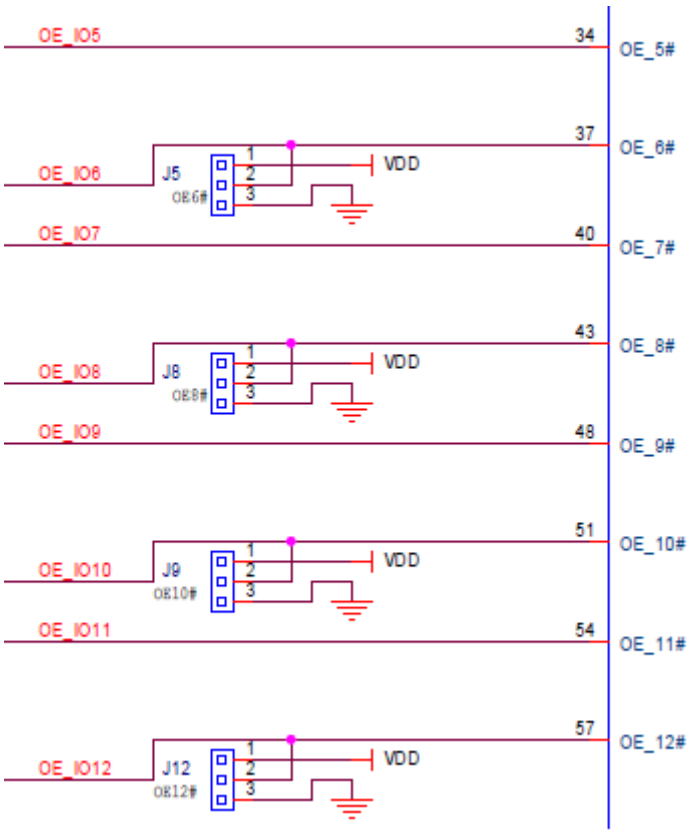


Figure 5. OE_n# Pins Schematic Configuration

100M_133M# – Frequency Selection (J18)

The 100M_133M# frequency selection pin can be controlled manually with the High/Low header jumper J18, H = 100 MHz, L = 133 MHz.



Figure 6. 100M_133M# Pin Schematic Configuration

PWRGD/PWRDN# (J19)

The PWRGD/PWRDN# pin can be controlled manually with the High/Low header jumper J19; H = PWRGD, L = PWRDN#.

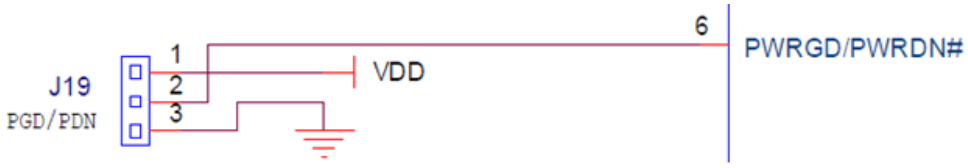


Figure 7. PWRGD/PWRDN# Pin Schematic Configuration

Differential Clock Inputs and Outputs

CLK_IN & CLK_IN# – Differential Clock Inputs

The differential Clock input traces, CLK_IN/CLK_IN#, are equal length routed straight from the SMA connectors on the left side directly to the DUT; there are no vias on metal traces.

CLK_IN & CLK_IN# have resistor pads (R63 & R64) to GND to terminate a signal generator, if used. 50-Ω resistors are installed. **Remove these resistors** if CLK_IN & CLK_IN# are driven by another IC device.

DIF_n and DIF_n# – Differential Outputs

NB3N1900KMNGEVB were designed to measure the differential HCSL outputs with a 50-Ω scope head or high-impedance FET probe. (See Output Schematic in Figure 8)

Six of the nineteen differential outputs are designed to have equal length metal traces from the device pins to the SMA connectors.

The other thirteen differential outputs have shortened metal traces, do not have SMA connectors and can be observed with a high-impedance probe on the metal pads provided.

Each DIF_n/DIF_n# output has a provision for C_{Load}; 2 pF capacitors are installed on all outputs.

R_S & R_P pads are located close to the DUT. R_S = 33-Ω is installed for the NB3N1900K.

NB3N1900K (HCSL Outputs): R_P can be uninstalled on the six output pair with long metal traces to SMA connectors; Use 50-Ω to GND of the oscilloscope head for R_P.

R_P is installed (50-Ω to GND) on the short metal traces without SMA connectors and will use Hi-Z probes.

Table 1. NB3N1900KMNGEVB OUTPUT LOAD AND TERMINATION VS. OSCILLOSCOPE MEASUREMENT

Device	Output Traces	R_S	R_P	C_{Load}	Scope
1900K	Long (1.5″)	33-Ω	Open (DNI) or 50-Ω	2 pF	50-Ω or Hi-Z
1900K	Short	33-Ω	50-Ω	2 pF	Hi-Z

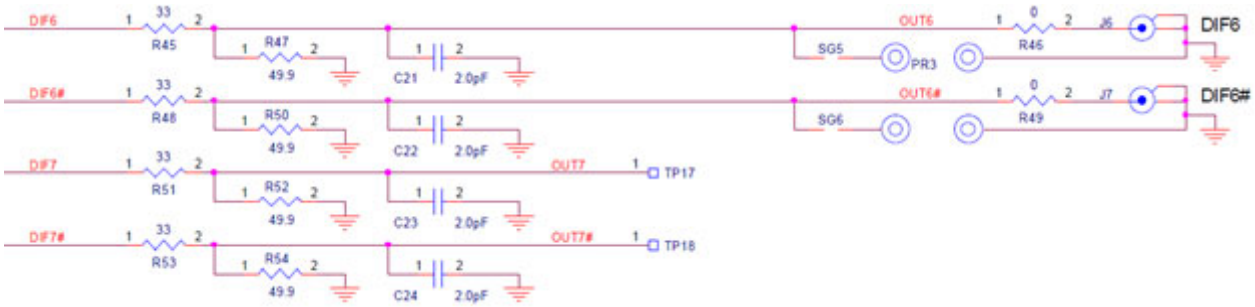


Figure 8. Differential Outputs Schematic Configuration: Long (OUT6) vs. Short (OUT7) Metal Traces

HCSL Output Measurement

HCSL outputs are typically terminated with 50-Ω to ground. Measuring HCSL outputs can be easily accomplished by:

NB3N1900K (HCSL Outputs) – 50-Ω Oscilloscope Head

With R_P removed from board, connect the HCSL outputs through the SMA connectors to the 50-Ω internal impedance of the oscilloscope sampling head.

NB3N1900K (HCSL Outputs) – Use Hi-Z Probe

With R_P installed, use a high-impedance probe on the output's metal trace. Holes for headers to connect to Hi-Z probes are available, but the header pins are not installed.

- Single-ended Hi-Z Probes or,
- Differential Hi-Z Probe;

Misc. Pins

FB_OUT & FB_OUT# – External Termination of Feedback Pins

FB_OUT & FB_OUT# have convenient "test point anvils" to monitor these pins with Hi-Z probe.

NB3N1900K (HCSL): Since the FB_OUT & FB_OUT# pins do not drive transmission lines (no SMAs), the board layout has these pins loaded/terminated at the DUT per datasheet; 83-Ω to GND is installed for the 100-Ω board.

IREF Pin

NB3N1900K (HCSL): The R_{REF} resistor (R99) to GND is for the HCSL output part device.

R_{REF} = 475-Ω is installed for the 100-Ω board.

Graphical User Interface (GUI)

USB & I²C/SMBus Interface

The NB3N1900K EVB has an on-board I²C/SMBus interface circuitry located in the upper left section of the board.

This circuitry will interface with the software program and the device via the SDA and SCL input pins, and can control all twelve of the OE_n# pins, PLL Mode and Frequency Select directly from the GUI.

SCL & SDA

The SMBus Clock (SCL) and Data (SDA) pins are exercised through the on-board I²C interface.

In order to enable the I²C control of the DUT, header jumpers J27 & J28 must be shorted.

The I²C/SMBus interface circuitry is powered separately from the USB type-B connection and is isolated from device VDD and VDDIO.

The SDA and SCL pins can also be externally accessed by an off-board programmer, allowing other SMBus emulators to be used to program the DUT. If used, remove both jumpers J27 & J28. “Test-point anvils” TP33 & TP34 are available for external control of the device with the use with mini-grabber cables.

To receive the GUI software and GUI software manual please contact below:



QUICK START LAB SET-UP USER'S GUIDE

Pre-Power-Up

1. Connect power supply cables to VDD, VDDIO and GND banana jacks; (do not turn power on, yet).
2. Connect a signal generator to the SMA connectors for the CLK_IN & CLK_IN# inputs.
3. 50-Ω termination resistors are installed for a signal generator on the board. Set appropriate input signal levels; (HCSL input, VIL = 0 V, VIH = 700 mV, Frequency 100.00 or 133.33 MHz).
4. Ensure the PWRGD/PWRDN# pin is in the Low state before power up (PWRDN#). There is a jumper on pin 6 to easily select between High and Low. See Figure 7.
5. The 100M_133M# and HBW_BYP_LBW pins need to be hardware selected with jumpers. See Figures 3 and 6.
6. Connect the DIF_n/DIF_n# outputs to the appropriate oscilloscope.

Table 2. POWER SUPPLY CONNECTIONS

Device Pin Power Supply Connector	Power Supply
VDD, VDDIO	VCC = +3.3 V
GND	0 V

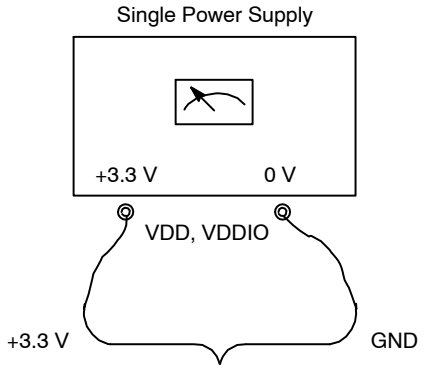


Figure 9. Power Supply Connections

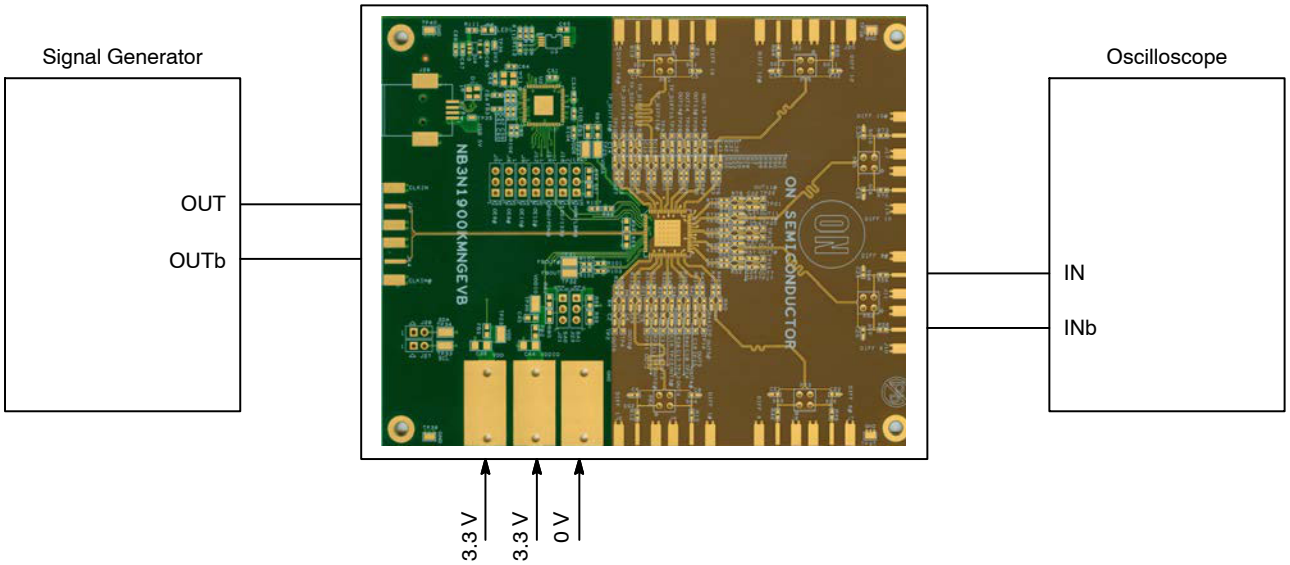


Figure 10. Typical Lab Test Set-Up

Power-Up Sequence

1. Turn on power supply, 3.3 V (VDD & VDDIO)
2. Move PWRGD/PWRDN# jumper from Low to logic High, PWRGD position
3. Turn on the Differential Clock Signal for the CLK_IN inputs
4. Monitor DIF_n/DIF_n# outputs on oscilloscope

Optional

Graphical User Interface

There is a stand-alone Graphical User Interface software package and user's manual that will interface with the DUT via the USB connector.

1. Connect the USB port on the evaluation board to a USB port on the PC via cable.
2. See the stand-alone GUI instructions document.
3. Allow Windows to install the necessary drivers for the eval board USB interface hardware.
4. Start the GUI program.

Table 3. BILL OF MATERIALS FOR THE NB3N1900KMNGEVB

Ref. Des.	Qty	Part#	Value	PCB Footprint	Vendor	Vendor PN	Manufacturer
B1	1		PC Board, Clock Fanout Board		HiQ Electronics	NB3N1900KMNGEVB	
C1−C35, C37, C42, C43	38	C1005C0G1H020C	2.0 pF	C0402	Digi-Key	445-4863-1-ND	TDK
C36, C44	2	TR3A106K010C2000	10 μF	C1206	Digi-Key	718-1300-1-ND	Vishay
C38, C40, C67, C68	4	GRM155R61A105ME15D	1 μF	C0402	Digi-Key	490-5409-1-ND	Murata
C39, C41, C46−C54, C56−C58, C60, C62, C65, C69	18	0402ZD104KAT2A	100 nF	C0402	Digi-Key	478-1129-1-ND	AVX
C45	1	C1608X5R1A106M	10 μF	C0603	Digi-Key	445-6853-1-ND	TDK
C55, C59, C61	3	C1005X5R0J475M	4.7 μF	C0402	Digi-Key	445-7395-1-ND	TDK
C63	1	0402YC103KAT2A	10 nF	C0402	Digi-Key	478-1114-1-ND	AVX
C64, C66	2	GRM1555C1H100JZ01D	10 pF	C0402	Digi-Key	490-1278-1-ND	Murata
D1	1	PACDN004SR	PACDN004	SOT_143	Mouser	748-PACDN004SR	**onsemi**
FB1, FB2	2	BLM18KG601SN1D	600	L0603	Digi-Key	490-5258-1-ND	Murata
FB3, FB4	2	BLM15AG601SN1D	600	L0402	Digi-Key	490-1006-1-ND	Murata
H1, H2, H3, H4	4		.129 Hole in .240 Round Pad	HOLE_0.240R0.129 _PTH			
J1−J4, J6, J7, J10, J11, J13, J14, J15, J17, J20, J22	14	142-0701-801	SMA Jack, End Launch	SMA_Jack_End_Launch	Digi-key	J502-ND	Johnson Components
J5, J8, J9, J12, J16, J18, J19, J21, J23	9	961103-6404-AR	Header 3-pin	HDR_1X3_2P54	Digi-Key	3M9448-ND	3M
J24	1	571-0500	Banana Jack, Thru-Hole, Red	con_571-0500	Mouser	164-6219	Deltron
J25	1	571-0700	Banana Jack, Thru-Hole, Yellow	con_571-0500	Mouser	164-7170	Deltron
J26	1	571-0100	Banana Jack, Thru-Hole, Black	con_571-0500	Mouser	164-6218	Deltron
J27, J28	2	961102-6404-AR	Header 2-pin	HDR_1X2_2P54	Digi-Key	3M9447-ND	3M
J29	1	USB-B1SMHSW6	Conn, USB−B, SMT	Con_USB_B_RA	Digi-Key	ED2994-ND	On Shore Technology
LED1	1	LTST-C190KGKT	LED, Green	LED_0603	Digi-Key	160-1435-1-ND	Lite-On
M1−M8, M10	9	QPC02SXGN-RC	Shunt		Digi-Key	S9337-ND	Sullins
M9, M11−M13	4	1808	Standoff, 4−40 1/4 × 5/8		Digi-Key	1808K-ND	Keystone
M14−M17	4	PMS 440 0025 PH	Screw, 4−40 × 0.25, PHP		Digi-Key	H342-ND	Building Fasteners
PR1−PR6	6	No Part	4 Round Pads, .060 with .040 Hole	BERG_2X2_2P54			
R1, R2, R5, R6, R10, R11, R14, R18, R19, R22, R25, R27, R30, R31, R32, R34, R37, R39, R41, R43, R45, R48, R51, R53, R55, R58, R61, R65, R69, R72, R75, R77, R79, R83, R88, R92, R95, R97	38		33 Ω	R0402	Digi-Key	P33JTR-ND	Panasonic
R3, R7, R16, R20, R23, R28, R33, R35	8		49.9 Ω	R0402	Digi-Key	P49.9LCT-ND	Panasonic

Table 3. BILL OF MATERIALS FOR THE NB3N1900KMNGEVB (continued)

Ref. Des.	Qty	Part#	Value	PCB Footprint	Vendor	Vendor PN	Manufacturer
R4, R8, R17, R21, R24, R26, R29, R36, R38, R40, R42, R44, R47, R50, R52, R54, R57, R60, R62, R66, R71, R74, R76, R78, R82, R87, R90, R94, R96, R98	30		49.9 Ω	R0402	Digi-Key	P49.9LCT-ND	Panasonic
R9, R12, R13, R15, R46, R49, R56, R59, R70, R73, R80, R84	12	CRCW04020000Z0ED	0 Ω	R0402	Digi-Key	541-0.0JCT-ND	Vishay
R63, R64	2	ERJ-3EKF49R9V	49.9 Ω	R0603	Digi-Key	P49.9HCT-ND	Panasonic
R67, R68, R85, R89	4	ERJ-3GEYJ472V	4.7 kΩ	R0603	Digi-Key	P4.7KGCT-ND	Panasonic
R81, R86	2	ERJ-3GEYJ472V	4.7 kΩ	R0603	Dig-Key	P4.7KGCT-ND	Panasonic
R91, R93	2	ERJ-3GEYJ2R2V	2.2 Ω	R0603	Digi-Key	P2.2GCT-ND	Panasonic
R99	1	ERJ-2RKF4750X	475 Ω	R0402	Digi-Key	P475LCT-ND	Panasonic
R100, R102	2	ERJ-2GE0R00X	0 Ω	R0402	Digi-Key	P0.0JCT-ND	Panasonic
R101, R103	2	ERJ-2RKF82R5X	82.5 Ω	R0402	Digi-Key	P82.5LCT-ND	Panasonic
R104−R106, R108−R110	6	ERJ-2GEJ103X	10 kΩ	R0402	Digi-Key	P10KJCT-ND	Panasonic
R107	1	ERJ-2RKF1202X	12 kΩ	R0402	Digi-Key	P12.0KLCT-ND	Panasonic
R111	1	ERJ-2GEJ471X	470 Ω	R0402	Digi-Key	P470JCT-ND	Panasonic
R112	1	ERJ-2GEJ222X	2.2 kΩ	R0402	Digi-Key	P2.2KJCT-ND	Panasonic
SG1−SG12	12	No Part	Solder Gap	R0201			
TP1−TP22, TP24, TP26, TP28, TP29	26		Test Pad 30 × 30 mil	tp_30_30			
TP23, TP25, TP27, TP30−TP34	8	5015	Test Point, SMT	tp_70_135	Digi-Key	5015KCT-ND	Keystone
TP35, TP36	2	No Part	Test Pad 30 × 60 mil	tp_30_60			
TP37−TP40	4	No Part	Test Pad 50 × 100 mil	tp_50_100			
U1	1	NB3N1900KMNG	DNI NB3N1900K	QFN_72P_0P5MM	−	−	**onsemi**
U2	1	FT2232HQ-REEL	FT2232H	QFN_64_0p5	Digi-Key	768-1025-1-ND	FTDI
U3	1	93LC46BT-I/ST	93LC46B	TSSOP_8_4p4W_0P65	Digi-Key	93LC46BT-I/STCT-ND	Microchip
U4	1	NCP4586DSN33T1G	NCP4586, 3.3 V	SOT23_5p	**onsemi**	NCP4586DSN33T1G	**onsemi**
Y1	1	ABM8G-12.000MHZ-4Y-T3	12 MHz	Cry-4p-SMD1	Digi-Key	535-10901-1-ND	Abracon Corp

REVISION HISTORY

Revision	Description of Changes	Date
2	Rebranded document to current **onsemi** format. Updated R99, R101, and R103 part numbers in the page 9 BOM table.	11/16/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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