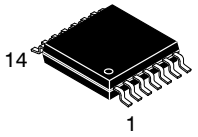
# Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop

# 74LVX74




**TSSOP−14 WB**
**CASE 948G**

### General Description

The LVX74 is a dual D−type flip−flop with Asynchronous Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

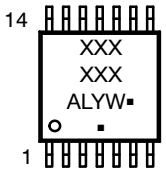
Asynchronous Inputs:

- LOW Input to $\overline{S}_D$ (Set) Sets Q to HIGH Level
- LOW Input to $\overline{C}_D$ (Clear) Sets Q to LOW Level
- Clear and Set are Independent of Clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ Makes Both Q and $\overline{Q}$ HIGH

### Features

- Input Voltage Level Translation from 5 V to 3 V
- Ideal for Low Power/Low Noise 3.3 V Applications
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance
- Pb−Free, Halogen Free/BFR Free and RoHS Compliant

### MARKING DIAGRAM



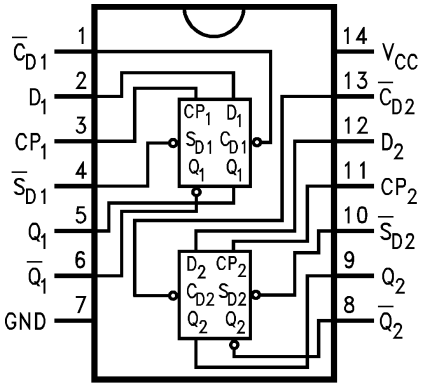

| | |
|---|---|
| XXX | = Specific Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

### Connection Diagram



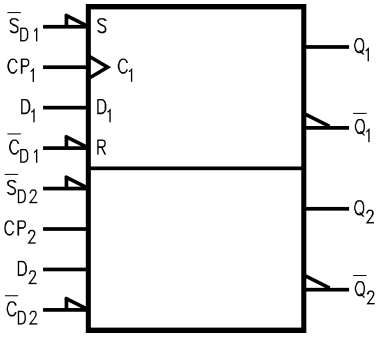

### Pin Description

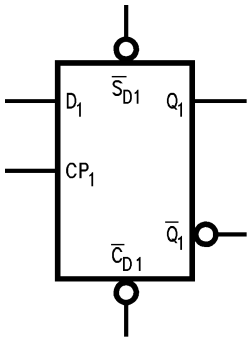
| Pin Names | Description |
|---|---|
| $D_1$, $D_2$ | Data Inputs |
| $CP_1$, $CP_2$ | Clock Pulse Inputs |
| $\overline{C}_{D1}$, $\overline{C}_{D2}$ | Direct Clear Inputs |
| $\overline{S}_{D1}$, $\overline{S}_{D2}$ | Direct Set Inputs |
| $Q_1$, $\overline{Q}_1$, $Q_2$, $\overline{Q}_2$ | Outputs |

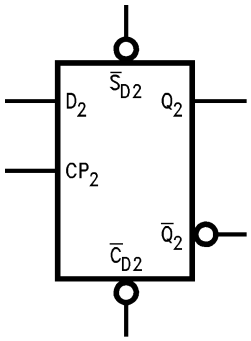
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## Logic Symbols

IEEE/IEC




## Truth Table

(Each Half)

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| $\overline{S}_D$ | $\overline{C}_D$ | CP | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H | H |
| H | H | ↗ | H | H | L |
| H | H | ↗ | L | L | H |
| H | H | L | X | $Q_0$ | $\overline{Q}_0$ |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW−to−HIGH Clock Transition
$Q_0$ ($\overline{Q}_0$) = Previous Q ($\overline{Q}$) before LOW−to−HIGH Transition of Clock



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## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | | Rating | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | –0.5 to +6.5 | V |
| $I_{IK}$ | DC Input Diode Current, $V_I$ = –0.5 V | | –20 | mA |
| $V_I$ | DC Input Voltage | | –0.5 to +6.5 | V |
| $I_{OK}$ | DC Output Diode Current | $V_O$ = –0.5 V | –20 | mA |
| | | $V_O$ = $V_{CC}$ + 0.5 V | +20 | mA |
| $V_O$ | DC Output Voltage | | –0.5 to $V_{CC}$ + 0.5 | V |
| $I_O$ | DC Output Source or Sink Current | | ±25 | mA |
| $I_{CC}$ or $I_{GND}$ | DC $V_{CC}$ or Ground Current | | ±50 | mA |
| $T_{STG}$ | Storage Temperature | | –65 to +150 | °C |
| $P_D$ | Power Dissipation | | 833 | mW |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS (Note 1)

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2.0 to 3.6 | V |
| $V_I$ | Input Voltage | 0 to 5.5 | V |
| $V_O$ | Output Voltage | 0 to $V_{CC}$ | V |
| $T_A$ | Operating Temperature | –40 to +85 | °C |
| $\Delta t / \Delta V$ | Input Rise and Fall Time | 0 to 100 | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.



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## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | $V_{CC}$ (V) | Conditions | $T_A$ = 25°C | | | $T_A$ = −40°C to +85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $V_{IH}$ | HIGH Level Input Voltage | 2.0 | | 1.5 | – | – | 1.5 | – | V |
| | | 3.0 | | 2.0 | – | – | 2.0 | – | |
| | | 3.6 | | 2.4 | – | – | 2.4 | – | |
| $V_{IL}$ | LOW Level Input Voltage | 2.0 | | – | – | 0.5 | – | 0.5 | V |
| | | 3.0 | | – | – | 0.8 | – | 0.8 | |
| | | 3.6 | | – | – | 0.8 | – | 0.8 | |
| $V_{OH}$ | HIGH Level Output Voltage | 2.0 | $V_{IN} = V_{IL}$ or $V_{IH}$, $I_{OH} = -50$ μA | 1.9 | 2.0 | – | 1.9 | – | V |
| | | 3.0 | $V_{IN} = V_{IL}$ or $V_{IH}$, $I_{OH} = -50$ μA | 2.9 | 3.0 | – | 2.9 | – | |
| | | | $V_{IN} = V_{IL}$ or $V_{IH}$, $I_{OH} = -4$ mA | 2.58 | – | – | 2.48 | – | |
| $V_{OL}$ | LOW Level Output Voltage | 2.0 | $V_{IN} = V_{IL}$ or $V_{IH}$, $I_{OL} = 50$ μA | – | 0.0 | 0.1 | – | 0.1 | V |
| | | 3.0 | $V_{IN} = V_{IL}$ or $V_{IH}$, $I_{OL} = 50$ μA | – | 0.0 | 0.1 | – | 0.1 | |
| | | | $V_{IN} = V_{IL}$ or $V_{IH}$, $I_{OL} = 4$ mA | – | – | 0.36 | – | 0.44 | |
| $I_{IN}$ | Input Leakage Current | 3.6 | $V_{IN}$ = 5.5 V or GND | – | – | ±0.1 | – | ±1.0 | μA |
| $I_{CC}$ | Quiescent Supply Current | 3.6 | $V_{IN} = V_{CC}$ or GND | – | – | 2.0 | – | 20.0 | μA |

## NOISE CHARACTERISTICS (Note 2)

| Symbol | Characteristic | $V_{CC}$ (V) | $C_L$ (pF) | $T_A$ = 25°C | | Unit |
|---|---|---|---|---|---|---|
| | | | | Typ | Limit | |
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 3.3 | 50 | 0.3 | 0.5 | V |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | 3.3 | 50 | −0.3 | −0.5 | V |
| $V_{IHD}$ | Minimum HIGH Level Dynamic Input Voltage | 3.3 | 50 | – | 2.0 | V |
| $V_{ILD}$ | Maximum LOW Level Dynamic Input Voltage | 3.3 | 50 | – | 0.8 | V |

2. Input $t_r = t_f$ = 3.0 ns



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## AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | $V_{CC}$ (V) | $C_L$ (pF) | $T_A$ = 25°C | | | $T_A$ = −40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay $CP_n$ to $Q_n$ or $\overline{Q}_n$ | 2.7 | 15<br>50 | –<br>– | 7.3<br>9.8 | 15.0<br>18.5 | 1.0<br>1.0 | 18.5<br>22.0 | ns |
| | | 3.3 ± 0.3 | 15<br>50 | –<br>– | 5.7<br>8.2 | 9.7<br>13.2 | 1.0<br>1.0 | 11.5<br>15.0 | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay $\overline{C}_{Dn}$ to $\overline{S}_{Dn}$ to $Q_n$ or $\overline{Q}_n$ | 2.7 | 15<br>50 | –<br>– | 8.4<br>10.9 | 15.6<br>19.1 | 1.0<br>1.0 | 18.5<br>22.0 | ns |
| | | 3.3 ± 0.3 | 15<br>50 | –<br>– | 6.6<br>9.1 | 10.1<br>13.6 | 1.0<br>1.0 | 12.0<br>15.5 | |
| $t_W$ | $CP_n$ or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width | 2.7 | – | 8.5 | – | – | 10.0 | – | ns |
| | | 3.3 ± 0.3 | – | 6.0 | – | – | 7.0 | – | |
| $t_S$ | Setup Time, $D_n$ to $CP_n$ | 2.7 | – | 8.0 | – | – | 9.5 | – | ns |
| | | 3.3 ± 0.3 | – | 5.5 | – | – | 6.5 | – | |
| $t_H$ | Hold Time, $D_n$ to $CP_n$ | 2.7 | – | 0.5 | – | – | 0.5 | – | ns |
| | | 3.3 ± 0.3 | – | 0.5 | – | – | 0.5 | – | |
| $t_{REC}$ | Recovery Time, $\overline{C}P_n$ or $\overline{S}_{Dn}$ to $CP_n$ | 2.7 | – | 6.5 | – | – | 7.5 | – | ns |
| | | 3.3 ± 0.3 | – | 5.0 | – | – | 5.0 | – | |
| $f_{MAX}$ | Maximum Clock Frequency | 2.7 | 15<br>50 | 55<br>45 | 135<br>60 | –<br>– | 50<br>40 | –<br>– | MHz |
| | | 3.3 ± 0.3 | 15<br>50 | 95<br>60 | 145<br>85 | –<br>– | 80<br>50 | –<br>– | |
| $t_{OSLH}$, $t_{OSHL}$ | Output to Output Skew (Note 3) | 2.7 | 50 | – | – | 1.5 | – | 1.5 | ns |
| | | 3.3 | | – | – | 1.5 | – | 1.5 | |

3. Parameter guaranteed by design $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

## CAPACITANCE

| Symbol | Parameter | $T_A$ = 25°C | | | $T_A$ = −40 to +85°C | | Unit |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | |
| $C_{IN}$ | Input Capacitance | – | 4 | 10 | – | 10 | pF |
| $C_{PD}$ | Power Dissipation Capacitance (Note 4) | – | 25 | – | – | – | pF |

4. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \dfrac{C_{PD} \times V_{CC} \times f_{IN} \times I_{CC}}{2 \text{ (per F/F)}}$

## ORDERING INFORMATION

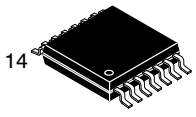
| Device | Package | Marking | Shipping† |
|---|---|---|---|
| 74LVX74MTCX | TSSOP−14 | LVX<br>74 | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

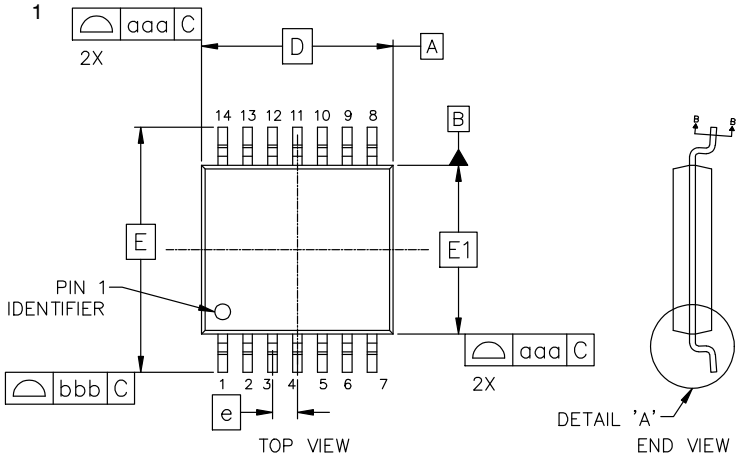


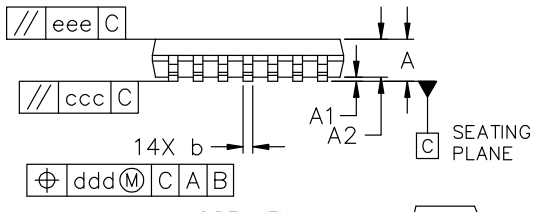
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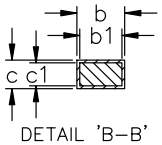


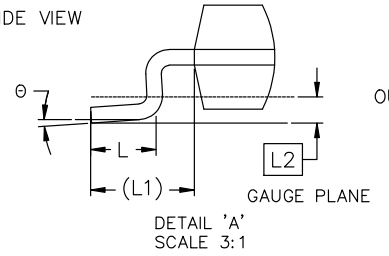
**TSSOP−14 5.00x4.40x0.95, 0.65P**
CASE 948G
ISSUE D

DATE 30 JUN 2026

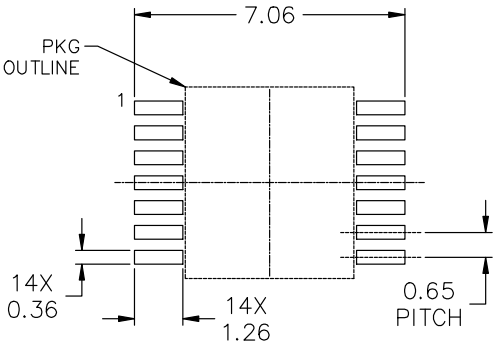



| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | −−− | −−− | 1.20 |
| A1 | 0.05 | 0.10 | 0.15 |
| A2 | 0.85 | 0.95 | 1.05 |
| b | 0.19 | 0.25 | 0.30 |
| b1 | 0.19 | 0.22 | 0.25 |
| c | 0.09 | 0.15 | 0.20 |
| c1 | 0.09 | 0.12 | 0.16 |
| D | 5.00 BSC | | |
| E | 6.40 BSC | | |
| E1 | 4.40 BSC | | |
| e | 0.65 BSC | | |
| L | 0.50 | 0.63 | 0.75 |
| L1 | 1.00 REF | | |
| L2 | 0.25 BSC | | |
| θ | 0° | 4° | 8° |
| TOLERANCE FORM & POSITION | | | |
| aaa | 0.10 | | |
| bbb | 0.15 | | |
| ccc | 0.08 | | |
| ddd | 0.10 | | |
| eee | 0.10 | | |

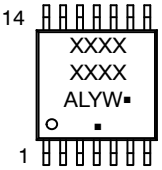



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D DOES NOT INCLIDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

**GENERIC MARKING DIAGRAM***




A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **TSSOP−14 5.00x4.40x0.95, 0.65P** | **PAGE 1 OF 1** |

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